

Drain Current Model of Graphene Channel G^4 -FET and Gate-All-Around MOSFET

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Abstract: Potential distribution and Wave function distribution are obtained by solving 2-D Poisson-Schrödinger equation using COMSOL with MATLAB. Conduction band profile and carrier density are investigated. Drain current of Graphene Channel Four Gate Transistor (G^4 -FET) and Gate-All-Around (GAA) MOSFET are calculated and compared.

Keywords: Four Gate Transistor (G^4 -FET), Gate-All-Around (GAA), 2-D Poisson-Schrödinger equation, potential distribution, Wave function distribution, Drain current

I. INTRODUCTION

Transistors are the main components of all modern electronic devices [1]. At-first Bipolar Junction Transistor (BJT) was invented by W.B. Shockley at the Bell Telephone Laboratories in 1948 [2]. To develop the nano-electronics technology BJT is replaced by Metal Oxide Semiconductor Field Effect Transistor (MOSFET) which is invented in 1960's [3]. The continuous scaling of GAA silicon nanowire Field Effect Transistor (FET) [4],[5] shows better control of short channel effect over other structures [6] due to their gate controllability, low leakage, high on-off ratio and carrier transport property [7].

Z. Chen et al. [8] discussed the fabrication process and device measurements of GAA Carbon Nanotube FET (GAA-CNFET) with an ' Ω ' shaped model. S. Garg et al. [9] have calculated threshold voltage using centre potential and the effect of device parameters on threshold voltage of cylindrical GAA MOSFET [10], [11].

Saeed et al. [12] proposed an analytical model to calculate gate capacitance and drain current of GAA nanowire MOSFET with group III-V channel [13]. S. Jahangir et al. [14], [15] have shown a numerical model which was developed to obtain the potential distribution [16], [17] solving 2-D Poisson equation in Depletion-All-Around (DAA) operation of n-channel Silicon-On-Insulator (SOI) G^4 -FET. Ballistic current-voltage model in DAA was also shown in [18]. In this paper, Graphene which has lower relative permittivity and very higher mobility than Silicon is used as the channel of G^4 -FET and GAA MOSFET to increase the potential distribution and drain current. In this work, potential profile, conduction band profile, carrier distribution and the drain current of three structures are calculated and compared.

II. G^4 -FET AND GAA MOSFET STRUCTURES

The G^4 -FET is a double gate MOSFET consisting of two lateral junction-gates. It has a lateral double-gate MOS consisting of two vertical MOS gates (top-gate and back-gate). Under appropriate gate bias voltages, the performance and properties of the device are affected by the presence of inversion layers under MOS gates because the junction gates are interconnected through the channel. There are two types of structure of GAA MOSFET: rectangular and cylindrical. In GAA MOSFETs, the gate oxide and the gate electrodes wrap around the channel region. In this paper, Graphene is used as the channel in G^4 -FET and GAA MOSFET. I_D flows through the Graphene and the conducting channel surrounded by depletion regions.

In G^4 -FET device structure (Fig. 1(a)), the channel width and channel thickness are 90 nm, gate oxide and buried oxide thickness are 15 nm, top and bottom gate thickness are 10 nm. The doping density of junction gate is $N_A = 2 \times 10^{26} \text{ m}^{-3}$ and the channel doping density is $N_D = 5 \times 10^{23} \text{ m}^{-3}$.

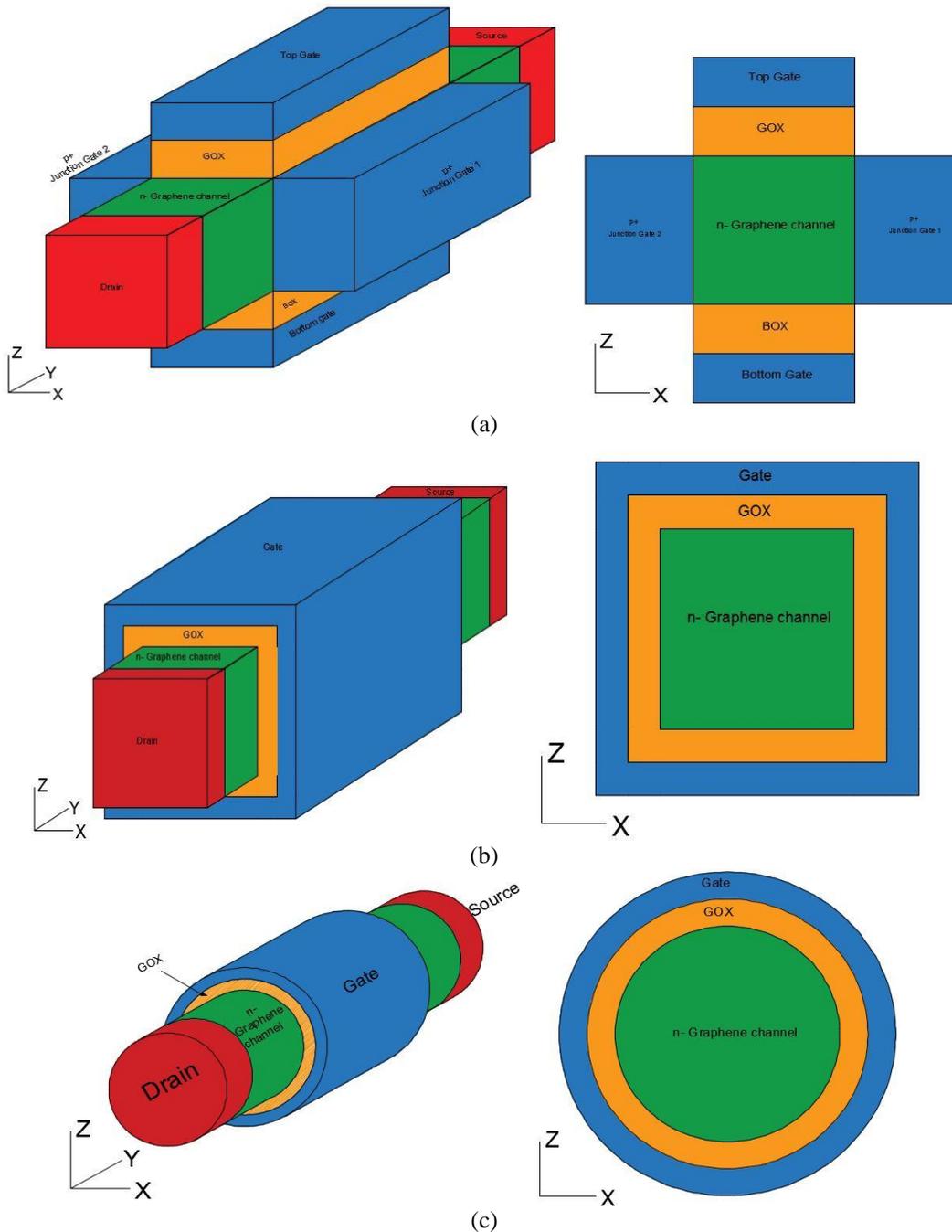


Fig. 1. 3-D structure and cross-section between drain to source (a) for n-Graphene channel G^4 -FET, (b) for n-Graphene channel rectangular GAA MOSFET, (c) for n-Graphene channel cylindrical GAA MOSFET

In rectangular GAA MOSFET (Fig. 1(b)), the channel width and channel thickness are 90 nm, surrounding gate oxide thickness is 15 nm and surrounding gate thickness is 10 nm.

In cylindrical GAA MOSFET (Fig. 1(c)), the channel diameter is 90 nm, surrounding gate oxide thickness is 15 nm and surrounding gate thickness is 10 nm.

In all the three structures, the gate oxide thickness and gate thicknesses are the same and the other dimensions are comparable to make the analyses on the same footing. For example, the channel diameter of cylindrical GAA MOSFET, the channel width and the thickness of rectangular GAA MOSFET and the channel width of G^4 -FET device structure are all 90 nm.

III. SOLVING METHOD

In this paper, Potential distributions are calculated by solving 2-D Poisson equation using COMSOL with MATLAB at any cross-section of n-Graphene channel G⁴-FET and GAA MOSFET.

2-D Poisson equation is:

$$-\epsilon_0 \epsilon_r \left[\frac{\partial^2 V(x,y)}{\partial x^2} + \frac{\partial^2 V(x,y)}{\partial y^2} \right] = \rho_{\text{depl}} \quad (1)$$

where, ϵ_0 = permittivity of free space, ϵ_r = relative permittivity, ρ_{depl} = depletion charge density = qN_D .

A coefficient form is used for solving 2-D Poisson equation in COMSOL which is:

$$-\nabla \cdot (c \nabla u) = f \quad (2)$$

Comparing equation (1) with (2)

$$c \equiv \epsilon_0 \epsilon_r, \quad u \equiv V(x,y) \quad \text{and} \quad f \equiv \rho_{\text{depl}}$$

Wave function distributions are calculated by solving 2-D Schrödinger equation using COMSOL with MATLAB at any cross-section of n-Graphene channel G⁴-FET and GAA MOSFET.

2-D Schrödinger equation is:

$$-\frac{\hbar^2}{2m_{y1}^*} \frac{d^2}{dy^2} \varphi_{ij}(y,z) - \frac{\hbar^2}{2m_{z1}^*} \frac{d^2}{dz^2} \varphi_{ij}(y,z) + v(y,z) \varphi_{ij}(y,z) = E_{ij} \varphi_{ij}(y,z) \quad (3)$$

where, $v(y,z)$ = conduction band profile, E_{ij} = eigen energy, $\varphi_{ij}(y,z)$ = wave function distribution, m_{y1} , m_{z1} = directional effective masses.

A coefficient form is used for solving 2-D Schrödinger equation in COMSOL which is:

$$-\nabla \cdot (c \nabla u) + au = \lambda u \quad (4)$$

Comparing equation (3) with (4)

$$a \equiv v(y,z), \quad u \equiv \varphi_{ij}(y,z), \quad \lambda \equiv E_{ij}, \quad c = \begin{bmatrix} \frac{\hbar^2}{2m_{y1}^*} & 0 \\ 0 & \frac{\hbar^2}{2m_{z1}^*} \end{bmatrix}$$

IV. DRAIN CURRENT MODEL

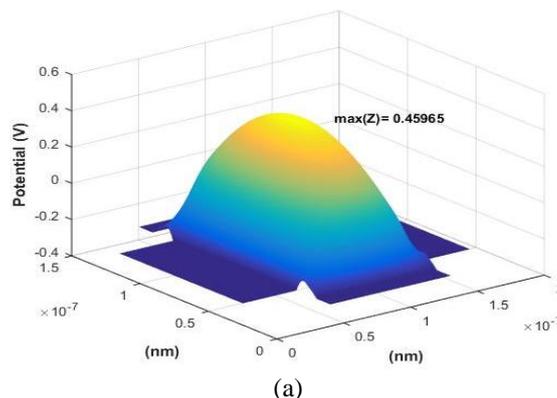
After solving 2-D Poisson- Schrödinger equation, the drain current is calculated by equation (5),

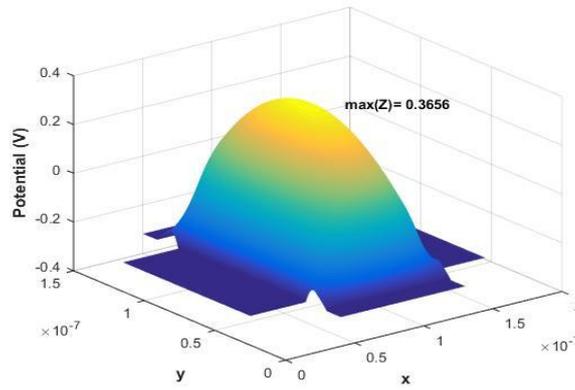
$$\frac{I_D}{W} = \left[\frac{q}{\hbar^2} \sqrt{\frac{m_c}{2}} \left(\frac{k_B T}{\pi} \right)^{\frac{3}{2}} \right] \left\{ \mathcal{F}_1 \left[\frac{(E_F - E_i)}{k_B T} \right] - \mathcal{F}_1 \left[\frac{(E_F - E_i - qV_D)}{k_B T} \right] \right\} \quad (5)$$

Where, m_c = conductivity effective mass, E_i = subband energy, \mathcal{F}_1 = Fermi-Dirac integral of order one-half which is defined by Blakemore [19].

V. RESULTS AND DISCUSSION

The potential profile for n-Graphene channel G⁴-FET and GAA MOSFET are shown. Fig. 2 shows the potential profile under appropriate gate bias voltage for Graphene channel G⁴-FET and Silicon channel G⁴-FET.





(b)

Fig. 2. Potential profile at bias conditions: $V_{tg} = -0.28$ V, $V_{bg} = -0.28$ V, $V_{jg1} = -0.28$ V, $V_{jg2} = -0.28$ V and $V_d = 0.25$ V, $V_s = 0$ V. (a) for n-Graphene channel G^4 -FET ,(b) for n-Silicon channel G^4 -FET

Maximum potential of Graphene channel G^4 -FET is higher than Silicon channel G^4 -FET because Graphene has lower relative permittivity than silicon.

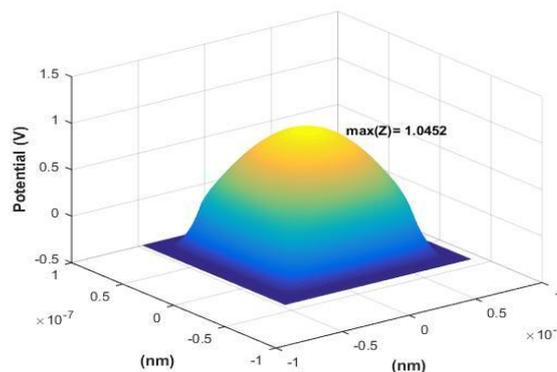


Fig. 3. Potential profile at bias conditions: $V_{tg} = -0.28$ V, $V_d = 0.25$ V, $V_s = 0$ V for n-Graphene channel rectangular GAA MOSFET

Under appropriate gate bias voltage, the potential distribution is calculated for rectangular GAA MOSFET in Fig. 3. Maximum potential is higher than Graphene channel G^4 -FET because channel is surrounded by gate oxide in rectangular GAA MOSFET.

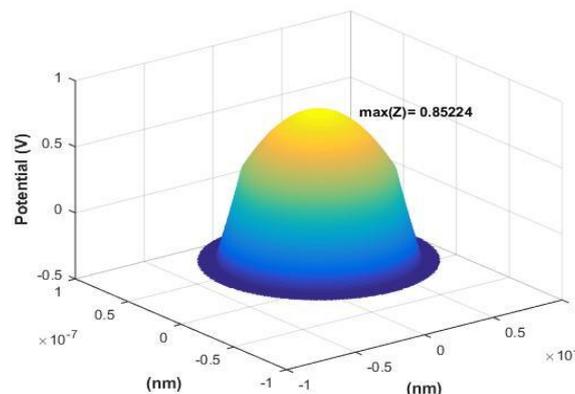


Fig. 4. Potential profile at bias conditions: $V_{tg} = -0.28$ V, $V_d = 0.25$ V, $V_s = 0$ V for n-Graphene channel cylindrical GAA MOSFET

For cylindrical GAA MOSFET, Fig. 4 shows the potential distribution under appropriate gate bias voltage. Maximum potential of cylindrical GAA MOSFET is increased compared to Graphene channel G^4 -FET, but lower than rectangular GAA MOSFET for different structures of MOSFET (Table I).

Table I Comparison Of Potential Profile Between G⁴-Fet And Gaa Mosfet

Properties	n-Silicon channel G ⁴ -FET	n-Graphene channel G ⁴ -FET	n-Graphene channel rectangular GAA MOSFET	n-Graphene channel cylindrical GAA MOSFET
Maximum Potential	0.36 V	0.46 V	1.04 V	0.85 V

Conduction band profiles of G⁴-FET and GAA MOSFET are calculated from potential profile. Fig. 5 shows the conduction band profiles.

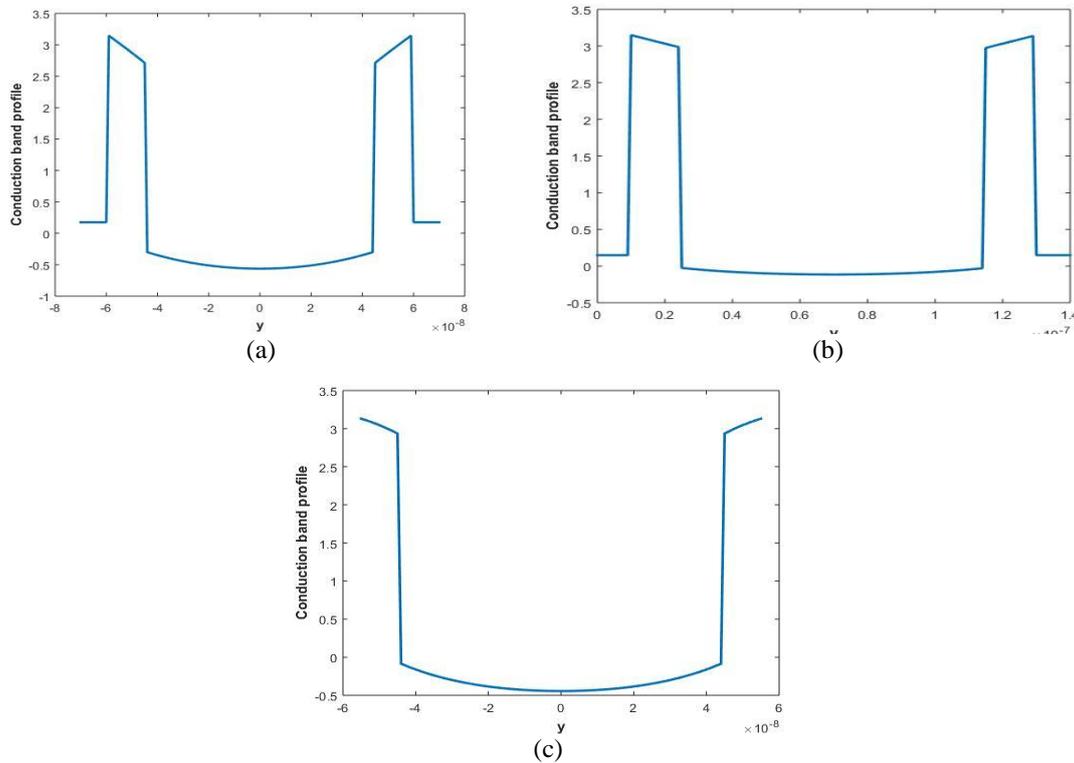
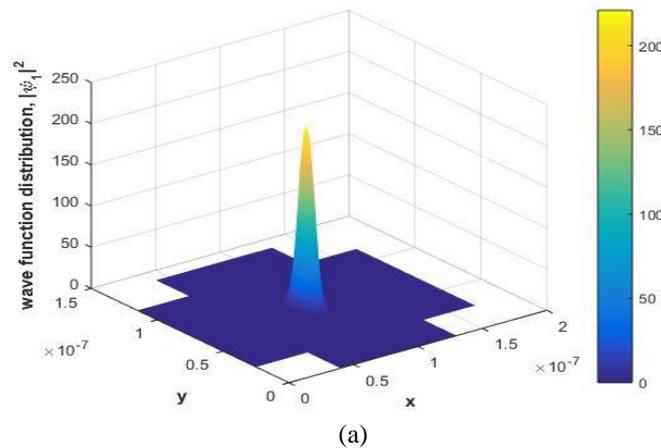


Fig. 5. Cross-section view of Conduction band profiles at $V_{tg} = -0.28$ V (a) for n-Graphene channel G⁴-FET, (b) for n-Graphene channel rectangular GAA MOSFET, (c) for n-Graphene channel cylindrical GAA MOSFET

2-D Schrödinger equation is solved for corresponding the conduction band profile to obtain the different eigen states (i.e. subbands). The wave function distributions are also calculated corresponding the different subbands. Fig. 6 shows the wave function distributions for three structures.



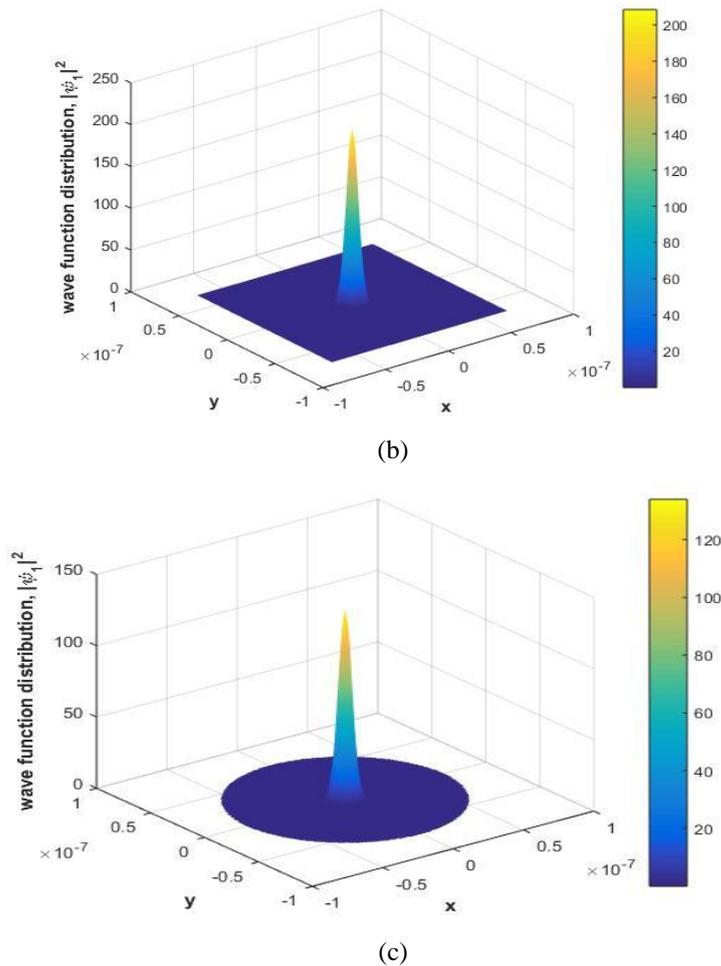
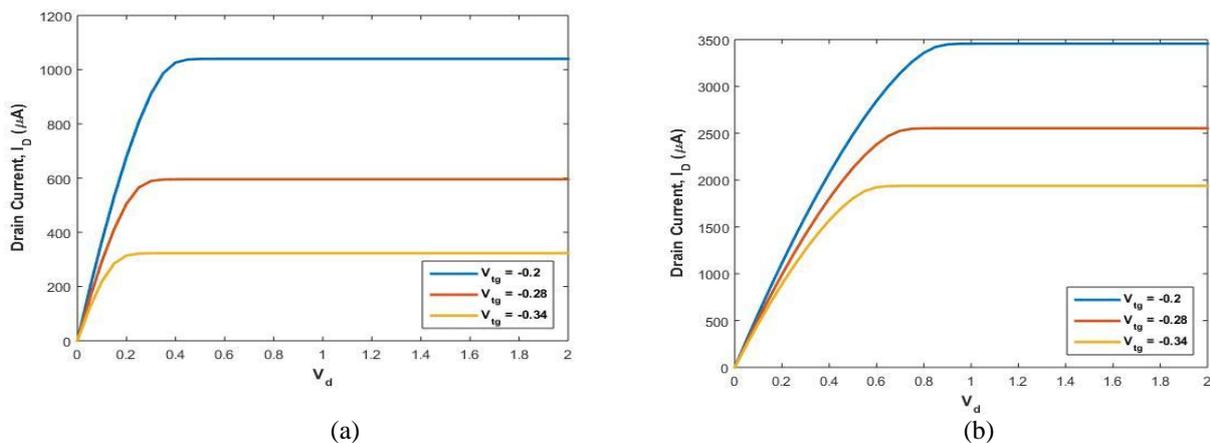


Fig. 6. carrier density corresponding to 1st eigen at $V_{tg} = -0.28$ V (a) for n-Graphene channel G⁴-FET, (b) for n-Graphene channel rectangular GAA MOSFET, (c) for n-Graphene channel cylindrical GAA MOSFET

After solving 2-D Poisson-Schrödinger equation, the drain current is calculated by equation (5) where Fermi-Dirac integral of order one-half is used which is defined by Blakemore [19]. Fig. 7 shows the drain current for n-Graphene channel G⁴-FET and GAA MOSFET. Drain current increases due to increasing gate bias voltages.



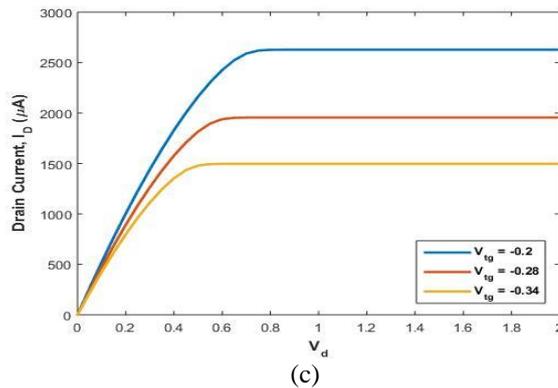


Fig. 7. Drain Current vs Drain Voltage at $V_{tg} = -0.34$ V, $V_{tg} = -0.28$ V and $V_{tg} = -0.2$ V (a) for n-Graphene channel G^4 -FET, (b) for n-Graphene channel rectangular GAA MOSFET, (c) for n-Graphene channel cylindrical GAA MOSFET

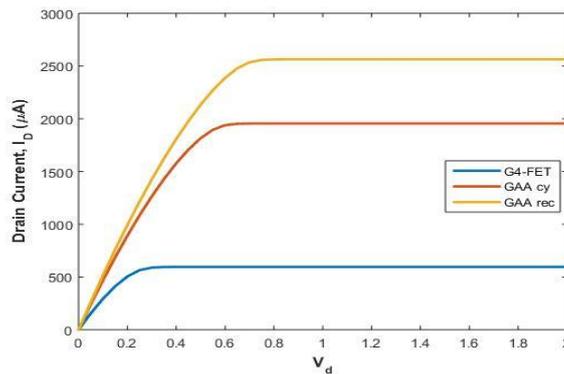


Fig. 8. drain current vs Drain Voltage at $V_{tg} = -0.28$ V for n-Graphene channel G^4 -FET and GAA MOSFET.

Fig. 8 shows the comparison of the drain current at $V_{tg} = -0.28$ V for n-Graphene channel G^4 -FET and GAA MOSFET. Drain current of n-Graphene channel rectangular GAA MOSFET is larger than other two structures.

Fig. 9 shows the drain current at $V_{tg} = -0.28$ V for n-Silicon channel G^4 -FET which is smaller than n-Graphene channel G^4 -FET and GAA MOSFET (Table II).

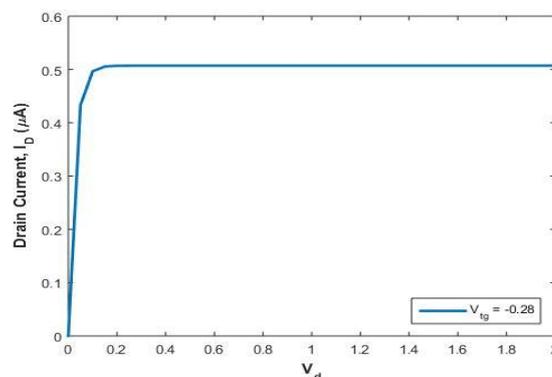


Fig. 9. drain current vs Drain Voltage at $V_{tg} = -0.28$ V for n-Silicon channel G^4 -FET

Table II Comparison Of Drain Current Between G^4 -Fet And Gaa Mosfet

Properties	n-Silicon channel G^4 -FET	n-Graphene channel G^4 -FET	n-Graphene channel rectangular GAA MOSFET	n-Graphene channel cylindrical GAA MOSFET
Maximum Drain Current	0.5 μ A	596 μ A	2560 μ A	1960 μ A

CONCLUSION

The potential distribution and Wave function distribution for n-Graphene channel G⁴-FET and GAA MOSFET have been obtained by solving 2-D Poisson-Schrödinger equation using COMSOL with MATLAB. The maximum potential of G⁴-FET and GAA MOSFET has been compared. Conduction band profile and carrier density has been investigated. Drain current of n-Graphene channel G⁴-FET and GAA MOSFET has been calculated and compared with n-Silicon channel G⁴-FET. In the future, transconductance, threshold voltage, Sub-threshold Swing (SS), Drain Induced Barrier Lowering (DIBL), on-off current ratio will be calculated for those structures.

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