IJIREEICE

ISSN (Online) 2321-2004
ISSN (Print) 2321- 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering
ISO 3297:2007 Certified
Vol. 6, Issue 6, June 2018

Thirty Seven Level Inverter with Low THD and Less Number Of Power Switches

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Abstract*:*In this paper, simulation of single-phase 5-level, 17-level, 37-level and three-phase37-level asymmetric inverters with reduced number of power switches and total harmonic distortion is carried out. The topology of single phase 17-level and single phase 37-level inverters are obtained by cascading connection of basic unit of single phase 5-level inverter topology twice and thrice respectively. Using single phase 37-level asymmetric inverters, threephase 37-level inverter is developed. This is achieved by connecting three single-phase inverter bridges with 120° phase difference between each inverter bridges in cascade. This phase difference is achieved by generating pulses with a delay of 120° with respect to each bridge. Pulse generation technique used is based on, comparison between amplitude of sine wave and range of numbers. Simulation of single-phase 5-level, 17-level, 37-level, and three-phase 37-level inverters is carried out using the above mentioned pulse generation technique. The simulation is carried out by using MATLAB\Simulink R2015a software. Results include output voltage, and current waveforms and THD for single phase 37-level inverter. Also shown phase voltage, line voltage, phase and line current waveforms and THD for three-phase 37-level inverter.

Keywords: Asymmetric, Multilevel Inverter (MLI), Total Harmonic Distortion(THD), Pulse Generation Technique.

I. INTRODUCTION

Now-a-days DC/AC power electronic converters, generally known as inverters are being used widely in domestic and industrial applications. This is due to the fact that they consume less energy and have improved system efficiency and quality. Recent advancements in the power electronic technology have introduced multilevel inverters. These inverters acts as an alternative in applications such as conveyors, compressors, mills, fans, pumps etc. Different topologies have been proposed to achieve high output power rating, reduced voltage stress on the individual switching devices, reduced number of sources required, reduced total harmonic distortions and improved output power quality.To achieve the above mentioned parameters, a new general topology of multilevel inverter (MLI) has been proposed in which switching power devices, DC voltage sources used are less in number to obtain higher output levels with reduced total harmonic distortions.Recently, diverse topologies of symmetric cascaded multilevel inverter with different types of pulse generation techniques have been proposed. The advantage of these symmetric type topologies is the requirement of DC voltage sources of same magnitude. Disadvantage is the requirement of more number of switching power devices such as MOSFET or IGBT switches and more number of sources. Different topologies of asymmetric multilevel inverter have also been proposed. These structures have disadvantages such as, requirement of more number of power switches, increased size and increased space requirement and thus increase in cost of the inverter. With different switching pulse generation technique, a new topology of multilevel inverter has been proposed. In this topology, the required number of power switches is less with requirement of different magnitude or amplitude dc voltage sources.

II. BASICS OF MULTILEVEL INVERTER

The multilevel inverter concept introduced since 1975, is best suitable for the medium voltage and high power applications. The inverters employed in applications such as HVDC systems, FACTS systems, high voltage AC drives, must possess the ability to operate at high voltage and high power. To accomplish this, the two-level inverters need to be connected in series arrangement to enable it to operate at high voltages. One main disadvantage of this arrangement is that, the unequal distribution of voltage across series connected switching power devices.The multilevel inverters have overcome such disadvantages. The first topology proposed was cascaded multi-level inverter. This structure consists of full-bridge inverter configurations connected in series with separate DC sources in each bridge to produce stepped or multileveled AC output voltage.

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As the steps or levels in the output voltage increases, quality of the output gets improved as it becomes more sinusoidal in nature and thus it reduces the need of filters at the output to filter harmonics present in the output voltage and current. The Multi-Level Inverter (MLI) circuits consist of many DC voltage sources at the input side and the levels in the output voltage are derived from these DC voltage sources. Depending upon the magnitude of DC voltage sources employed at the input of inverters, multilevel inverters are classified as,

Symmetric MLI :The magnitude of all the DC voltage sources used in these inverters are equal or exactly the same magnitude.

Asymmetric MLI :The magnitude of the DC voltage sources used in these inverters are unequal or different from one another.

The major advantage of asymmetric MLI over symmetric MLI is that, when compared to symmetric MLI, asymmetric MLI is able to generate more number of output levels in output voltage by using reduced switching power devices and DC voltage sources, driver circuits. Thus the installation space required and the total cost of the inverter decreases in asymmetric MLI.The three level output voltage is the smallest level in the output voltage of MLI. If bi-directional switches are used in MLI, then it can be operated in both rectifier and inverter mode depending upon the requirement. As the levels in the output increases towards infinity, the total harmonic distortion of the output reduces towards zero.

The MLIs are majorly classified in to three types as mentioned below,

1. Diode clamped MLI
2. Flying capacitors MLI
3. Cascaded MLI

III.NEW TOPOLOGY OF MULTILEVEL INVERTER

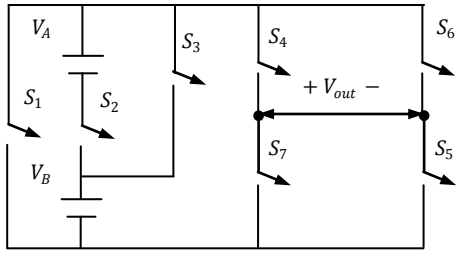

Fig.1 Basic topology of 5 level inverter

Table I Switching states of 5 level inverter

State	Switches states							Vout
	S 1	S 2	S 3	S 4	S 5	S 6	S 7	
1	1	0	0	1	1	0	0	0
2	0	1	0	1	1	0	0	V_A
3	0	0	1	1	1	0	0	$V_A + V_B$
4	0	1	0	0	0	1	1	$-V_A$
5	0	0	1	0	0	1	1	$-V_A-V_B$

The topology of basic unit of 5-level inverter shown in Fig. 1.This basic unit comprises of three power switches and two DC voltage sources. The power switches are specified as S_1, S_2, and S_3. The DC voltage sources are specified as V_A and V_B. Renewable voltage sources like photovoltaic cells, fuel cells etc., can be used as isolated DC sources. Switches (S_1, S_2), (S_1, S_3) and (S_2, S_3) should not be turned on at the same time in order to avoid short circuit of DC voltage sources. An H-bridge comprising of switches S_4, S_5, S_6 and S_7 is used to get both positive and negative output levels. Table I shows the switching scheme.

In order to get 5-levels in the output voltage, switches in the inverter must be operated as per the switching states mentioned in Table I.

'ON' and 'OFF' positions of power switches are represented by '0' and '1' respectively.To get zero level in the output, switch S_1 must be in 'ON' position and switches S_2 and S_3 must be in 'OFF' position and either $S_4$and S_5 or S_6 and S_7 must be in 'ON' position. To get remaining levels switches should be operated as shown in TableI.
In general, for the topology shown in Fig.1
The Output Voltage, $\boldsymbol{V_{out}(t) = \sum_{i=1}^{n} = Vout(i)}$
Number of power switches required, $\mathbf{N_s = 3n + 4}$
Number of input DC voltage sources required, $\mathbf{N_{vs} = 2n}$
Magnitude of input DC voltage sources, $\mathbf{V_{nA} = V_{nB} = (2n\text{-}1)\ V_{dc}}$
Maximum number of voltage levels at the output of inverter, $\mathbf{N_{level} = 4\ x\ (\sum_{i=1}^{n} = 2i - 1) + 1}$
Highest Voltage level at the output of inverter, $\mathbf{V_{out,max} = 2x\ (\sum_{i=1}^{n} = V_{iA})}$
Where 'n' is the number of basic units connected in cascade.

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Vol. 6, Issue 6, June 2018

A. Single Phase 37 Level Inverter

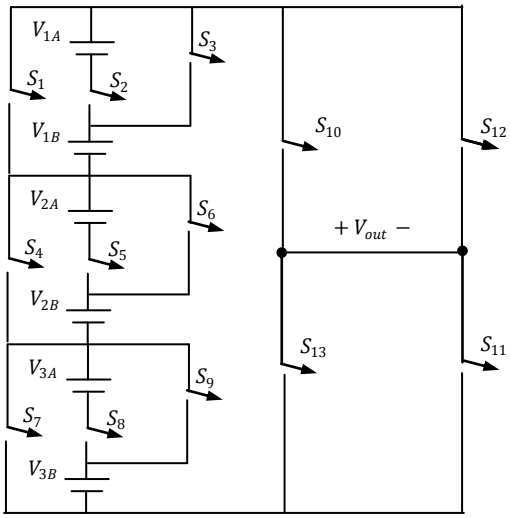

Fig.2 Single phase 37 level inverter

Figure.2 shows the topology of single phase 37-level inverter. Three numbers of basic units are connected in cascade as shown in Fig.2 to obtain 37 level inverter.

Table II Switching states of 37 level inverter

State	Switches States													V_{out}
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	
1	1	0	0	1	0	0	1	0	0	1	1	0	0	0
2	0	0	1	1	0	0	1	0	0	1	1	0	0	V_{1B}
3	0	1	0	1	0	0	1	0	0	1	1	0	0	$V_{1A} + V_{1B}$
4	1	0	0	0	0	1	1	0	0	1	1	0	0	V_{2B}
5	0	0	1	0	0	1	1	0	0	1	1	0	0	$V_{1B} + V_{2B}$
6	0	1	0	0	0	1	1	0	0	1	1	0	0	$V_{1A} + V_{1B} + V_{2B}$
7	1	0	0	0	1	0	1	0	0	1	1	0	0	$V_{2A} + V_{2B}$
8	0	1	0	1	0	0	0	0	1	1	1	0	0	$V_{1A} + V_{1B} + V_{3B}$
9	0	1	0	0	1	0	1	0	0	1	1	0	0	$V_{1A} + V_{1B} + V_{2A} + V_{2B}$
10	0	0	1	0	0	1	0	0	1	1	1	0	0	$V_{1B} + V_{2B} + V_{3B}$
11	1	0	0	1	0	0	0	1	0	1	1	0	0	$V_{3A} + V_{3B}$
12	0	0	1	1	0	0	0	1	0	1	1	0	0	$V_{1A} + V_{3A} + V_{3B}$
13	0	1	0	1	0	0	0	1	0	1	1	0	0	$V_{1A} + V_{1B} + V_{3A} + V_{3B}$
14	1	0	0	0	0	1	0	1	0	1	1	0	0	$V_{2B} + V_{3A} + V_{3B}$
15	0	0	1	0	0	1	0	1	0	1	1	0	0	$V_{1B} + V_{2B} + V_{3A} + V_{3B}$
16	0	1	0	0	0	1	0	1	0	1	1	0	0	$V_{1A} + V_{1B} + V_{2B} + V_{3A} + V_{3B}$
17	1	0	0	0	1	0	0	1	0	1	1	0	0	$V_{2A} + V_{2B} + V_{3A} + V_{3B}$
18	0	0	1	0	1	0	0	1	0	1	1	0	0	$V_{1B} + V_{2A} + V_{2B} + V_{3A} + V_{3B}$
19	0	1	0	0	1	0	0	1	0	1	1	0	0	$V_{1A} + V_{1B} + V_{2A} + V_{2B} + V_{3A} + V_{3B}$

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The switching scheme for switches S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8, S_9, S_{10}, S_{11}, S_{12} and S_{13} is as shown in TableII.The switches S_{10} and S_{11} are turned on and switches S_{12} and $S_{13}$are turned off simultaneously to generate positive output levels and the switches S_{12} and S_{13} are turned on and the switches S_{10} and $S_{11}$are turned off simultaneously to generate negative output voltage levels. In order to get 37-levels in the output voltage, switches in the inverter must be operated as per the switching states mentioned in TableII

'ON'and 'OFF' positions of power switches are represented by '0' and '1' respectively.

To get zero level in the output, switches S_1, S_4 and S_7 must be in 'ON' position and switches S_2, S_3, S_5, S_6, S_8 and S_9 must be in 'OFF' position and either S_{10}&S_{11} or S_{12}&S_{13} must be in 'ON' position.

To get 1st level in the output, switches S_3, S_4 &S_7 must be in 'ON' position and switches S_1, S_2, S_5, S_6, S_8 and S_9 must be in 'OFF' position. Positive 2nd level is obtained when S_{10}&S_{11} are in 'ON' position and S_{12}&S_{13} are in 'OFF' position and Negative 2nd level is obtained when S_{12}&S_{13} are in 'ON' position and S_{10}&S_{11} are in 'OFF' position.

Similarly, remaining levels in the output voltage can be obtained by switching the power switches in a sequence mentioned in TableII.

To avoid short circuit of voltage sources, simultaneous switching of the power switches in the same unit must be eluded.

IV. PULSE GENERATION TECHNIQUE

A. Pulse Generation for 5-level Inverter: Comparison between amplitude of sine wave and range of numbers

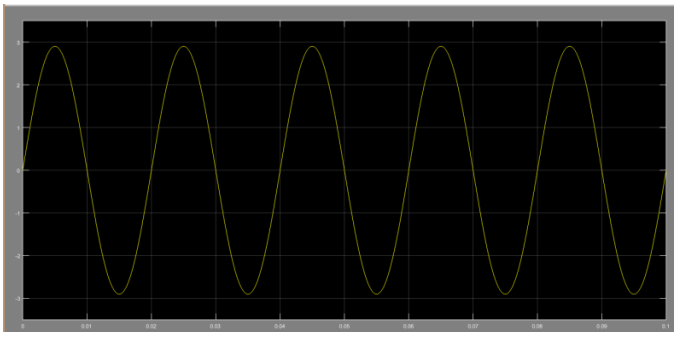

Fig 3: Comparison between amplitude of sine wave and rangeof numbers

In this method, sine wave of amplitude 2.9 and frequency 50 Hz is selected and it is compared with range of numbers. For 5-level inverter, '3' ranges of numbers with step of '1'i.e., (0 to 1), (1 to 2) and (2 to 3) are chosen. The relational operators such as '≥', '>', '<' and '≤' are used to compare inputs (amplitude of sine wave and range of numbers). For instance, if the amplitude of sine wave is compared with range of numbers between (0 and 1), then pulse is generated for that range and given to power switches. Similarly, amplitude of sine wave is compared with range of numbers between (1 and 2) and between (2 and 3) and the generated pulses are given to power switches to generate particular output voltage levels.

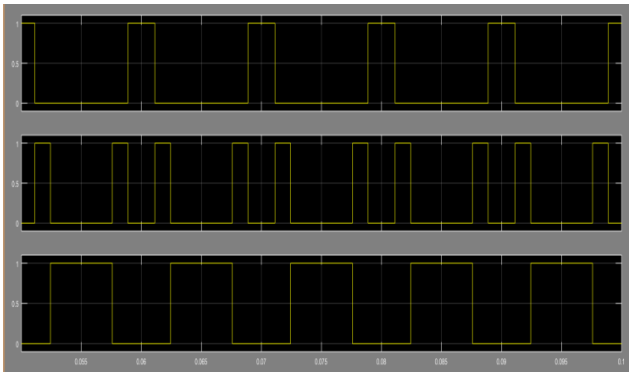

Fig.4 : Switching pulse pattern of switches S_1, S_2, S_3

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Similarly pulses for 37 level inverter are obtained as shown below

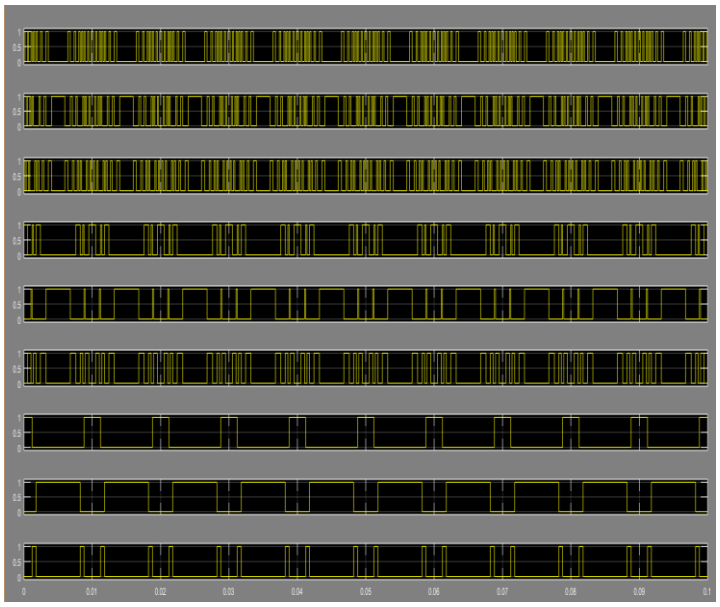

Fig 5: Switching pulse pattern of switches S_1, S_2, S_3, S_4, S_5, S_6, S_7, $S_8$and S_9

V. THREE PHASE 37 LEVEL INVERTER

The three phase 37-level inverter is developed by using existing topology of single-phase 37-level inverter. This is achieved by slight modification in pulse generation technique over three numbers of single phase inverters connected in cascade as shown in Fig.6. To realize this modification, three numbers of single-phase inverters are required and pulses with 120° phase delay between each pulse generator are generated. The pulses so generated are given to three numbers of single-phase inverters connected in cascade, which gives the three phase output voltages and currents with 120° phase difference.

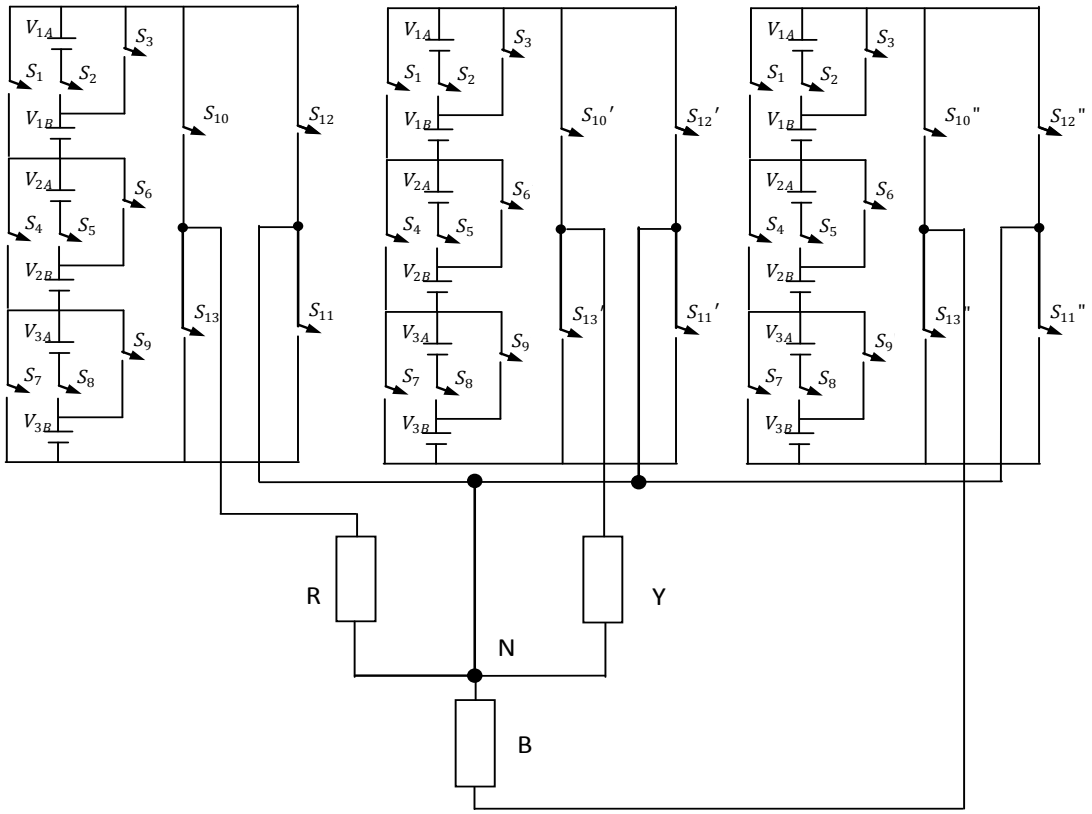

Fig.6: Three phase 37-level inverter

IJIREEICE

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VI. SIMULATION AND RESULTS

A. Single-phase 37-level inverter:

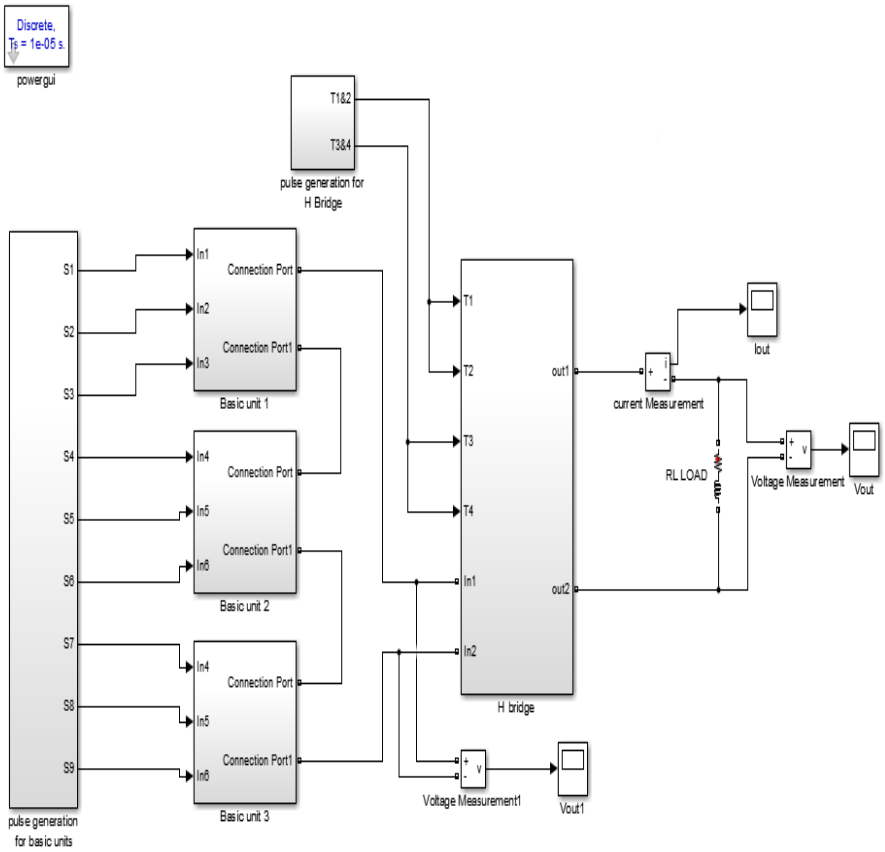

Fig.7: Simulink model of single phase 37-level inverter

he topology of single phase 37-level inverter shown in Fig.2 is simulated in MATLAB\Simulink R2015a. Simulink model of the same is shown in Fig.7. IGBTs are used as power switches. DC voltage sources of magnitude V_{1A} = 10V, V_{1B} =10V, V_{2A} = 30V, V_{2B} = 30V, and V_{3A} = 50V, V_{3B} = 50V, are used at input side and R-L load with R=50 ohm, L=30mH is used at the output side. A subsystem is created for pulse generation block, in which 'Goto' and 'From' blocks are used for transfer of signal generated to the power switches.

B. Three-phase 37-level inverter:

The topology of three phase 37-level inverter shown in Fig.6 is simulated in MATLAB\Simulink R2015a. It is similar to the concept described in the section VI A. The Simulink model of the three phase 37-level inverter is shown in Fig.8. Here three such Single phase 37-level inverters and three phase star connected R-L load is used. Three pulse generators with 120° delay between each other is employed in this case.

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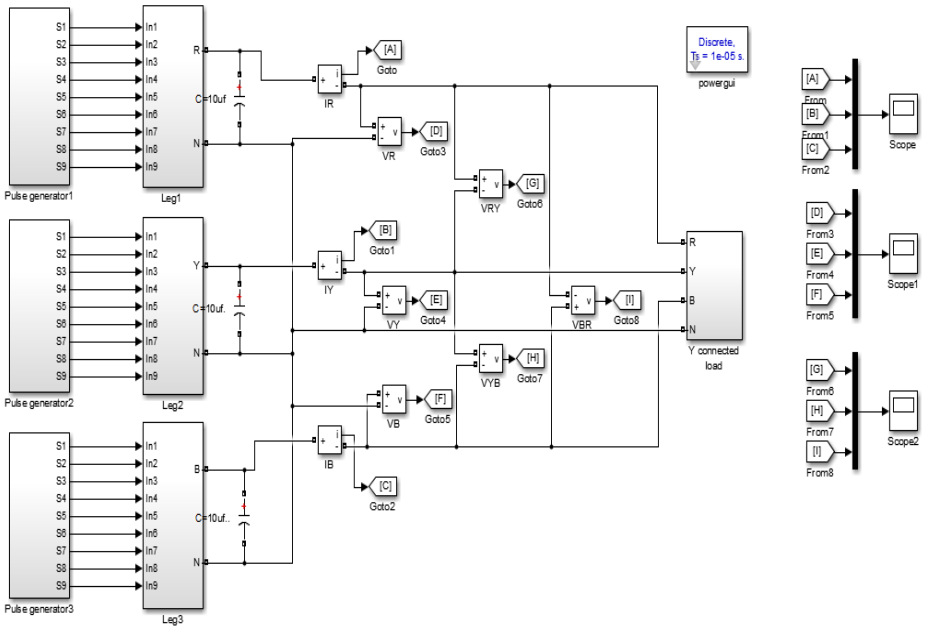

Fig 8 : Simulink model of the three phase 37-level inverter

C. Three-phase 37-level inverter simulation results

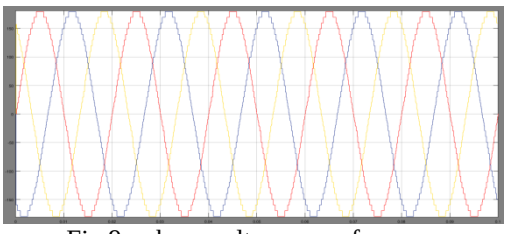

Fig.9 : phase voltage waveforms

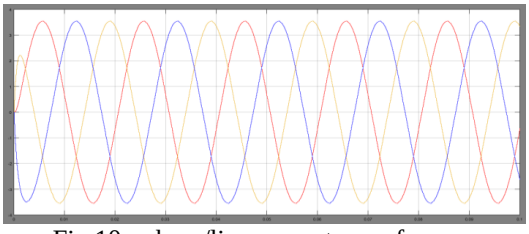

Fig.10 : phase/line current waveforms

D. THD analysis of three phase 37-level inverter

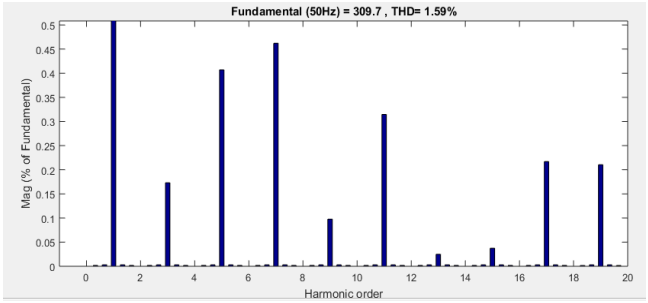

Fig.11 : THD analysis of line voltage

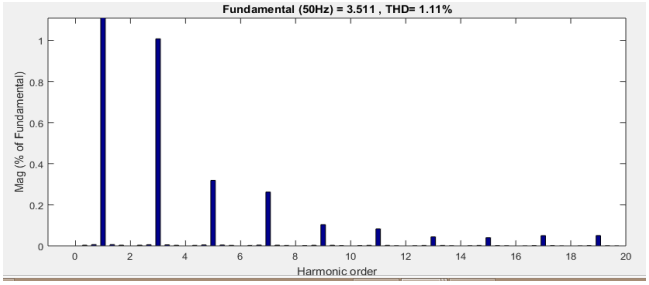

Fig.12 : THD analysis of line/phase current

IJIREEICE

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Table III Comparison between different types of MLI with respect to number of power switches required.				
	Number of Power Switches required			
Type of MLI	DCMLI	FCMLI	CHBMLI	New topology of MLI
	2(N-1)	2(N-1)	2(N-1)	3N+4
	N – number of output levels			N – number of basic units
Single phase, 5-level inverter	8	8	8	7
Single phase, 17-level inverter	32	32	32	10
Single phase, 37-level inverter	72	72	72	13
Three-phase, 37-level inverter	216	216	216	39

Table IV Comparison of THD between the present and other topologies of multilevel inverter						
Sl. No.	Present Topology	THD %	switches required	Topology in Ref. Paper [2]	THD %	switches required
1	1-φ 5-level inverter	10.72	7	1-φ 7-level inverter	17.67	8
2	1-φ 17-level inverter	3.88	10	1-φ 9-level inverter	14.99	10
3	1-φ 37-level inverter	3.64	13	1-φ 11-level inverter	7.11	12

❖ Based on above comparison it is concluded that the present topology is better topology than the one mentioned in ref. paper [2] as the number of power switches required is less and also THD is also very less.

V. CONCLUSION

This paper presented the simulation of single-phase 5-level, 17-level, 37-level and three-phase 37-level asymmetric inverters with reduced number of power switches and total harmonic distortion. Using single-phase 37-level asymmetric inverters, three-phase 37-level inverter is developed. Pulse generation technique used is based on, comparison between amplitude of sine wave and range of numbers. Simulation of single-phase 5-level, 17-level, 37-level, and three-phase 37-level inverters is carried out in MATLAB\Simulink R2015a software. Results include output voltage, current waveforms and THD for single-phase5-level, 17-level and 37-level inverter and also three-phase 37-level inverter.

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