

Analysis of Multi-Level Inverter For 7-Level Architecture using MATLAB Simulink

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Abstract: This thesis describes the detailed study of Multi-level Inverters for 5-level and 7-level Multi-level inverters and an improvement is seen in 7-level harmonic distortion by a significant amount. Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. The THD in 7 –level is about 28%.

Keywords: MLI, Cascaded, THD, 5-level, 7-level

1. INTRODUCTION

The idea of multilevel converters has been presented since 1975. The term multilevel started with the three-level converter. In this manner, a few multilevel converter topologies have been produced. Be that as it may, the rudimentary idea of a multilevel converter to accomplish higher power is to utilize a progression of power semiconductor switches with a few lower voltage dc sources to play out the power change by combining a staircase voltage waveform. Capacitors, batteries, and sustainable power source voltage sources can be utilized as the multiple DC voltage sources. The replacement of the power switches aggregate these multiple DC sources with a specific end goal to accomplish high voltage at the yield; be that as it may, the appraised voltage of the power semiconductor switches depends just upon the rating of the dc voltage sources to which they are associated.

2. SIMULATION RESULTS

In this chapter, Implementation and results are presented. The model for 5 level Multi-level Inverter is shown in Figure 1. It is a cascaded type of multi-level inverter using MOSFET.

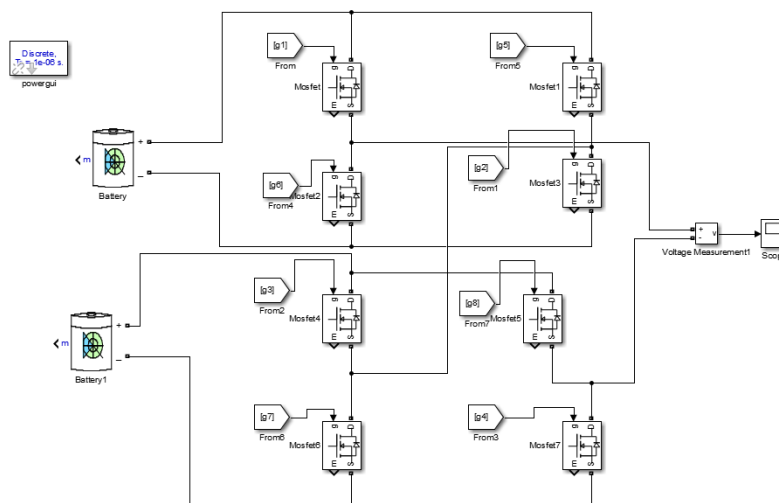


Figure 1: Multi-level Inverter for 5 –level

For controlling of the switches techniques used is based on Sinusoidal Pulse width modulation which is generally known as SPWM. The control diagram is given in Figure 2.

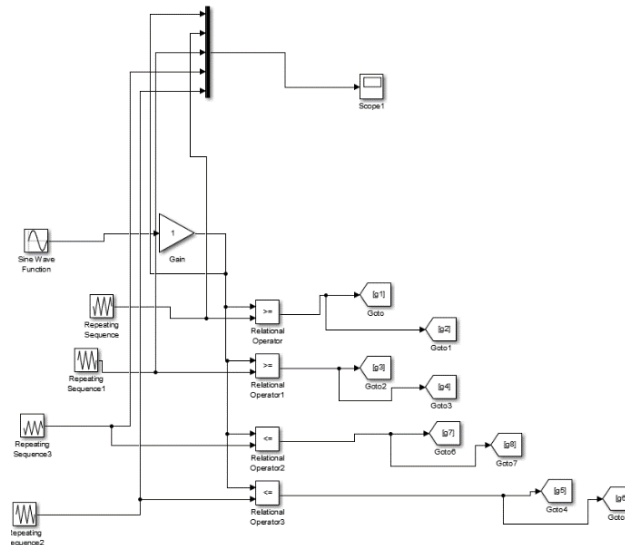


Figure 2: Controlling of Converter 5 level

Figure 3 shows the output waveform, and figure 5 shows the waveform for FFT analysis of the same and Figure 4.6 shows the FFT analysis.

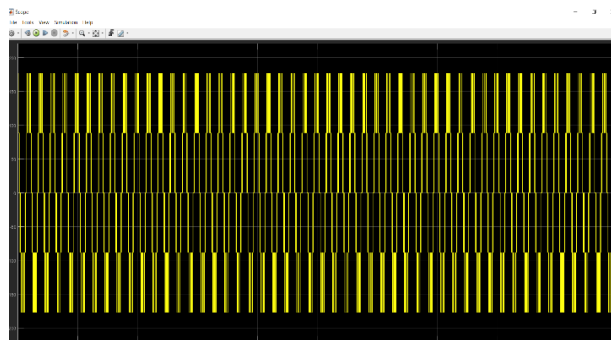


Figure 4: Waveform output

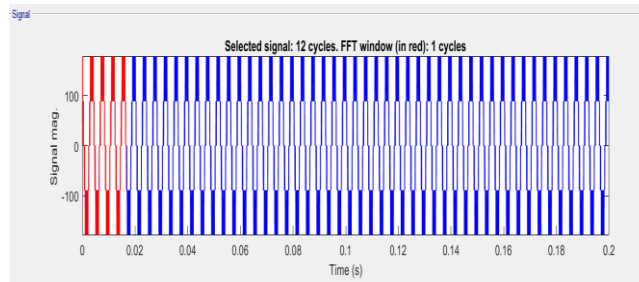


Figure 5: Waveform output for FFT analysis

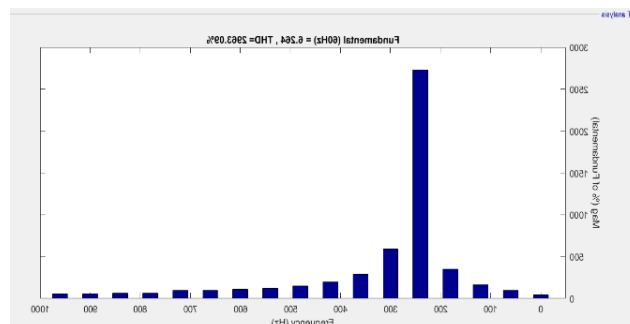


Figure 6: FFT analysis of 5 level

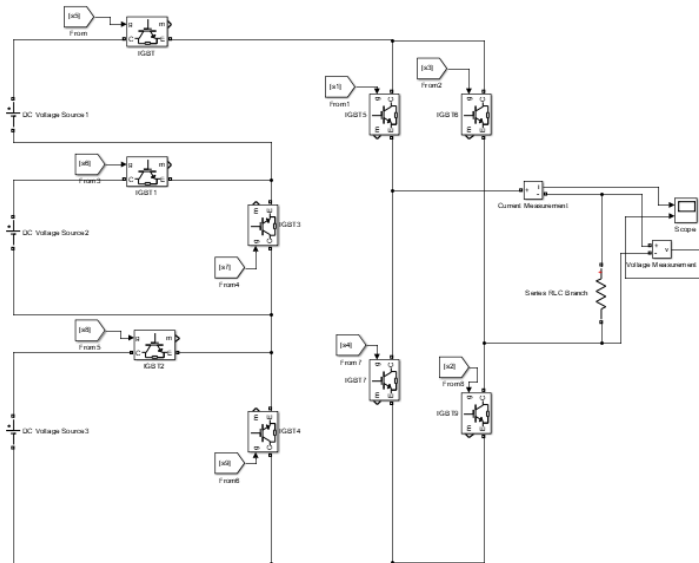


Figure 7: Proposed Model for 7 -level

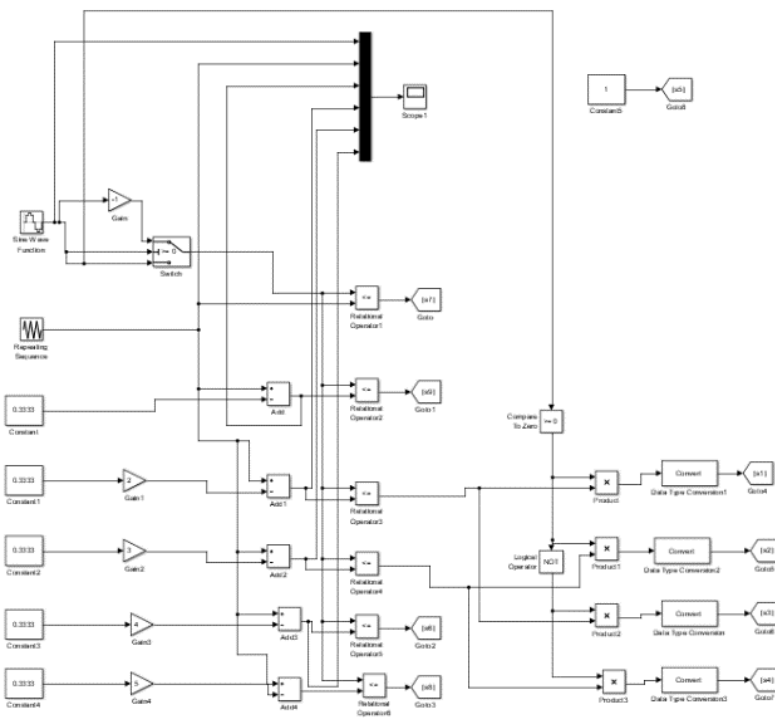


Figure 8: Control Strategy for proposed model

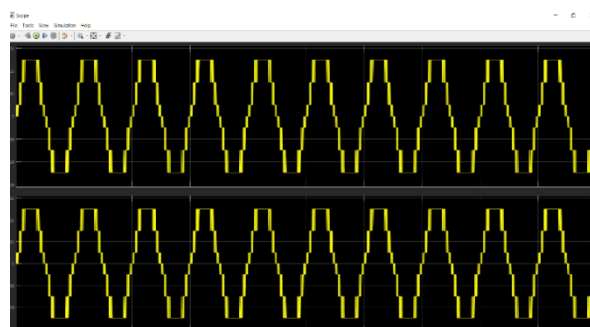


Figure 9: Waveform output of proposed 7-level

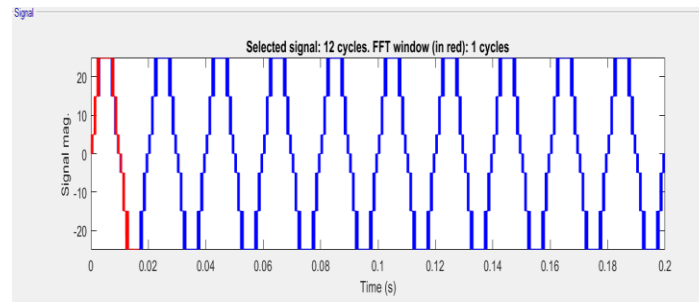


Figure 10: Waveform output for FFT Analysis proposed 7-level

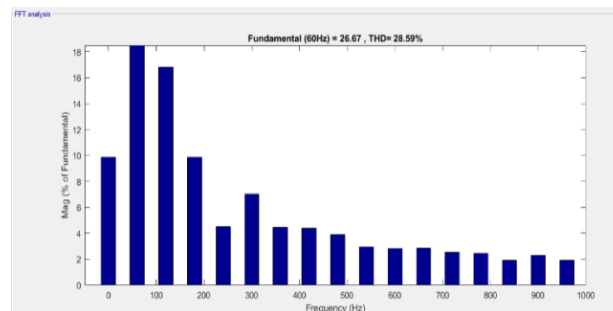


Figure 11: FFT Analysis of Proposed 7-level

3. CONCLUSION

This paper has provided a brief summary of multilevel inverter circuit topologies (5-level and 7-level) and their analysis. It is seen that in 7-level inverter THD is minimum when compared to the base paper results as shown in Figure 12. The THD of 7-level inverter is 28.59%.

M.I	Proposed CO-APOD	
	THD%	Voltage
1.0	31.76	189.60
0.9	32.76	180.30
0.8	35.58	164.60
0.7	40.64	141.40

Figure 12: comparison to base results[1]

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