IJIREEICE

ISSN (Online) 2321-2004
ISSN (Print) 2321- 5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

NFTPCOS-18

National Conference on Future Technologies in Power Control and Communication Systems

College of Engineering Perumon, Kollam, Kerala

Vol. 1, Special Issue 2, March 2018

Power Quality Improvement in Bridgeless Canonical Switching Cell Converter fed Switched Reluctance Motor Drive

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Abstract: A Switched Reluctance Motor (SRM) drive has wide benefits such as high torque-volume ratio, low manufacturing cost, high dynamic response and wide speed range is required. Many industrial and home appliances have devices of power automatic recycled as a rectifier and driver along with motors. The use of these devices have several non-linearity in the electrical system. Some problems are high harmonics, low power factor, reduced performance and increased consumer cost has produced as a result of non-linearity. In a conventional switched reluctance motor drive, the AC mains power factor is low and the overall Total Harmonic Distortion (THD) rises as a result of harmonics. In instruction to diminish the THD and progress the power factor of the supply mains of SRM, a Bridgeless canonical switching cell (CSC) converter configuration is working in Discontinuous inductor current mode and it is recycled to control the yield voltage of DC and to enhance the power factor at the supply mains. Furthermore, it controls the voltage of DC-link and to find the speed controller of motor side. Here, the SRM with diode bridge rectifier (DBR) and also, with and without converter is analysed. The THD and power factor of the above systems was analysed. The power quality directories are obtained in the array of International power quality principles like IEC 61000-3-2. The drive performance is evaluated by using MATLAB/SIMULINK software.

Keywords: Switched reluctance motor (SRM) drive; Power quality; Bridgeless Canonical switching cell (CSC) converter; Mid-point converter; Discontinuous inductor current mode (DICM); THD.

I. INTRODUCTION

Cost and efficiency are two most important aspects which shows a crucial role in the plan and progress of low power motor drives targeting towards households uses such as water pumps, vacuum cleaner, fan, washing machine etc. SRM (Switched Reluctance Motor) has salient pole construction such that stator is provided with concentrated windings, which are excited with the help of mid-point converter [1]. The rotor is constructed by laminated magnetic materials or permanent magnet and free from any sort of winding. SRM become visible as a top selection of household applications owing to its robustness and mechanical simplicity [2-3].

Power quality improvement is individual of the essential requirement in today's world. The given typical standard of IEC 61000-3- 2 on power quality [4], recommends high power factor (PF) and little total harmonics distortion (THD) on the AC supply. The predictable system of SRM drive nourished by a diode bridge rectifier (DBR) draws a non-sinusoidal current from the AC supply, which grades in high current THD of the order of 70% to 80% in mains side. Thus power quality converters are highly recommended to obtain high power factor (PF) and to reduce THD. These single stage converters have increased attention due to enhanced power quality at the AC supply and to control the DC bus voltage.

This paper displays the control and plan of SRM drive with front end of PFC converter [5]. By using the converter, a noble motor driving presentation is obtained. The proposed bridgeless configuration develops one extra inductor both for output side and input side which add disadvantage in respect to cost and size. But, on other side the developed current performance is achieved. Another advantage of proposed configuration is that present pressure of power switches are decreased to half as each switch is conducting for half cycle.

In the proposed SRM drive, wide array of speed regulator is obtained under wide variation in supply voltages at the equal period cultivating the power quality at the AC with low harmonic distortion in the mains current and high power factor. The buck-boost converter has recycled but it draws the current from the AC supply in way such that it results in power factor correction. In the proposed SRM drive, the plan of a mid-point converter is used to nourish the SRM. A

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mid-point converter is a small cost converter which contain only one IGBT (Insulated-gate bipolar transistor) switch and one diode are recycled for feeding each phase of converter side. The SRM speed drive is organised by a variable voltage of DC link, at the equivalent interval SRM appears as viable alternative to AC machines since of its simple design which marks in reduction of cost in the machine for the different rating and has advantage of mass invention [6]. Many arrangement of bridgeless converters are defined in the literature survey, each having their own peculiar characteristics. A bridgeless buck and a bridgeless boost converters have an incomplete voltage translation ratio (< 1 for buck and > 1 for boost) and it cannot be used for an extensive variability of voltage regulator. To overwhelm this topic, a bridgeless buck–boost converter has stayed proposed, but it has extraordinary switching losses matching to three switches. A double-switch bridgeless buck–boost PFC converter is proposed, which has low losses associated. Advanced order PFC bridgeless SEPIC [13], Zeta and Cuk converters have broadly used but it have a great number of machineries. On other hand, no attention have rewarded to the canonical switching cell (CSC) converter, while it has outstanding routine as a power factor pre regulator, a slight element count (compared to the non-isolated Cuk converter[10]), and upright light load instruction. Fig. 1 displays the conservative PFC created CSC converter. In this, a mixture of switch (Sw), and diode (D) and capacitor (C1) is known as a 'canonical switching cell,' and this lockup, mutual with an inductor (Li) and a dc link capacitor (Cd), is identified as CSC converter. With correct selection and strategy of factors, this grouping is used to accomplish PFC operation once nourished by a single phase ac mains over DBR and a DC filter. This effort goals at the growth of a bridgeless configuration of CSC converter, which shows the incomplete removal of DBR at front end converter for falling the conduction losses related with it.

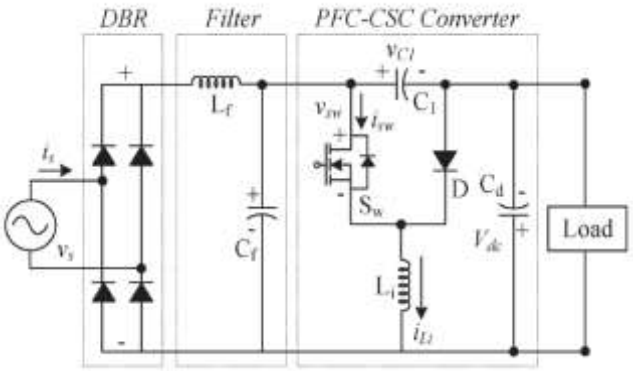

Fig. 1 Conventional PFC-based CSC converter

II. PFC BL-CSC CONVERTER –FED SRM DRIVE

Fig. 2 shows the planned block diagram BL-CSC-converter-based SRM drive. As revealed in this representation, the DBR is eradicated in this BL-CSC converter, so it plummeting the switching losses related with it. This BL-CSC converter nourished SRM drive is intended to run in a discontinuous inductor current mode (DICM) so that the current is curving through the inductors L_{i1} and L_{i2} are irregular, where the voltage transversely the intermediate capacitors C_1 and C_2 ruins continuous in a switching period. An approach of a variable dc link voltage for regulatory the speed of SRM is used. The procedure, plan, and controller of this BL-CSC converter fed SRM drive are described in the following chapters. Presentation of the future drive is confirmed with test outcomes gained on an advanced prototype with better power quality at the ac mains for a wide range of speed and voltage.

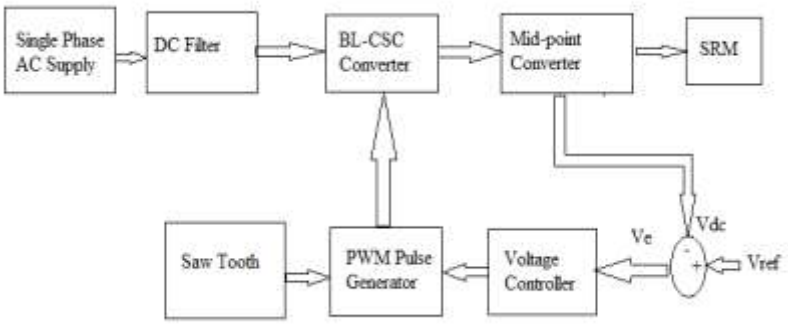

Fig. 2. Block Diagram of Proposed Bridgeless CSC Converter fed SRM drive

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A short-term judgment of the anticipated formation with the present bridgeless converter configurations is tabulated in Table I. It displays that the entire quantity of components (Switch— Sw, Diode—D, Inductor—L, and Capacitor—C) and the modules conducting throughout each half-cycle of supply voltage. The bridgeless buck and boost converter conformations are not apt for the required application due to condition of high voltage conversion ratio (i.e., voltage bucking and boosting) for regulatory the wide range of speed.

Table i. Comparative analysis of the proposed bl-csc converter with existing configurations

Configuration	**No of the Devices**					**½ Period**
	S_W	D	L	C	Tot	
BL-BUCK BOOST	3	4	1	3	11	8
BL-Cuk	2	4	4	3	13	7
BL-Sepic	2	3	2	2	9	7
BL-Zeta	2	4	4	3	13	7
Proposed BL-CSC	2	4	2	3	11	6

As associated with the various bridgeless configuration of Cuk, SEPIC and Zeta converters, the proposed BL-CSC converter have moderately lower number of machineries and least number of conducting procedures throughout each half-cycle of the supply voltage, anywhere the future configuration shows the lowest conduction losses due to the transmission of minimum number of modules during each half line cycle.

III. WORKING PRINCIPLE OF THE PFC BL-CSC CONVERTER

The procedure of the BL-CSC converter is categorised into two important categories.

A. Process in Positive and Negative Half Cycles of Supply

This bridgeless converter is intended between the two switches work for positive and negative half-cycles of the supply voltage. Fig. 3(a)–(f) shows the process of the proposed BL-CSC converter for positive and negative half-cycles of the voltage of supply accordingly. As revealed in Fig. 3(a)–(c), through the positive half-cycle of the supply voltage, the input current flows through switch S_{w1}, inductor L_{i1}, and a diode D_p. Similarly, switch S_{w2}, inductor L_{i2}, and diode D_n behaves for a negative half-cycle of the voltage of supply, as exposed in Fig. 3(d)–(f). Fig. 4(a) shows the waveforms of mains voltage with inductor currents (i_{Li1} and i_{Li2}) and intermediate capacitor voltages (V_{C1} and V_{C2}) accordingly. The planned converter is operating in DICM, i.e., the inductor currents (i_{Li1} and i_{Li2}) are discontinuous, and the voltages across the intermediate capacitor (V_{C1} and V_{C2}) were continuous with a permissible sum of voltage ripple in a switching period completely.

B. Operation through Complete Switching Period

The anticipated BL-CSC converter is plotted to function in a DICM so that the current in inductors L_{i1} and L_{i2} becomes irregular for a period of switching. Fig. 3(a)–(f) displays dissimilar modes of procedure during the switching period completely for positive and negative half-cycles of the voltage of supply, accordingly. Fig. 4(b) displays the related diagrams of three modes of operations.

- Mode I-A: By the way Fig. 3(a) is shown, when switch S_{w1} is curved on, the response side of inductor L_{i1} charging through diode D_p, and current i_{Li} enhances, where the intermediate capacitor C_1 starts settling through the switch S_{w1} to control the dc link capacitor C_d. So that the voltage of intermediate capacitor V_{C1} declines, where the dc link voltage V_{dc} increases.
- Mode I-B: When switch S_{w1} is off, the energy stowed in the inductor L_{i1} releases to dc link capacitor C_d through the diode D_1, as shown in Fig. 3(b). The current i_{Li} diminishes, where the dc link voltage remains to increase in this operation. Intermediate capacitor C_1 starts charging, and voltage V_{C1} goes high, as shown in Fig. 4(b).
- Mode I-C: This method is the Discontinuous Current Mode (DCM) of process as the current in input inductor L_{i1} is zero, as exposed in Fig. 3(c). The intermediate capacitor C_1 continues to hold energy and retains the charge of capacitor, where the dc link capacitor C_d materials the energy to the load. The similar behaviour of the converter is obtained for the other negative half-cycle of the supply. An inductor L_{i2}, an intermediate capacitor C_2, and diodes D_n and D_2 conducts in a same way, as presented in Fig. 3(d)–(f).

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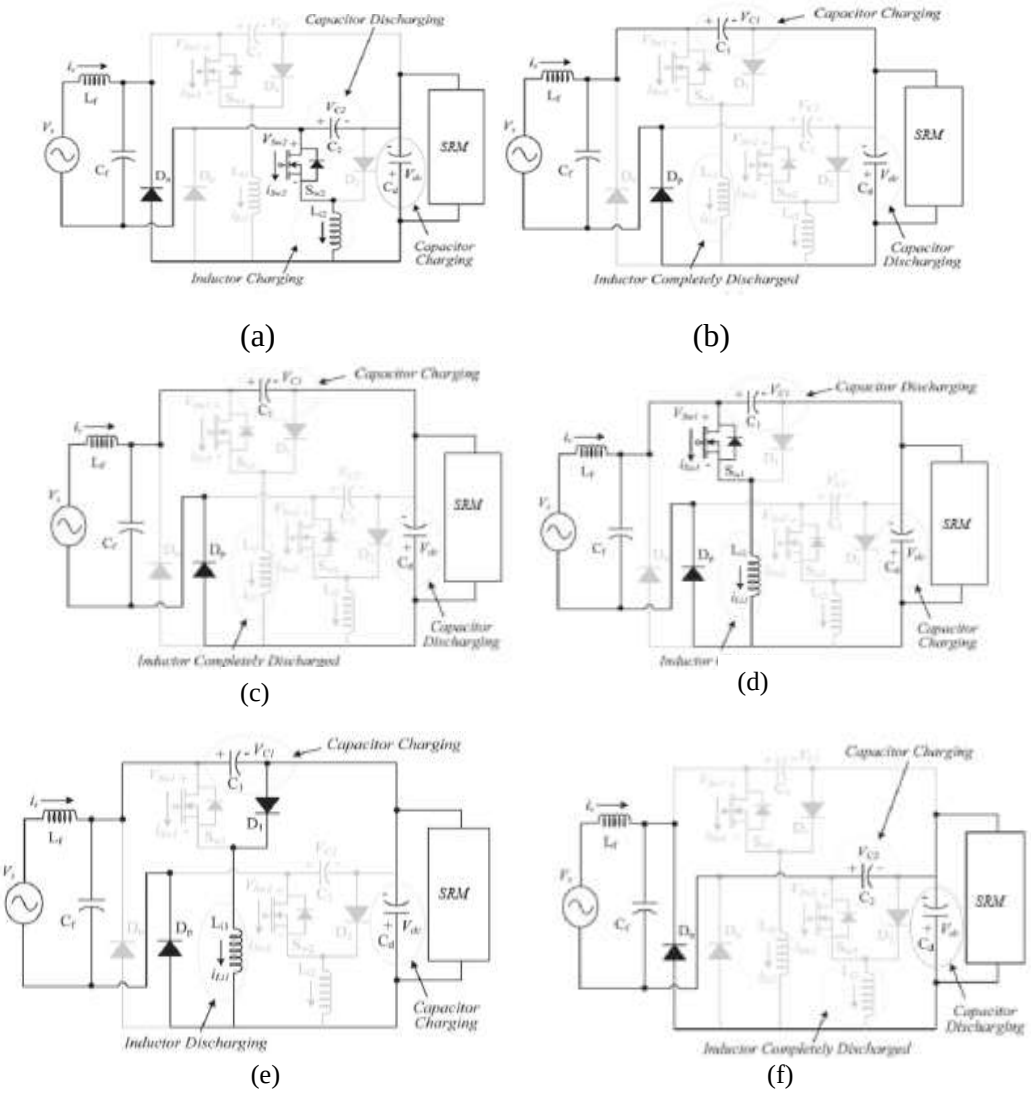

Fig. 3. Different methods of operation of the proposed BL-CSC converter. (a) Mode I-A. (b) Mode I-B. (c) Mode I-C. (d) Mode II-A. (e) Mode II-B. (f) Mode II-C.

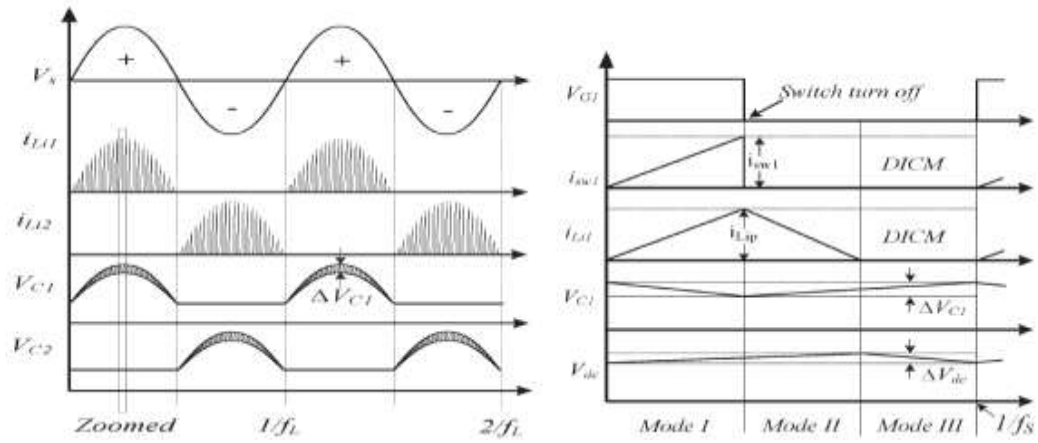

Fig. 4. Waveforms in different styles of operation of the proposed converter

IV.DESIGN OF THE PFC BL-CSC CONVERTER

IJIREEICE
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A SR motor of 750W (Rating of the motor) is fed with front end PFC converter of 850W. Wide range of speed regulator is realized by varying the DC link voltage from low value (v_{dcmin}= 100 V) to regarded value of the DC link voltage (v_{dcmax}= 320 V). The supply voltage (vs) is considered as 170 V to 220 V AC. Table II indicates the calculated the standards of Bridgeless CSC converter [9].
In this, the average input voltage V_{inav}, after an uncontrolled rectifier is given as

$$V_{inavg} = \frac{2Vm}{\Pi} \quad (1)$$

Where, V_m is the peak voltage of the supply.

The duty ratio D is given as,

$$D = \frac{Vdc}{(Vinav+Vdc)} \quad (2)$$

Where, V_{dc} is the output voltage.

Table ii. Calculated values of bridgeless csc converter

Parameters	Expressions	Design Data	Value
Inductor, L	$\frac{V_{in}(t)D(t)}{2I_{in}(t)f_s}$	$\frac{1}{2*20000}(\frac{170^2}{850})(\frac{320}{320+170\sqrt{2}})$	485.35 µH
Capacitor, C	$\frac{V_{dc}D}{\Delta V_{c1}f_sR_L}$	$\frac{850*0.507}{0.5*20000*631.12*120.4}$	566nF
DC-Link Capacitor, C_d	$\frac{P_{min}}{2\omega\delta V_{dcmin}^2}$	$\frac{144.6}{2*314*.05*100^2}$	460.73 µF
LC Filter, C_{max}	$\frac{I_m}{\omega_L V_m}(\tan\theta)$	$\frac{(\frac{850\sqrt{2}}{220})}{314*220\sqrt{2}}\tan(0.5)$	488.09 nF
LC Filter, L_{req}	$\frac{1}{4\Pi^2 f_c^2 C_f}$	$\frac{1}{4*4222.1^2*10^{-9}}9*10^{-3}$	3.91 mH

V. CONTROL OF FRONT-END PFC CONVERTER

The PFC operation and control of speed by fluctuating the converter output voltage is attained by changing the duty ratio (D) of the converter switch at a fixed frequency (fs). The converter voltage is separated into two series capacitors with a mid-point N. The complete control algorithm consists of design of control, selection of sensor for sensing voltage and generation of switching pulses to find the preferred speed control of power factor correction [10].
Two control approaches are used in PFC converter i.e., current multiplier approach and the voltage follower approach. These control outlines select the operation in DICM and CICM respectively [8]. Here an approach of voltage follower is considered with a constant DC voltage (v_{ref}) is taken as reference voltage and it is compared with the voltage of sensed DC link (v_{dc}) to generate error voltage (v_e) at any instant "k" which is given as,

$$V_e(k) = V_{dc}^*(k) - V_{dc}(k) \quad (3)$$

This error voltage act as an input to PI controller which gives the controlled output voltage v_{cdc}

$$V_{cdc}(k) = V_{cdc}(k-1) + k_{pv}\{V_e(k) - V_e(k-1)\} + k_{iv}V_e(k) \quad (4)$$

Where k_{iv} denotes the integral gain and k_{pv} denotes the proportional gain for the PI voltage controller, finally the controller output is allowed to pass over the comparator which compares with saw tooth waveform of high frequency i.e 20000 kHz to generate the converter switching pulses.

VI. SIMULATIONS AND RESULTS

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A. Performance during Steady State

Figure 5 displays that the MATLAB model of Power Factor Correction (PFC) converter and speed mechanism of Switched reluctance motor (SRM) drive using PI controller.

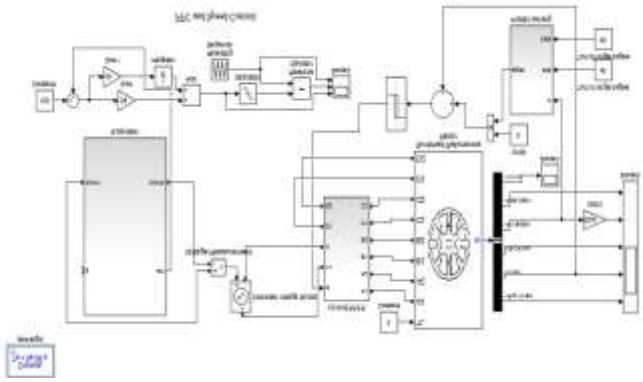

Fig .5. MATLAB/Simulink model of power factor correction converter and speed control of SRM using PI controller

The simulation results of this proposed system such as input current in the AC mains, speed and torque waveforms of SRM are as shown in figures from 6 to 8 respectively. Figure 6 displays the waveform of input current in AC supply which increases up to 2.6 A.

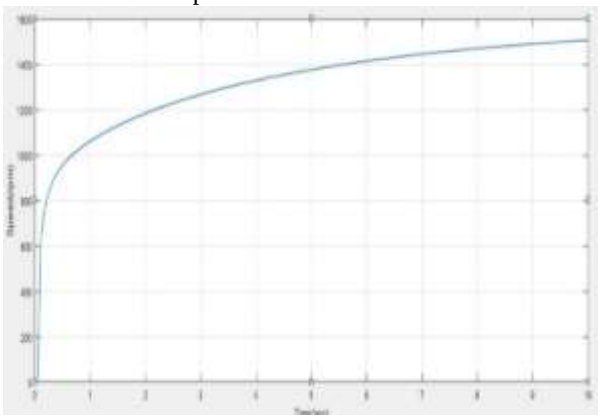

Fig.6. Simulated input current curve in AC mains

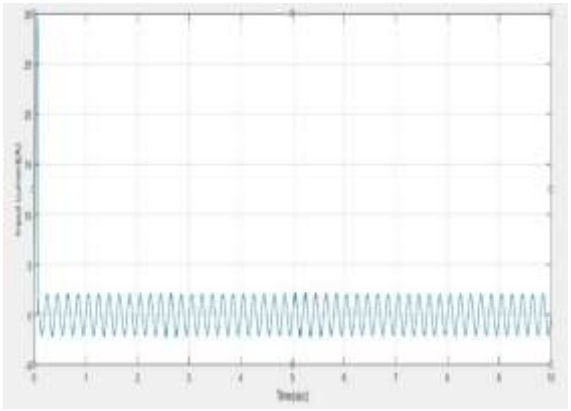

Fig.7. Speed response of SRM drive

The Figure 7 is a graph plotted between the Speed (N) v/s time(s). It displays the result of output speed of Switched reluctance motor which increases up to 1500 rpm. The Figure 8 is a graph plotted between the torque (N-m) v/s time(s). It shows the result of output torque of Switched reluctance motor which increases up to 4.8 N-m.

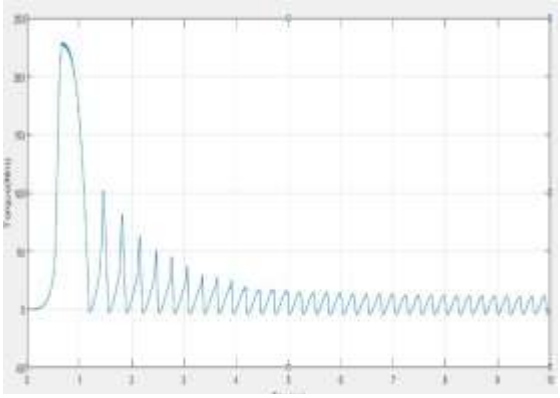

Fig.8. Torque characteristics of SRM drive

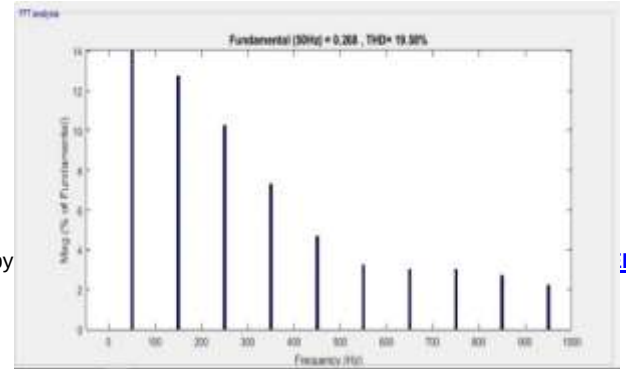

Figure 9 shows the THD and power factor of

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without CSC converter. The obtained THD is 19.58% and power factor is 0.8601. This shows that the system harmonics has increased.

Fig.9.THD and Power factor of without Bridgeless CSC converter

Figure 10 shows the THD and power factor of the system with CSC converter. The obtained THD has reduced to 7.21% and power factor is 0.9639 when a CSC converter was introduced in between the ac mains and Midpoint converter. This shows that the system has low harmonics.

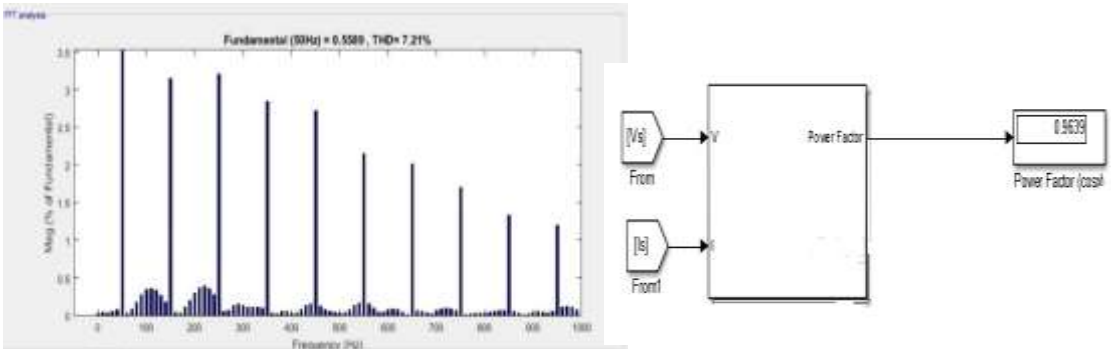

Fig.10. THD and Power factor of with Bridgeless CSC converter

The model of the Bridgeless Canonical switching cell (CSC) Converter developed in MATLAB is given in the Figure11.

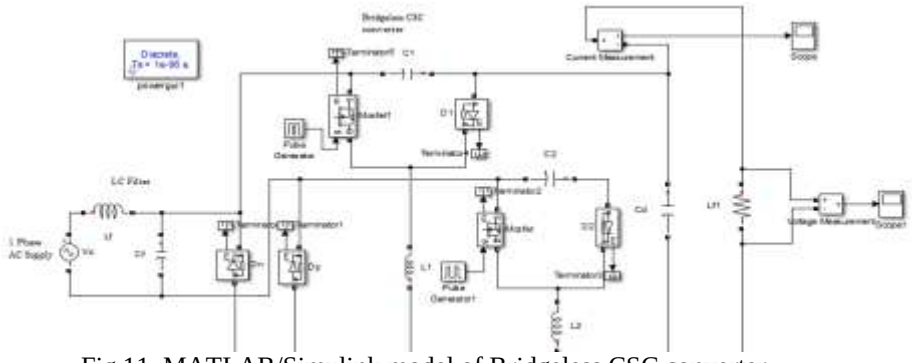

Fig.11. MATLAB/Simulink model of Bridgeless CSC converter

Once simulated in MATLAB the output waveforms were plotted and below graphs are obtained. The output current and output voltage of Bridgeless CSC Converter is shown in Figure 12 and Figure 13. The output voltage of this converter is about 320 V. The output current of this converter is about 2.9A.

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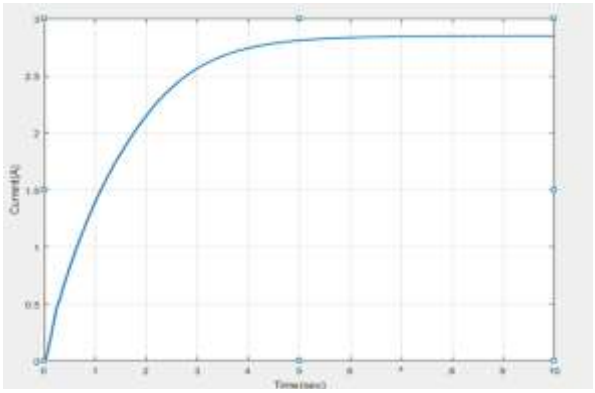

Fig.12. Waveform of output voltage of Bridgeless CSC converter

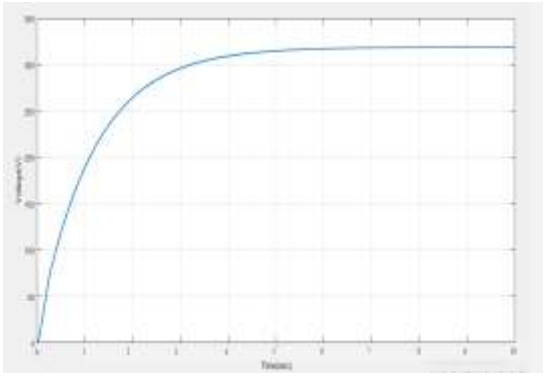

Fig.13. Waveform of output current of Bridgeless CSCconverter

B. Performance During Change in DC Link Voltage

Table III shows the SRM drive performance over wide range of speed control.

Table iii. Srm motor drive performance under wide range of speed control

V_{dc}(V)	ω(rpm)	Is(A) (Peak)	THD of Is(%)	PF
160	1350	1.03	19.58	0.8665
180	1400	1.22	13.67	0.9127
200	1475	1.94	9.70	0.9446
225	1523	2.31	7.21	0.9639
260	1579	2.67	4.07	0.9834
280	1662	3.18	2.99	0.9883
300	1736	3.82	2.44	0.9917
320	1784	4.27	1.81	0.9932

The voltage of DC link is decreased from 320V to 160V, the presentation of this drive during the step change in DC link voltage is well displayed in this table which ends in reduced current input from the supply side. The speed variation on step change in voltage of DC link is reflected. In response to this change, the variation in motor performance is also calculated. The concert of controller is satisfactory as DC link smooth control of voltage is obtained. Therefore, motor control is achieved whereas continuing the power quality as AC mains under acceptable limits.

VII. CONCLUSION

A new system which advances the power quality in Bridgeless CSC converter for SRM drive was anticipated in this project. There is an increased use of power electronic devices in the electrical machines area and drive systems. The usage of such devices has caused in the consumption of current from the ac mains. Thus to minimize the THD and to enhance the power factor of the mains in low power applications, a SRM drive with a Bridgeless canonical switching cell (CSC) converter was used. The simulations are done on MATLAB using the SRM drive with and without Bridgeless canonical switching cell converter. The Simulink results verifies the PFC performance of the Bridgeless CSC converter and THD about 7.21% is obtained with 0.963 PF. The presentation of the future system is estimated

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under varying input AC voltages and initiate agreeable. The indices power quality in speed regulator and fluctuating AC mains voltage is attained inside the limits by IEC 61000-3-2.

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