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A Soft-Switching Bridgeless AC-DC Power Factor Correction Converter

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Abstract: This paper presents a bridgeless PFC boost converter for power supply and battery charging applications. Boost converter operating in CCM is widely used in low power factor corrector due of its simplicity and switching losses. The converter operates in both pulse-width-modulation (PWM) mode and resonant mode in each switching cycle, and use standard average current mode control. The performance of the proposed model is evaluated under varying input voltages and loads by simulating the circuit in MATLAB/Simulink environment.

Keywords: AC-DC converters, PFC, resonant converters, soft-switching, ZCS, ZVS.

I.INTRODUCTION

Power factor correction (PFC) is necessary for nowadays in an ac-dc power supply in accordance with harmonic standards. Power factor correction can be achieved by active or passive methods. The passive filters can be provided to improve power factor and has many drawbacks leading to poor efficiency. The active PFC converters are implemented with single stage approach or with two stage approach. Generally, the CCM boost converters has been used for a PFC circuit, CCM operation has lower conduction losses. The boost converter provided with a diode bride rectifier is most commonly used as an ac-dc converter for PFC. However this converter achieves a simply and a unity power factor with proper control techniques provided. The main drawback of this converter is high switching losses and high conduction losses. In order to reduce the switching losses, many soft switching techniques have been proposed.In the dual boost/bridgeless topology there is no diode bridge rectifier, it reduces the semiconductor devices and reduces the conduction losses. In this paper, a ZVS hybrid resonant pulse width modulated ac-dc converter is proposed; it minimizes the switching losses by achieving the ZVS for all switches. ZCS is provided for the output rectifier diodes reduce the reverse recovery losses.

II.PROPOSED CONVERTER OPERATING PRINCIPLES

The proposed ZVS HRPWM ac-dc PFC converter is shown in Fig. 1. This converter has only one input inductor Lin. The PFC switches S1 and S2 is driven with the same PWM signal, hence it is not necessary to sense both the positive and negative ac line-cycle operation. The converter operates in the resonant mode when S1 and S2 are on, providing resonance between Cr, and Lr, and PWM mode when the auxiliary switch Sa is on, hence its operation can be described as hybrid resonant PWM. The discussion is provided only to the positive half cycle over one switching cycle.The key waveforms for the converter are provided in Fig. 2.

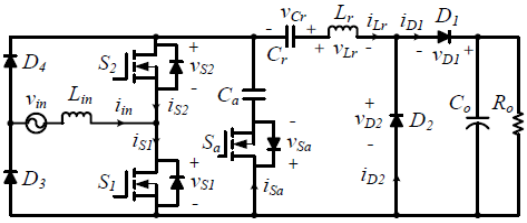

Fig.1 Proposed AC-DC converter

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1) Interval-1(t0-t1): The equivalent circuit is provided in Fig.3(a).This mode starts when the output capacitor Cs1 of S1 is fully discharged and the output capacitor Csa of Sa is fully charged (interval 7). The switch current of S1 is maintained by the body diode D_{s1} to initiate ZVS turn-on of S1. The gating signal vgs_S1/S2 enables ZVS turn-on for both S_1 and S_2. The input current and resonant current are given by (1) and (2)

$$i_{in}(t) = V_{in}/L_{in}(t\text{-}to)+i_{in}(to) \quad (1)$$

$$i_{Lr}(t) = (V_{cr}(min)\text{-}V_o)/L_r(t\text{-}to)+i_{Lr}(to) \quad (2)$$

2) Interval-2(t1-t2): The equivalent circuit is provided in Fig.3 (b).In this mode the switch current is1 follows the resonant current and is the sum of the input current and resonant current. The input current iin stores energy in input inductor Lin. This mode ends when the resonant current is zero, which makes D2 to turn-off with zero-current switching (ZCS) .The resonant current and voltage across the resonant capacitor, are given by (3) and (4)

$$i_{Lr}(t) = -\text{-}i_{Cr}(t) = (V_{Cr(min)}/Z)\sin(\omega_r(t\text{-}t_1) \quad (3)$$

$$v_{Cr}(t) = V_{Cr(min)}[\cos(\omega_r(t\text{-}t_1) - 1] + v_{Cr}(t_1) \quad (4)$$

where $Z = \sqrt{(L_r/C_r)}$ and $\omega r = 1/\sqrt{(L_rC_r}$

3) Interval-3(t2-t3): The equivalent circuit is provided in Fig.3 (c).This mode starts when D2 stops conducting, and there is no current in the resonant branch. In this interval the input inductor stores energy, similar to boost operation This interval ends when switch S1 is turned OFF.

4) Interval-4(t3-t4): The equivalent circuit is provided in Fig.3 (d) and Fig .3(e). At t= t3, the switch S1 is turned-off. The input current charges the output capacitor Cs1 discharges the output capacitor Csa. The switch current of Sa is then clamped by the body diode Dsa.. The input current, resonant current and voltage across the resonant capacitors are given by (5),(6) and (7)

$$i_{in}(t) = (V_{in}\text{-}V_{Ca})/L_{in}(t\text{-}t3) + i_{in}(t_3) \quad (5)$$

$$i_{Lr}(t) = -i_{Cr}(t) = (V_{Cr(max)}/Z)\sin(\omega_r(t\text{-}t_3)) \quad (6)$$

$$V_{Cr}(t) = V_{Cr(max)}[\cos\omega_r(t\text{-}t_3)) - 1] + v_{Cr}(t_3) \quad (7)$$

5) Interval-5(t4-t5): The equivalent circuit is provided in Fig.3 (f). In this mode the gating signal vgs_Sa enables ZVS turn-on for switch Sa after Dsa ,begins conducting in the previous interval.

6) Interval-6(t5-t6): The equivalent circuit is provided in Fig.3 (g).This mode starts when iLr equals iin, and the current through switch Sa starts flowing from drain to source. Hence, the current through switch *Sa* changes its direction. This mode ends when switch Sa is turned OFF.

7) Interval-7 (t6-t7): The equivalent circuit is provided in Fig.3 (h).During this mode the input current iin charges capacitor Csa, and discharges capacitor Cs1. The current through switch S1 is maintained by the body diode in the next interval.

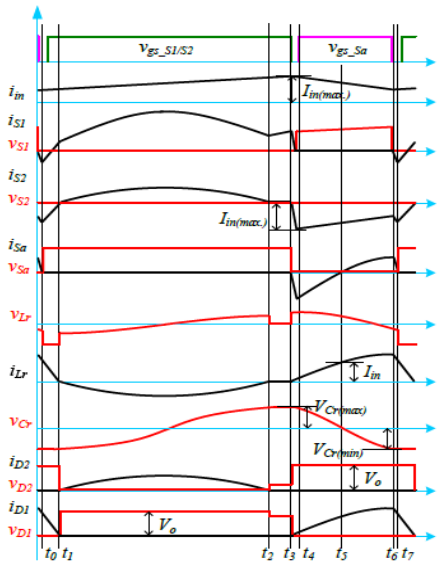

Fig.2.Waveforms explaining proposed converter waveforms.

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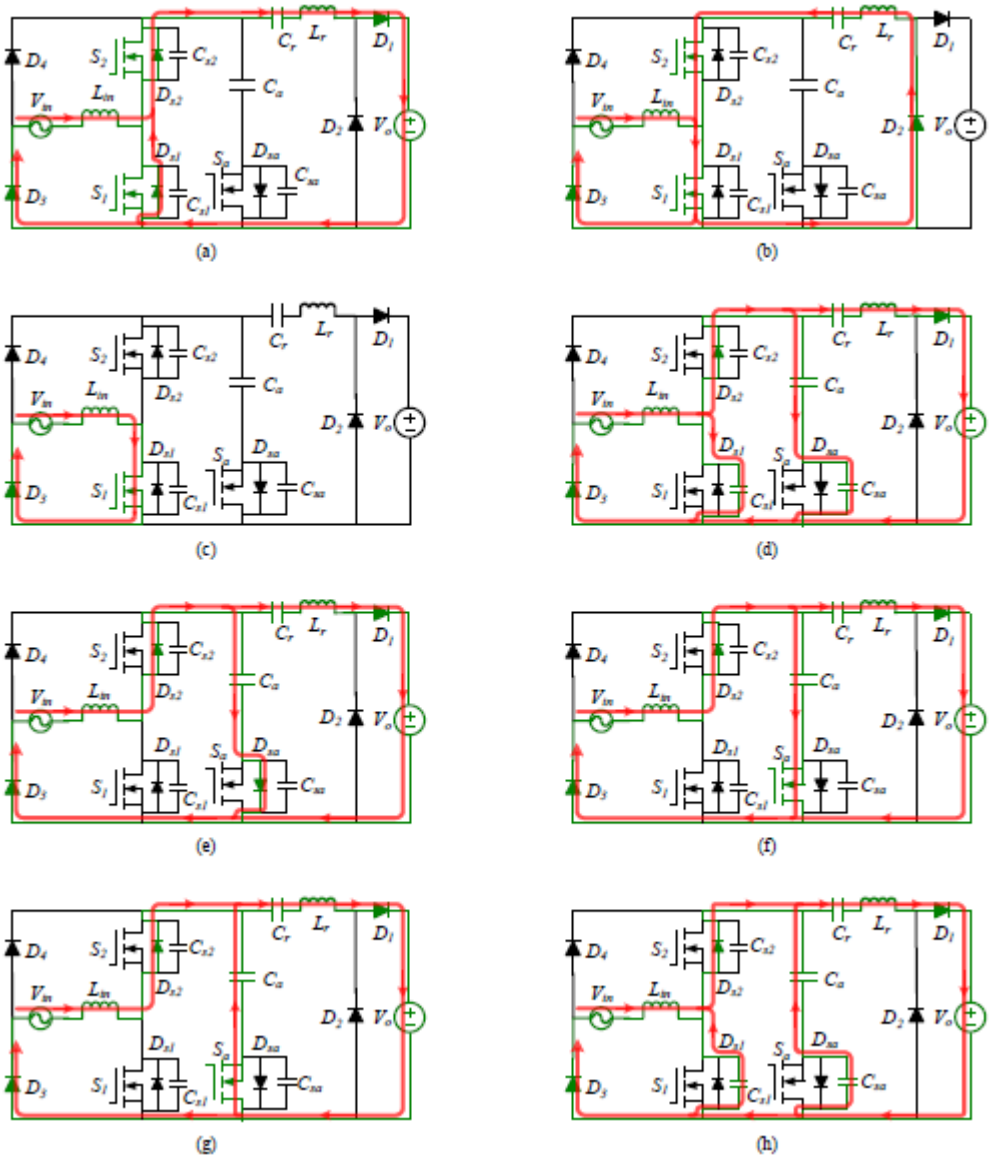

Fig.3.Equivalent circuits for each operation stage for the converter.

III.SIMULATION DIAGRAM OF PROPOSED CONVERTER

The proposed converter system is simulated in MATLAB to check its performance and its simulink model is been shown. The input voltage is taken as 100-200V and the output of the converter was obtained as 400V. The output of the ac-dc converter with and without closed loop control is shown.

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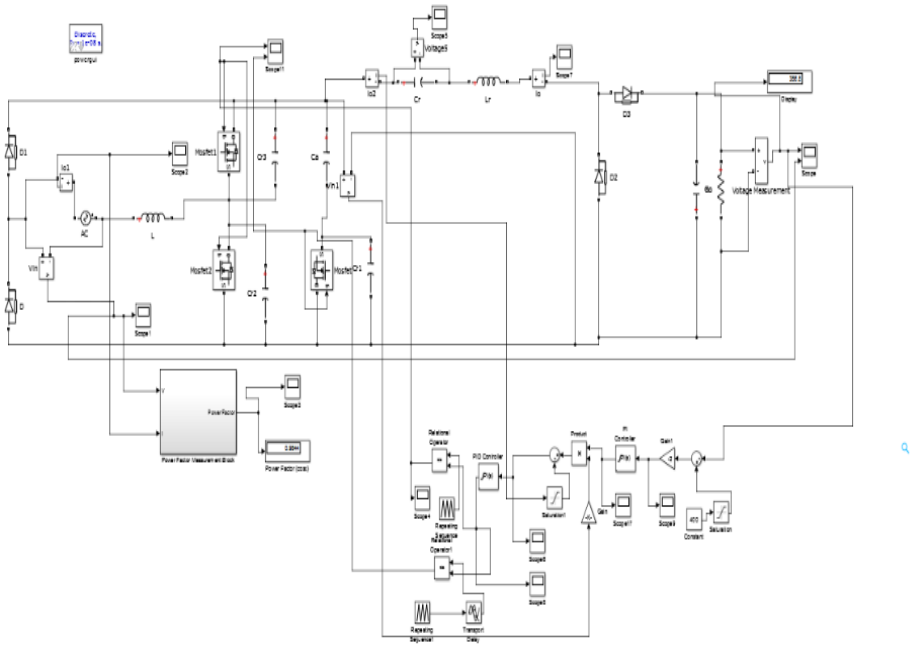


Fig.4.MATLAB Simulation diagram of converter

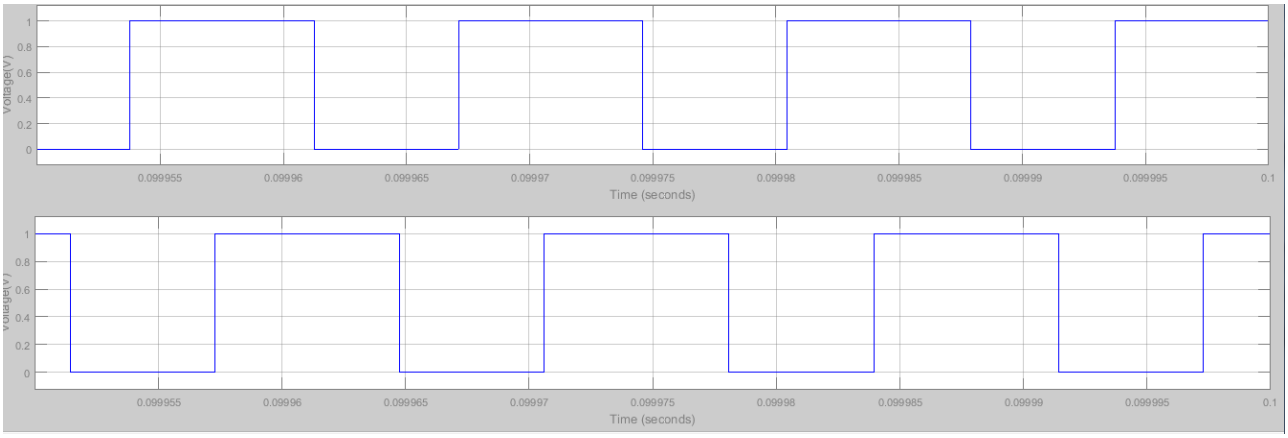
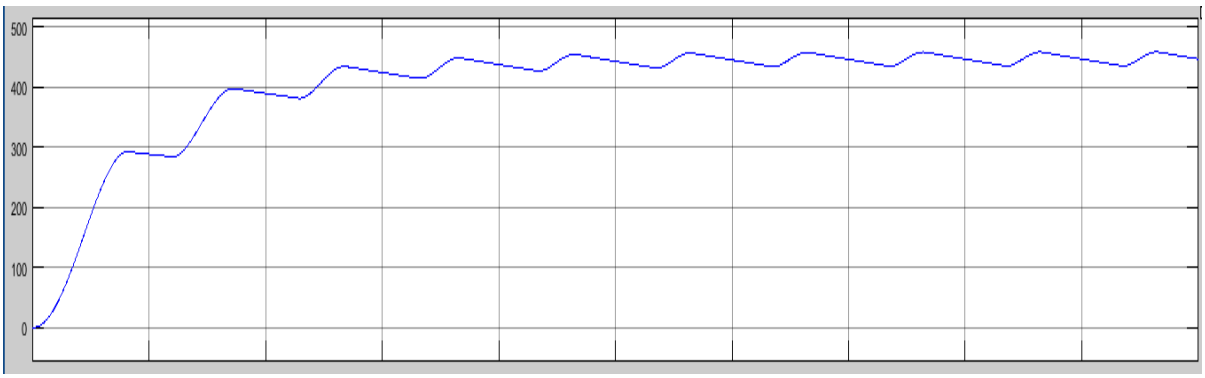


Fig.5. Voltage across switches S_1, S_2, S_a



(a)

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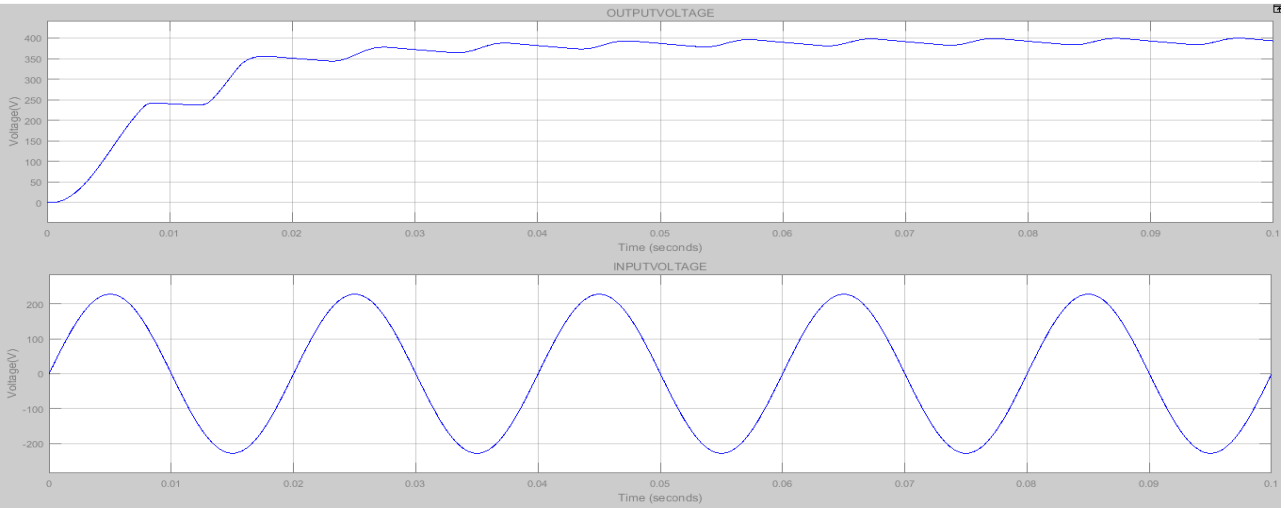

(b)

Fig.6. Waveforms of input voltage and output voltage ((a) with and (b)without closed loop)

IV.CONCLUSION

A ZVS bridgeless boost converter is presented in this paper. The performance of the converter has been evaluated sing MATLAB environment. In the proposed converter switching losses is reduced by soft switching operation across all the semiconductor devices.

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