IJIREEICE

ISSN (Online) 2321-2004
ISSN (Print) 2321- 5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

NFTPCOS-18

National Conference on Future Technologies in Power Control and Communication Systems

College of Engineering Perumon, Kollam, Kerala

Vol. 1, Special Issue 2, March 2018

A PFC BL-Buck Boost Converter for Switched Mode Power Supply using Flyback Inverter

Gopika Krishnan P[1], Dinesh Pai .A [2]

PG student, EEE Department, Government Engineering College Bartonhill, Thiruvananthapuram, India[1]

Professor, HOD, EEE Department, Government Engineering College Bartonhill, Thiruvananthapuram, India[2]

Abstract - The analysis, design, modelling and simulation of a power supply for computers is presented. The proposed SMPS is capable of avoiding the harmonic burden associated with conventional systems. This paper presents the simulation of a SMPS using PFC bridgeless (BL) buck-boost converter at the front end which helps in the reduction of conduction losses and diode reverse recovery problems. The bridgeless buck-boost converter is operating in discontinuous conduction mode (DCM) thereby providing inherent PFC operation and reduces complexity in control. The performance of the proposed model is evaluated under varying input voltages and loads by simulating the circuit in MATLAB/Simulink environment.

Keywords - Bridgeless (BL), power factor corrected (PFC), power quality (PQ) Total harmonic distortion (THD), DCM, High Frequency Transformer (HFT).

I. INTRODUCTION

Power Quality (PQ) related issues are of most concern now days. Power quality is often defined as the grid's ability or the electrical network's ability to supply a clean and stable power supply[1]. The harmonic pollution in the distribution system is a major problem concerning power electronic technology such as mobile phone charging, personal computers etc [2]. Switched mode power supplies (SMPSs) are used in computers for powering up different parts by developing multiple dc voltages from a single phase ac voltage. Conventional SMPS are fed from the supply using a diode bridge rectifier at the front end followed by a bulky filter capacitor. This results in a highly distorted peaky current waveform which is out of phase with the supply voltage. Therefore the harmonic current burden increases and the power factor becomes very low and thereby increasing the losses in the system. The input current has a high value of THD of about 80% with power factor less than 0.5 and crest factor (CF) in the order of 3.8.Such poor power quality violates the standards set by IEC 61000-3-2.
The input voltage and current of a conventional SMPS is shown in Fig 1.The use of single stage SMPS using a single DBR with an isolated converter is used in many applications. However the use of such systems increases the stresses across the switches[3] and thereby the voltage regulation under different loading becomes worse. Different PFC circuits using different converters such as buck, boost were used at the front end to improve the PQ but they are not suitable for computer applications.

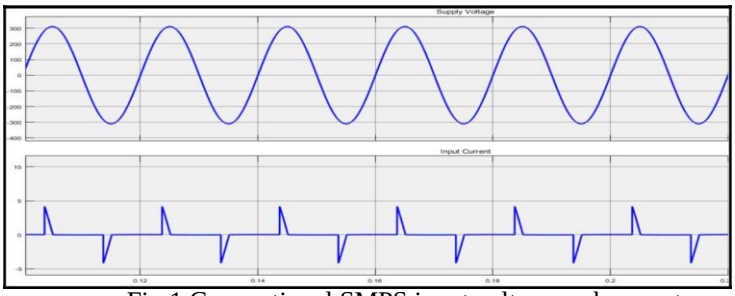


Fig.1 Conventional SMPS input voltage and current

In case of boost converter [5] the voltage cannot be controlled below 350V hence it is difficult to use in computer SMPS where ac varies from 170V to 270V.Buck –boost converters fed from a DBR at front end [6] is a better solution for computer applications but if a higher dc voltage is selected high frequency transformers (HFT) have to be modelled for the particular voltage which increases the losses and moreover the increased voltage results in insulation problems and common mode noise.

IJIREEICE
ISSN (Online) 2321-2004
ISSN (Print) 2321- 5526
International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering
NFTPCOS-18
National Conference on Future Technologies in Power Control and Communication Systems
College of Engineering Perumon, Kollam, Kerala
Vol. 1, Special Issue 2, March 2018

II. BL-BUCK BOOST CONVERTER FED SMPS

The configuration of proposed multiple output SMPS is shown in Fig 2. In which a single phase ac supply is fed to two buck boost converters through a Lin-Cin filter which eliminates the high frequency switches. The BL buck boost converter is designed in DCM to provide inherent PFC and easier control. The upper converter operates in the positive half cycle through the switch Sp, Lp and diodes Dp1 and Dp2.Similarly the lower converter operates for the negative half cycle through Sn, Ln and diodes Dn1 and Dn2.The output dc voltage of the buck boost converter if filtered using the capacitor of the flyback inverter.

The regulated dc output of the converter is fed to a fly back inverter for obtaining multiple dc voltages for the SMPS .The flyback inverter consists of a capacitor C_{11}, switch S1 and multiple output High Frequency Transformer (HFT).The HFT consists of one primary and four secondary windings arranged in a Centre tapped configuration. The secondary side of HFT consists of filter inductors L1, L2, L3, L4 and capacitors Co1, Co2, Co3, and Co4 are connected to each winding to reduce the current and voltage ripples. The output voltages are regulated using closed loop control of the highest rated dc voltage.

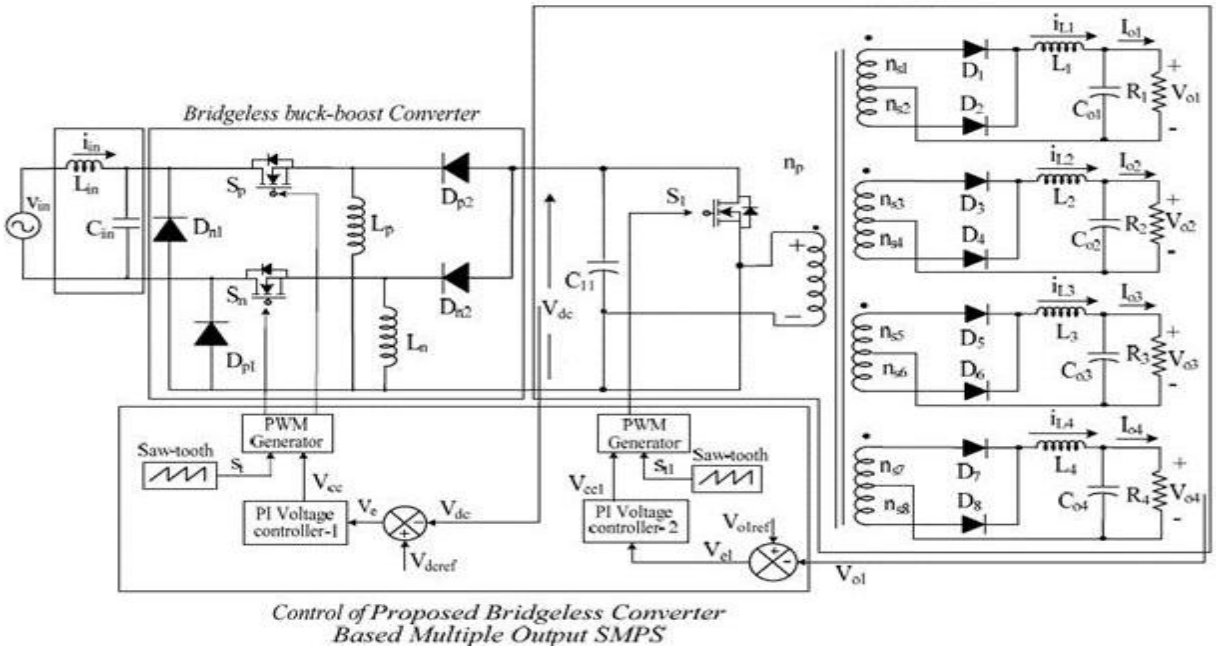


Fig.2 Circuit configuration of proposed SMPS

III. OPERATING PRINCIPLE OF PROPOSED BRIDGELESS CONVERTER FED SMPS

The proposed bridgeless converter fed SMPS consists of two buck boost converters fed from a single phase ac supply, a fly back inverter and a HFT at the load end. The modes of operation of the buck boost converter includes the switching of the upper and lower buck boost converters during the positive and negative half cycles. Fig. 2a and 2b shows the operation of the converter during the positive and negative half cycles.

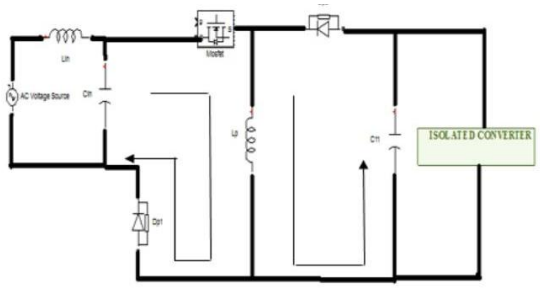


Fig.2a Operation of converter during positive half cycle

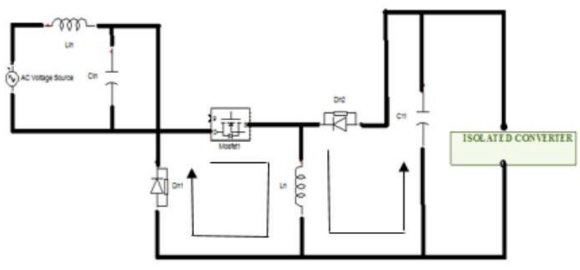


Fig.2b Operation of converter during negative half cycle

IJIREEICE
ISSN (Online) 2321-2004
ISSN (Print) 2321- 5526
International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering
NFTPCOS-18
National Conference on Future Technologies in Power Control and Communication Systems
College of Engineering Perumon, Kollam, Kerala
Vol. 1, Special Issue 2, March 2018

IV. DESIGN OF PROPOSED BL CONVERTER FED SMPS

A. Design of Buck-Boost Converter

The design of the inductors in the buck-boost converters is very important to ensure DCM operation. The values of upper and lower inductors are the same. The inductor value for a specified current ripple is expressed as

$$Lp = \frac{DTVavg}{iLpon} \quad (1)$$

where, D where, D is the duty cycle, i.e., tON/T where tON is the 'on' time of the switch and T is the total period in one switching cycle, Vavg is the average of single-phase ac input voltage across the input of the buck-boost converter.

The inductor current ripple during the DCM condition is considered maximum and it must be equal to twice the input current.

$$i_{Lon} = 2*I_{in} \quad (2)$$

Substituting (2) in (1) yields the value of Lpmin as,

$$Lpmin = \frac{DTV_{avg}}{2i_{in}} = \frac{0.2*50\mu s*198\ V}{2*2.3A} = 430\mu H \quad (3)$$

To maintain DCM operation under all working conditions, the inductor value should be less than one tenth of minimum inductor value [10]. Thus

$$Lp < \frac{Lpmin}{10} \quad (4)$$

The inductor value is calculated as 43 µH for D=0.2, switching time T being 50 µS and Vavg being 198V.

B. Design of Input Filter

To filter the higher order harmonics in the proposed SMPS, it is essential to use an L-C filter. The maximum value of capacitance is expressed as,

$$Cinmax = \frac{Im \tan\theta}{\omega Vm} = \frac{3.25* \tan(1)}{314*311V} = 580nF \quad (5)$$

where Im and Vm are the peak value of input ac current and ac voltage respectively. The maximum capacitance is estimated as 580nF for a θ value of 1°. The capacitance value Cin is selected as 330nF.

The filter inductor for obtaining at input ac mains is calculated as,

$$Lin = \frac{1}{4*\Pi^2*fc^2*Cin} = \frac{1}{4*3.14^2*(50\ kHz)^2*330nF} = 3.07mH \quad (6)$$

where fc is the cutoff frequency. The filter inductor Lin is calculated as 3.07mH.

C. Design of Input capacitor for flyback inverter

The input capacitor is designed to eliminate the harmonics caused due to the single phase ac mains. For proper PFC the supply voltage and current should be in phase. Therefore the input power is expressed as

$$Pin = \sqrt{2}Vin\ Sin(\omega t) * \sqrt{2}IinSin(\omega t) = Vin\ Iin(1-Cos2\omega t) \quad (7)$$

The total current $i_c(t)$ flowing in the capacitor C11 is given by,

$$i_c(t) = \frac{}{} - Vin\ Iin\ Cos\omega t \quad (8)$$

IJIREEICE
ISSN (Online) 2321-2004
ISSN (Print) 2321- 5526
International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering
NFTPCOS-18
National Conference on Future Technologies in Power Control and Communication Systems
College of Engineering Perumon, Kollam, Kerala
Vol. 1, Special Issue 2, March 2018

V_{dc}

The output voltage ripple corresponding to these capacitor current is given by,

$$\Delta V_{dc} = \frac{1}{C}\int i_c(t) = -\frac{I_{dc}}{2\omega C}\text{Sin}2\omega t \quad (9)$$

Sin (ωt) is taken as 1 for the maximum value of voltage ripple at the capacitor. Hence, (9) is rewritten as,

$$C_{11} = \frac{I_{dc}}{2\omega\Delta V_{dc}} = \frac{1.2A}{2*3.14*6V} = 0.31\text{mF} \quad (10)$$

V. SIMULATION PERFORMANCE OF PROPOSED SMPS

The improved PQ SMPS is modelled and evaluated in MATLAB/Simulink. The overall simulation of the proposed BL Converter fed SMPS is shown in Fig.3.

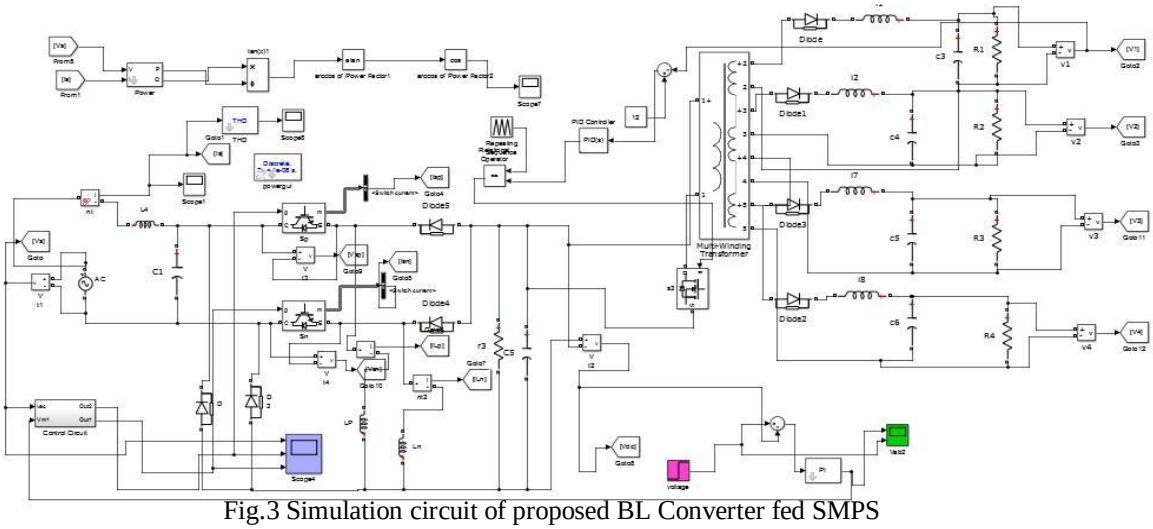
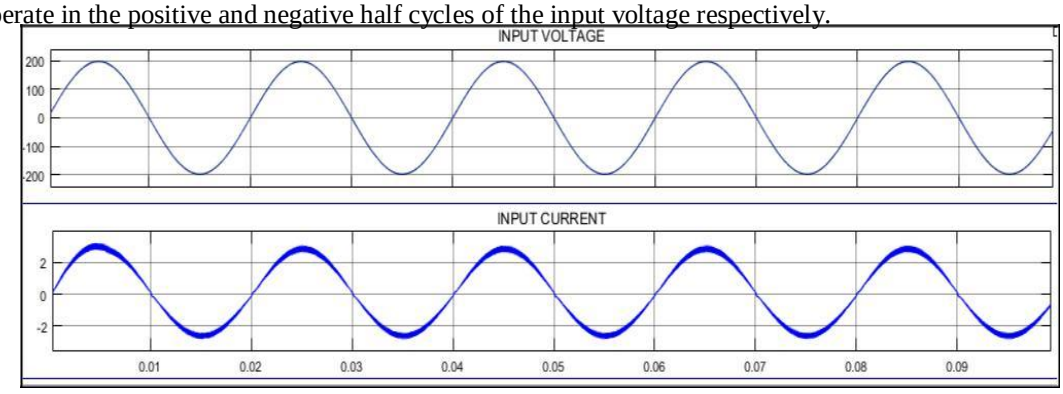


Fig.3 Simulation circuit of proposed BL Converter fed SMPS

A. Steady state performance

The performance of proposed bridgeless converter based multiple output SMPS at 220V ac rms voltage and at full load is performed using MATLAB . The performance of the SMPS is simulated in discrete sampling mode with a sampling time of 1μs.Fig. 3a shows the in phase waveform of supply voltage and input curent. The harmonic distortion of the input current is of the order of 2.37%.The THD of the input voltage is shown in Fig.3b . The waveforms of voltages and current across the switches and current across inductors Lp and Ln is shown in Fig.4.

It is seen that the switches Sp and Sn are turned on alternatively for each half cycles. The peak voltages across the switches is about 550V. The inductor current waveform shows the DCM operation as it touches zero in every switching cycle It clearly shows the DCM of inductor current under all operating conditions. The upper inductor Lp and the lower inductor Ln operate in the positive and negative half cycles of the input voltage respectively.



IJIREEICE
ISSN (Online) 2321-2004
ISSN (Print) 2321- 5526
International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering
NFTPCOS-18
National Conference on Future Technologies in Power Control and Communication Systems
College of Engineering Perumon, Kollam, Kerala
Vol. 1, Special Issue 2, March 2018

Fig.3a.Waveform of supply voltage and current.

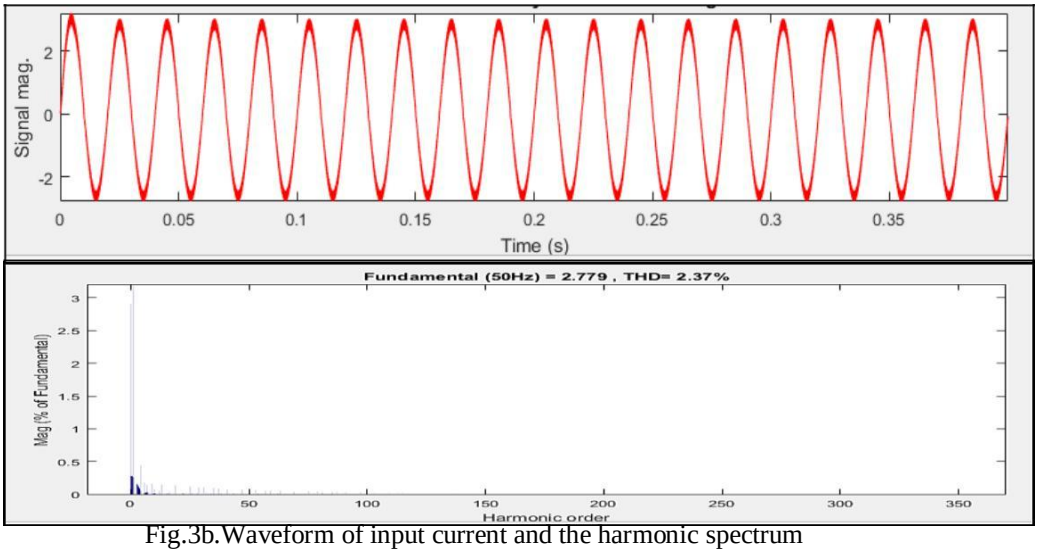


Fig.3b.Waveform of input current and the harmonic spectrum

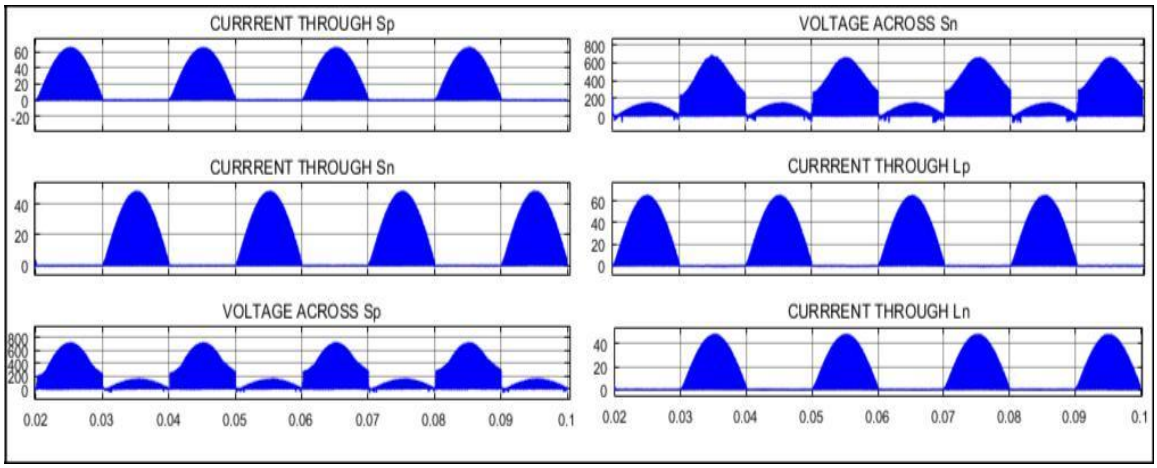


Fig.4 Waveforms of current and voltages of various components

B. Performance under Varying Input Voltages

The performance of the proposed computer SMPS is simulated by varying the input voltages from 170-270 Vrms.Table I shows the value of power factor and THD for different supply voltages.For an input voltage of 170V the power factor obtained is about 0.9997 with a THD of about 2.01% and as the voltage is increased to 270V the THD in the input current is measured as 3.2%.

Table I
POWER FACTOR AND THD FOR VARYING INPUT VOLTAGES

Vin(rms)	THD OF INPUT CURRENT Is (%)	PF
170V	2.01%	0.9997
220V	2.37%	0.9996
270V	3.2%	0.9992

IJIREEICE
ISSN (Online) 2321-2004
ISSN (Print) 2321- 5526
International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering
NFTPCOS-18
National Conference on Future Technologies in Power Control and Communication Systems
College of Engineering Perumon, Kollam, Kerala
Vol. 1, Special Issue 2, March 2018

C. Performance under Varying Load

The performance of the propsed drive is studied by applying a small step change in the load of +12V,+5V,+3V and +6.2V .The output voltage of the buck boost converter is regulated effectively.Fig.5. shows the output voltages with varitions in12V,+5V, +3V and +6.2V.

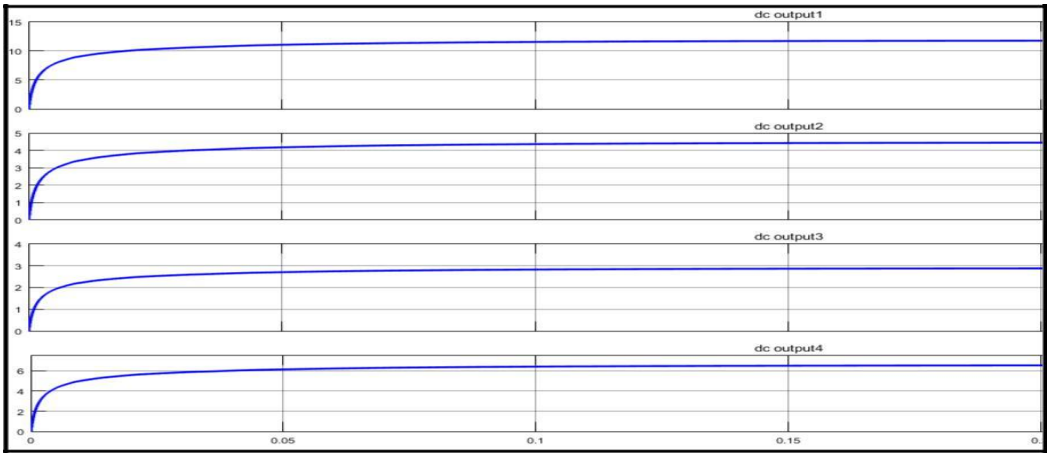


Fig.5.Output voltages with load variations in+12V,+5V,+3V and +6.2V

VI. CONCLUSION

The performance of the PFC BL buck boost converter fed SMPS have been evaluated using MATLAB/Simulink environment. The proposed drive is evaluated under variation of input voltages. The results shows that the PFC BL buck boost converter fed SMPS has a greater improvement in supply current and improved PF compared to conventional SMPS. It is a recommended solution for improving the power quality in systems.

REFERENCES

[1] W. Hart, *Power Electronics*, Tata McGraw-Hill, 2011.
[2] Limits for Harmonic Current Emissions, International Electro technical Commission Standard, 61000-3-2, 2004.
[3] IEEE Recommended Practices and Requirements for Harmonics Control in Electric Power System, IEEE Standard 519, 1992.
[4] B. Singh, S. Singh, A. Chandra and K. Al-Haddad, ―Comprehensive study of single-phase ac-dc power factor corrected converters with high frequency isolation,"*IEEE Trans. Ind. Inf.*, vol.7, no.4, pp.540-556, Nov. 2011.
[5] B. Lehman and R. M. Bass, ―Recent advances in averaging theory for PWM DC-DC converters,'' in *35th IEEE Conf. on Decision and Control*, vol. 4, 1996, pp. 4467-4471.
[6] Yen-Fang Li, Ming-Fa Tsai, Chung-Shi Tseng and Yi-Fan Chiang, ―Model reference adaptive control design for the buck-boost converter," in *38th Annual Conf. on IEEE –IES, IECON'12*, Oct. 2012, pp. 543-548
[7] MathWorks, Inc. Protected by U.S. patents ©1984-2012.
[8] C. S. Moo, H. L. Cheng and Y. N. Chang, ―Single-stage high-power factor dimmable electronic ballast with asymmetrical pulse-width modulation for fluorescent lamps,"*IEE Proc. on Electric Power Applications*, vol. 148, no. 2, pp. 125-132, March 2001.
[9] S.Abe, T. Ninomiya, J.Yamamoto and T. Uematsu,―Transient response comparison of conventional and output inductor less two stage DC-DC converter with low voltage/high current output," in 9th *IEEE Inter. Conf. on Power Electronics Congress, CIEP'04*, 2004,pp. 67-70.
[10] Vlatko Vlatkovic, Dusan Borojevic and Fred C. Lee, ―Input filter design for power factor correction circuits,"*IEEE Trans. on Power Electronics*, vol. 11, no.1, pp. 199-205, January 2005.
[11] Raising the efficiency of power- factor correction, from standby to full load, ON Semiconductor Components Industries, 2014.