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Performance Evaluation Of Cntfet Based Inverter Design

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Abstract: Carbon nanotubes based FET devices are getting more importance today because of their high channel mobility and improved gate capacitance versus voltage characteristics. This discussion provides an overview of carbon nanotubes, Operation of CNTFET, current types of CNTFETs, V-I characteristics of CNTFET, and comparison of type of CNTFET on different design parameters.

Keywords: Ballistic transport, carbon nanotubes (CNTs), non-equilibrium Green's function (NEGF), technology computer aided design (CAD).

I. INTRODUCTION

Moore's law describes a long-term trend in the history of computing hardware. The quantity of transistors that can be placed inexpensively on an integrated circuit has doubled approximately every two years. The trend has continued for more than half a century until 2007. Recent advancements made this law to continue even after this period. The scaling down of devices has been the driving force in technological advances since late 20th century. Aggressive scaling of CMOS circuits has led to higher and higher integration density, more functional complexity and better performance. However further scaling down has faced serious limits related to fabrication technology and device performances asthecritical down to sub-22 nm range. Within the bounds of MOS technology, the possible circuit realizations may be based on pMOS, nMOS, CMOS and even BiCMOS devices. As the device dimensions, such as the channel lengths approach to the sub-10 nm regime, direct tunnelling Between source (S) and drain (D), and severe short channel effects present a fundamental challenge in continued scaling of Silicon devices .The main drawbacks of the MOSFET is that the sensitivity of a MOSFET's gate to static and high-voltage spikes makes it vulnerable to damage resulting from parasitic oscillation. This undesired self-oscillation could result in excessive gate-to-source voltage that permanently damages the MOSFET's gate insulation [1]

Many solutions are proposed to overcome these limitations. Some solutions include modifications on the existing structures and technologies with a hope of extending their scalability. Other solutions involve using new materials and technologies to replace the existing silicon MOSFETs. Researchers currently focused on identifying alternatives which would enable continued improvement in the Performance of electronics systems are high dielectric constant (High–K) insulating material, metal gate electrode, double gate FET. High-K dielectric materials are useful for gate insulators as they can provide efficient charge injection into transistor channels and reduce direct tunnelling leakage currents [2].

Silicon based technology will reach its limits in 2020 when the channel length of MOSFET is below 10nm. For this reason, the semiconductor industry is looking for different materials and devices to integrate with the current siliconbased technology or maybe, in a long term future, even substitute it. Among the number of investigated solutions such as single-electron tunnelling (SET), rapid single-flux quantum logic, quantum cellular automata (QCA) and carbon

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nanotubes (CNT) [3].CNTFETs are novel devices that are expected to sustain the transistor scalability while increasing its performance. One of the major differences between CNTFETs and MOSFETs is that the channel of the former devices is formed by CNTs instead of silicon, which enables a higher drive current density, due to the larger current carrier mobility in CNTs compared to bulk silicon [1].CNTs can be exploited to build both low-resistance high-strength interconnections and highly scalable low-power carbon nanotube field-effect transistors (CNTFET) and single electron tunnelling transistors [3].

II. BASICS OF CARBON NANOTUBES

The Carbon nanotubes were discovered by S. Ijiima in1991 while performing some experiments on molecular structure composed of carbonium. They can be considered as the result of folding graphite layers into carbon cylinders and may be composed of a single shell–single wall nanotubes(SWNTs), or of several shells-multi-wall nanotubes(MWNTs) as shown in fig.1. Depending on the folding angle and the diameter, nanotubes can be metallic or semiconducting. Based on the chiral vector, the circular vector that is perpendicular to the axis of the tube [1].

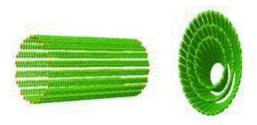


Fig. 1.single walled and multi walled nanotubes [1]

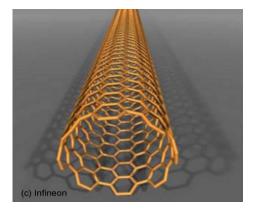


Fig.2. single walled CNT atoms structure [7]

An SWCNT can act as either a conductor or a semiconductor, depending on the angle of the atom arrangement along the tube. This is referred to as the chirality vector and is represented by the integer pair (n, m). A simple method to determine if a CNT is metallic or semiconducting is to considers its indexes (n, m). The nanotube is metallic if n = m or n - m = 3i, where i is an integer. Otherwise, the tube is semiconducting. The diameter of the CNT can be calculated based on the following.

$$D_{CNT} = \frac{\sqrt{3} a_0}{\pi} \sqrt{n^2 + m^2 + mn^0}$$

Where a 0 = 0.142 nm is the inter-atomic distance between each carbon atom and its neighbour.

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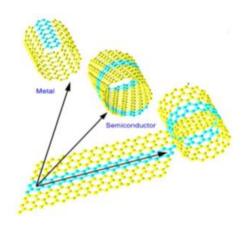


Fig.3 Different morphological configurations[7]

Most single walled nanotubes (SWNT) have a diameter of close to1 nanometre, with a tube length that can be many millions of times longer. The structure of a SWNT can be conceptualized by wrapping a one-atom-thick layer of graphite called graphene into a seamless cylinder [2].

III.CARBON NANOTUBE FIELD EFFECT TRANSISTOR

A CNFET is formed by a carbon nanotube connecting two metal electrodes on either side that form source and drain contacts, with gate electrode separated from the nanotube by a thin oxide film. Even though different types of gate structures are in use, a coaxially gated CNTFET is considered for symmetry and optimal results. Single-walled carbon nanotube (SWCNT) transistors have attracted intensive attentions for their potential as a novel generation of basic cells.

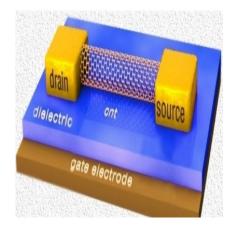


Fig. 4.Schematic diagram of a CNTFET [8].

The valence and conduction bands of the carbonnanotube are symmetric, which allows complementary structures in applications. The nearly ballistic transport at low bias implies the possibility of deriving carbon nanotube transistors.CNTFET could be more of an interest due to its similarities with MOSFET in terms of inherent electronic properties. Due to these similarities, previously designed CMOS architectures and basic CMOS-based platforms can still be used without any major modifications.

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IV. CNTFET OPERATION

Stanford University 32nCNTFET model is the Ballistic CNTFET model. For this model

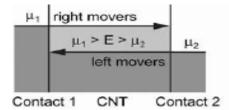


Fig.5: Illustration of a ballistic transport in a CNTFET [1]

The carriers are injected into the CNT from contact 1 with energies up to μ 1 and from contact 2 with energies up to μ 2. There is no scattering in the CNT, and carriers that are injected at certain energy E traverse the tube without any energy loss. The electrochemical potential equilibrates inside the macroscopic leads. The net current is carried by carriers with energy between μ 1 and μ 2 that travel from contact 1 to contact 2.

The peripheral length of the nanotube is given by

$$L = |Ch| = a * \sqrt{n^2 + nm + m^2}$$

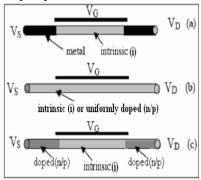
Semiconducting nanotubes are placed under the gate as channel region, while heavily doped CNT segments are placed between the gate and the source/drain to allow for a low series resistance in the ON-state. As the gate potential increases, the device is electro-statically turned on or off via the gate. The gate-to-source voltage that generates the same reference current is taken as the threshold voltage for the transistor that has different chirality. CNTFETs provide a unique opportunity to control threshold voltage by changing the chirality vector, or the diameter of the CNT [2].

V. TYPES OF CNTFETs

This section summarizes several types of CNTFETs fabricated so far. There are 3 possible CNTFET structures: Schottky-barrier (SB) CNTFET partially-gated (PG) CNTFET and doped-S/D CNTFET

In SB CNTFET type, the gate modulates the tunneling transmission through a SB between the source-metal and the nanotube channel. SB-CNTFETs exhibit strong ambipolar characteristics that limit the use of these transistors in conventional CMOS-like logic families because these SB-CNTFETs convert their functionality from n-type to p-type and vice versa depending on the gate bias. More important, the ION/IOFF ratio is rather small.

PG CNTFET are uniformly doped (or uniformly intrinsic) with ohmic contacts at their ends. PG-CNTFETs can be of n-type or p-type when respectively n-doped or p-doped. These devices work in a depletion mode.



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Fig.6.Three possible types of CNTFETs (a) Schottky barrier,(b)partially-gated and (c) doped-S/D transistors[3].

Doped-S/D CNTFETs are composed of two un-gated portions that are heavily or lightly n/p doped.

Parameter	SB-	PG-	C-CNTFET
	CNTFET	CNTFET	
Diameter	~1.4nm	~1.4nm	~1.6nm
Gate position	Тор	Local	Тор
Tox(nm)	1.5	4	8
Dielectric	ZnO2	Al2O3	HfO2
S/D metal	Ti	Ti	Pd
CNT length	260nm	600nm	80nm
Vds(V)	0.5	0.5	0.5
Ion(microA/micro	535	71	2500
m)			
Ion/Ioff	10^4	10^4	10^6
S(mV/dec)	n-type:312	p-type:63	n-type:80
	p-type:130		p-type:70
Gm(S/microm)	p-type:1160	-	n-type:6250
			p-type:3125
Vth(V)	n-type:0.3	p-type:0.5	n-type:0.6
	p-type:0.5		p-type:0.5

The ON-current is limited by the amount of charges that can be induced in the channel by the gate and not by the doping in the source. They operate in a pure p- or n-type enhancement-mode or in a depletion-mode based on the

Principle of barrier height modulation when applying a gate[3].

VI. I-V & C-V CHARACTRISTICS

Knowing the surface potential CPs in terms of the terminal voltages the drain current, ID and quantum capacitance, CQ can be obtained as follows:

$$I_{D} = \frac{4qkT}{h} \left[ln(1 + exp(\varepsilon_{S})) - ln(1 + exp(\varepsilon_{D})) \right]$$

$$C_{Q} = \frac{\partial Q_{CNT}}{\partial V_{GS}} = \frac{\partial Q_{CNT}}{\partial \phi_{S}} = \frac{\partial \phi_{S}}{\partial V_{GS}}$$

Where,

$$\frac{\partial \mathbf{Q}_{\text{CNT}}}{\partial \phi_{\text{S}}} = \mathbf{q} \left(\frac{\partial \mathbf{N}_{\text{S}}}{\partial \phi_{\text{S}}} + \frac{\partial \mathbf{N}_{\text{D}}}{\partial \phi_{\text{S}}} \right)$$

h is the Planck's constant and Q CN'F is the charge mobile [4].

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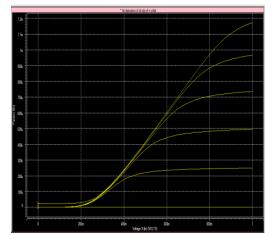


Figure 7: Simulated Transfer Characteristic N-CNTFET.

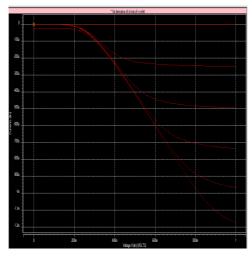


Figure 8: Simulated Transfer Characteristic P-CNTFET.

VII. CONCLUSION

Carbon nanotube (CNT) is it Honeycomb tube made of graphene sheet that can grow of up to millimeters in length and the size is within nanometer scale. The size of CN'T gives a possibility of making small-scale transistor and it also has unique properties that can boost the device performance such as it has very high current density. Depending on its chirality, CNT can have either semiconducting or metallic characteristic. Semiconducting CNT can be used as transistor channel since it has the characteristic of semiconductor whereas metallic CNT can be used as wire on circuit boards or electronic interconnections. As it conclusion, C'NFET has large potential that can be exploited to be an effective switching device. CTFET is still far to be a commercial device in electronic industry but the researchers are pushing very hard to improve its performance in order to replace MOSFET as the heart of digital applications Our future work will focus on the influence of these parameters on basic logic gates (NOT,NAND, NOR, etc.),and examine its potential for digital circuits.

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REFERENCES

- [1] R. Martel, H.-S. P. Wong, K. Chan, and P. Avouris, "Carbon nanotube field-effect transistors for logic applications," in IEDM Tech. Dig., 2001,pp. 159-162.
- (2004). The International Technology Roadmap for Semiconductor 2004 Update, ITRS Handbook. [Online]. Available: http://public.itrs.net [2]
- [3]
- S. Iijima, "Helical microtubules of graphite carbon," Nature, vol. 354, no. 6348, pp. 56–58, Nov. 1991. S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and P. Avouris, "Carbon nanotubes as schottky barrier transistors," Phys. Rev. [4] Lett., vol. 89, no. 10, pp. 106801-106803, Aug. 2002.
- [5] J. Appenzeller, J. Knoch, R. Martel, V. Derycke, S. Wind, and P. Avouris, "Short-channel like effects in schottky barrier carbon nanotube fieldeffect transistors," in IEDM Tech. Dig., 2002, pp. 285–288.
- [6] G. Fiori and G. Iannaccone, "Code for the 3-D simulation of nanoscale semiconductor devices, including drift-diffusion and ballistic transport in 1-D and 2-D subbands, and 3-D tunneling," J. Comput. Electron., vol. 4, no. 1, pp. 63-66, Sep. 2005.
- [7] S. Datta, "Nanoscale device modeling: Green's function method," Superlattices Microstruct., vol. 28, no. 4, pp. 253–277, Jul. 2000.
- J. Guo et al., "Performance analysis and design optimization of near ballistic carbon nanotube field-effect transistors," in IEDM Tech. Dig., [8] 2004, pp. 703-706.
- [9] R. Saito, G. Dresselhaus, and M. S. Dresselhaus, Physical Properties of Carbon Nanotubes. London, U.K.: Imperial College Press, 2003, pp.35-58.
- [10] R. Lake, G. Klimeck, R.C. Bowen, and D. Jovanovic, "Single and multiband modeling of quantum electron transport through layered semiconductors devices," J. Appl. Phys., vol. 81, no. 12, pp. 7845-7869, Feb. 1997.
- [11] A. Svizhenko, M. P. Anantram, T. R. Govindam, and B. Biegel, "Two-dimensional quantum mechanical modeling of nanotransistors," J. Appl.Phys., vol. 91, no. 14, pp. 2343-2354, Nov. 2001.