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# Performance Evaluation of 30 nm Double Gate MOSFET using VTCAD Tool

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**Abstract**: Scaling the transistor sizes in the sub micro-meter regime has made it difficult to overcome the problem of short channel effects. Double Gate (DG) MOSFETs reduce the short channel effects and provide a better control of the threshold voltage by utilizing the electrostatic coupling from two gates on either side of the channel. Independent control of front and back gate in DG devices can be effectively used to improve performance and reduce power in sub-50nm circuits. In this paper, our aim is to carry out simulations of Symmetric 30 nm Double Gate MOSFET in VTCAD and to improve the performance of MOSFET by studying the MOSFETs with double gate.

**Keywords**: Double Gate MOSFETs, Short Channel Effects, VTCAD, Drain Induced Barrier Lowering

## I. INTRODUCTION

Since late 1970s, Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has been a fundamental building block of microelectronics and VLSI Design for producing highly efficient and advanced Integrated Circuits (ICs). Moore's law has not only increased the complexity of the ICs but it also holds true till date only because of continuous down scaling of MOSFET dimensions. However, MOSFET size cannot be downscaled invariably, there are definite restrictions to it. As one tries to reduce the MOSFET channel length beyond a particular limit, the gate voltage starts losing its control over the drain current due to the onset of various Short Channel Effects (SCEs) such as threshold voltage roll-off and drain induced barrier lowering (DIBL). [1]

In conventional MOSFET technologies, SCEs are suppressed by reducing the gate oxide thickness and increasing the channel doping concentration. But as device enters the size range of 100nm or below the reduced gate oxide thickness leads to an abrupt increase in direct tunnelling current which further leads to an unwanted increase in the standby power consumption of the MOS device. Also an increased doping concentration leads to severe speed reduction in MOS devices (International Technology Roadmap for Semiconductors, ITRS-2004). To resolve the problem and in order to keep pace with Moore's law it is important to consider other non-classical MOSFET structures such as Double Gate MOSFETs, Triple-Gate MOSFETs, FINFETs, Gate All Around MOSFETs etc. for an improved device performance.
As per ITRS, device size scaled down to 7nm is expected around 2019. Such tiny dimensions would make the modeling of SCEs even more essential and complicated than today [3].

Double Gate MOSFET (DG MOSFET) provide an advantage over single gate MOSFETs in terms of low subthreshold leakage, high ON-current, an ideal 60mV/decade slope etc. and hence an excellent control over SCEs especially in subthreshold 100nm or below regime. Hence DG MOSFETs are being considered as a major substitute to single gate devices to reach high scaling limits. DG MOSFET is a device having two gates both separated by gate oxide of same thickness or different depending upon requirement as shown in fig. 2.

Presence of two gate increases gate coupling thus gate control over the channel increases. Therefore, better drain current is achieved. Due to two gates the fringing electric field lines from drain to source also vanish. The main idea of a DG MOSFET is to control the silicon channel very efficiently by choosing the silicon channel width to be very small and by applying a gate contact to both sides of the channel. This concept helps to reduce the short channel effects and leads to higher currents as compared with a MOSFET having only one gate. The larger the number of gates, better electrostatic control of the channel[4-7].

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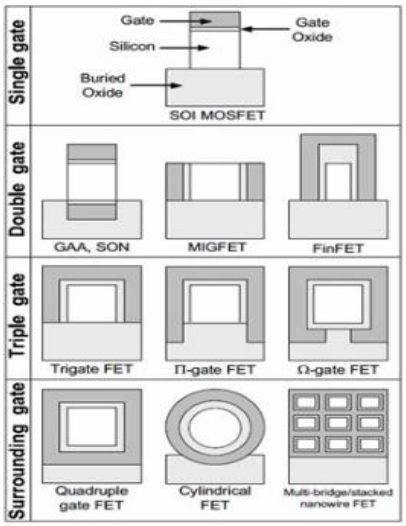


Fig 1. Multigate Transistors [2]

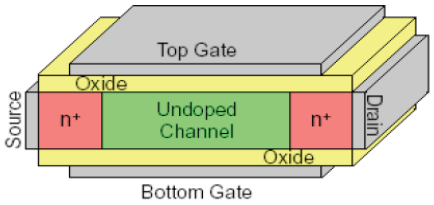


Fig 2. Structure of double gate MOSFET

## II. LITERATURE REVIEW OF DOUBLE GATE MOSFETS

F. Balestra, S. Cristoloveanu and M. Benachir presents "Double Gate Silicon on Insulator Transistor with Volume Inversion: A New Device with Greatly Enhanced Performance." Experimental and calculated characteristics for a new transistor following the concept of volume inversion is explored. It discusses the structure and operation of double gate MOSFET. Better electrical characteristics obtained for this device than conventional device.

Xuejue Huang, et.al. presents "Sub-50 nm P-Channel FinFET". It discusses fabrication of sub-50nm p-channel FETS with self-alligned double gate and vertical ultra-thin fins. In this technique source drain fabricated before gate. On the basis of simulations this structure is scalable to 10nm.High drive current of 820(μA/μm) obtained.

Mini Bhartia, Shrutika Satyanarayana and Arun Kumar Chatterjee presents "Design of 45 nm Fully Depleted Double Gate SOI MOSFET". In this impact of gate oxide thickness and channel doping upon threshold voltage, Ion and Ioff is studied.

Sharda P Narwade, Anish U Bhurke and Swapnali Makdey presents "Study on Performance of 22nm Single Gate and Multi-Gate MOSFET". Comparison is done for 22nm gate length of planar MOSFET and double gate MOSFET-Transconductance almost doubled, subthreshold slope improved, Ion/Ioff improved and threshold voltage decreases for double gate MOSFET. Device structure simulated is 2D in Visual TCAD.

Vinay Kumar Yadav, Ashwani K. Rana presents "Performance Analysis of Double Gate MOSFETs with Different Gate Dielectric". This paper investigates impact of using different gate dielectric on device performance. As dielectric constant increases, threshold voltage decreases, Ion and Ioff increases. Simulations done on Sentaurus TCAD simulator for gate length of 30nm.

## III. OPERATION OF DG-MOSFET

DG MOSFET is comprised of a conducting channel (usually undoped), surrounded by gate electrodes on either side. This ensures that no part of the channel is far away from a gate electrode [8]. The applied voltage on the gate terminals controls the electric field, determining the amount of current flow through the channel. Depending on the application of gate voltages, DG-MOSFETs are categorized as following:

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### 1. Symmetric DG-MOSFET (SDG)

A DG-MOSFET is said to be symmetric (fig. 3) when both gates have the same work function and a single input voltage is applied to both gates. At ON-state, the two conductive channels (inversion layers) are formed on the two side of silicon body for the SDG device. These channels conduct at the same time. In addition, the SDG device shows higher carrier mobility due to its lower transverse electric field as compared to the ADG device. [9]

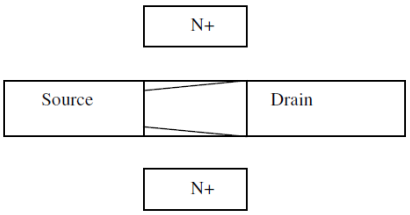


Fig 3. Symmetric DG MOSFET [9]

### 2. Asymmetric DG-MOSFET (ADG)

An asymmetric DG-MOSFET (fig. 4) either has synchronized but different input voltages to both of the identical gates, or has the same input voltage to two gates but gates having different work functions. DG MOSFET switching can be obtained by applying different voltage at both the gate. Only one channel is formed for the ADG device unless the operation voltage is extremely high to form the other inversion layer near the P+ gate. The threshold voltage of an ADG MOSFET can be adjusted by changing the body thickness (Tsi) and/or the gate-oxide thickness (Tox), without the need for exotic gate materials.

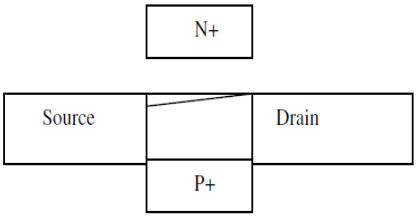


Fig 4. Asymmetric DG MOSFET [9]

## IV. SHORT CHANNEL EFFECTS

As the dimensions of the transistors are shrunk, the close proximity between the source and the drain reduces the ability of the gate electrode to control the potential distribution and the flow of current in the channel region, and undesirable effects called the “short-channel effects” start plaguing MOSFETs.
The SCEs can range from increased off-current due to threshold-voltage roll-off, Drain-Induced Barrier Lowering (DIBL), and degraded subthreshold slope, to degraded output resistance.

### 1. DIBL

DIBL effect occurs in short-channel devices when the depletion regions of the drain and the source interact with each other near the channel surface which results in lowering of the source potential barrier height. On application of drain voltage, barrier height reduces in the influence of drain electric field. This leads to injection of more carriers in the channel region but this increase in the carrier is due to drain voltage and not by gate voltage [10].
DIBL is defined as the ratio of change in threshold voltage to change in drain voltage.

$$\mathrm{DIBL} = \frac{\Delta V_{TH}}{\Delta V_{DS}} \qquad (1)$$
$$= \frac{V_{TH}(V_{DS1}) - V_{TH}(V_{DS2})}{V_{DS2} - V_{DS1}}$$

DIBL is more prominent at high drain voltages and shorter channel lengths. DIBL can be reduced by using higher surface and channel doping [11].

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## 2. Subthreshold region and Subthreshold Swing

When $V_{GS}$ is smaller than but close to $V_{TH}$, a small conduction current flows between source and drain in the MOSFET and it is said that transistor is in subthreshold or weak inversion region. In weak inversion region, minority carrier concentration is small, but not zero. Subthreshold swing ($S_t$) is an important parameter which determines the scalability limits of DG MOSFET. It indicates how effectively the flow of drain current of a device can be stopped when $V_{GS}$ is decreased below $V_{TH}$.[12-15]

$$`S_t = \left(\frac{d(\log_{10} I_{DS})}{dV_{GS}}\right)^{-1} \quad (2)$$

## V. DG-MOSFET IMPLEMENTATION

To design a DG MOSFET at 32nm technology. First we made geometry of the Double Gate MOSFET in which we define various region which are Substrate, Gate Contact (G), Drain (D), and Source (S). Table 1 shows regions and materials used in simulation of device. Table 2 shows doping profiles used in device.

A symmetric DG-MOSFET of (L=0.04um x H=0.01um) with the Source region and the Drain region (L=0.0005um x H=0.01um) and Substrate (L=0.0005um x H=0.01um) along with TOP GATE& BOTTOM GATE (L=0.03um x H=0.002um) and Oxide 1 & Oxide 2 (L=0.03um x H=0.001um) is drawn in Visual TCAD.

Table I. Regions and materials used in 30 nm device

| Region | Material |
|---|---|
| Substrate | Silicon |
| Source | Aluminium |
| Drain | Aluminium |
| Top gate | NPolySi |
| Bottom gate | NPolySi |

Table II. Design parameter of 30 nm device

| Design Parameters | Values |
|---|---|
| Gate Oxide thickness (Tox) | 1nm |
| Gate length | 30 nm |
| Substrate Doping (N-type) | 1e+15 |
| Source/ Drain Doping (P-type) | 2e+20 |

To design the geometry of 32nm DG MOSFET Visual TCAD tool is used which is a device simulation tool. The geometry of DG MOSFET is shown in fig 5.

## VI. SIMULATION AND RESULTS

In this work we had designed a symmetric DG-MOSFET on Visual TCAD simulator. The obtained current–voltage (I–V) characteristics of a 30-nm gate length device are shown in Fig. 10 (a and b).

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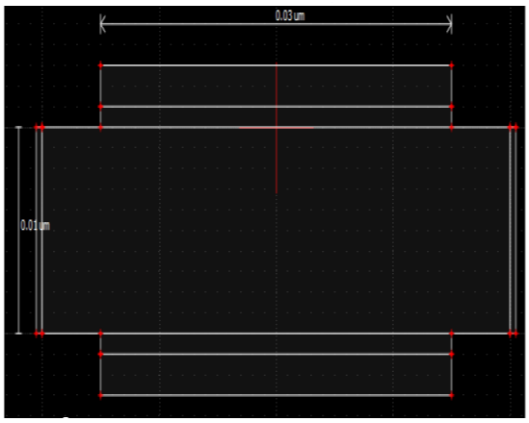


Fig 5. Geometry of 30nm DG MOSFET

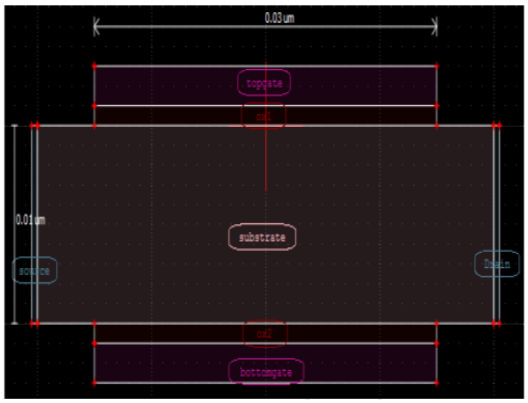


Fig 6. Structure of a DG MOSFET with all regions with material

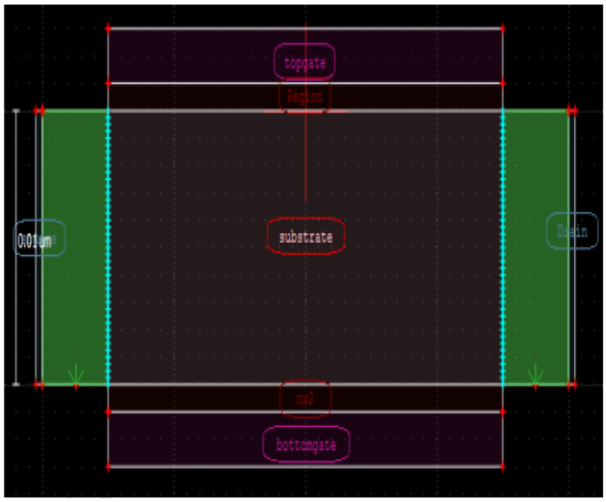


Fig 7. Doping Profile structure view

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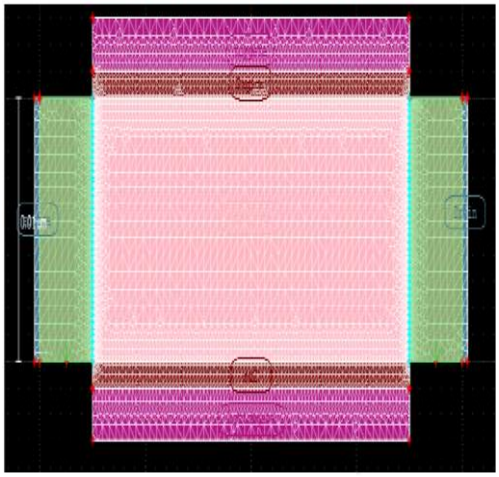

Fig 8. Meshing of DG MOSFET

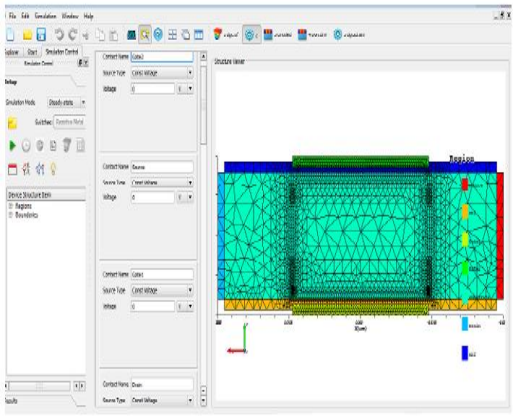

Fig 9. Simulation of DG MOSFET

The simulation is done and threshold voltage, Ion is observed.

### Threshold Voltage ($V_{TH}$)

Threshold voltage of the device is an important parameter which decides the device performance. The value of gate to source voltage (Vgs) for which sufficient amount of mobile electrons accumulates in the channel region so that a conducting channel is formed is called the threshold voltage. Table 3 shows the value of threshold voltage for the designed DG-MOSFET.

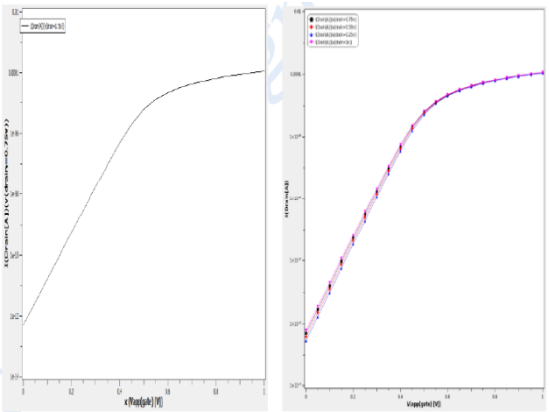

Fig 10 (a). DGMOSFET Simulation transfer characteristics Plots

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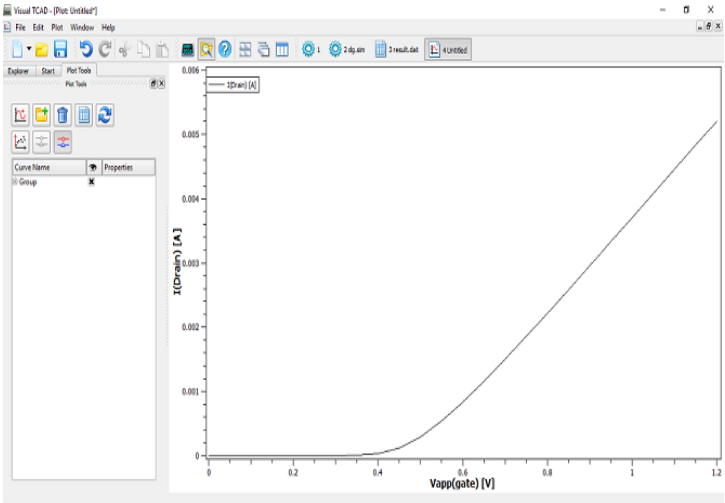


Fig 10(b). DG - MOSFET Simulation transfer characteristics Plots

**Drive Current (Ion)**

ON-State current, decides the driving capability of the device [16]. It is defined as drain to source current when Vgs=Vdd and Vds= Vdd. The drive current for the designed DG-MOSFET is shown in table 3.

**Drain Leakage Current (Ioff)**

It is defined as drain to source current when Vgs=0 and Vds= Vdd. MOSFET's drain leakage current or off-state current (Ioff) is the drain current when no gate voltage is applied. This off-state current is influenced by several other parameters such as channel physical dimensions, source/drain junction depth, thickness of gate oxide, channel/surface doping profile and supply voltage (Vdd).
As device dimensions are shrinking, leakage currents are becoming as one of the major parameter which needs more attention. In long-channel devices off-state current mainly due to leakage from the drain-well and well-substrate reverse-bias p-n junctions [16].

Ion/Ioff Ratio
The ratio of total drive current (ON state current) to the leakage current (OFF state current) is an important figure of merit [16].

$$\text{On}/_{\text{Off}}\ \text{Ratio} = \log_{10}\left[\frac{I_{on}}{I_{off}}\right] \qquad (3)$$

Table III: Simulation result of 30 nm DG MOSFET

| **Parameters** | **Value** |
|---|---|
| VDD | 1V |
| Threshold Voltage ($V_{TH}$) | 0.4 V |
| Drive current (Ion) | 3.708 mA |
| Leakage current (Ioff) | 23.6 pA |
| Ion/Ioff Ratio | 8.19 |
| DIBL | 2.5 |

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## VII. CONCLUSION

In this paper, we have analyzed and simulated the DG MOSFET by the help of Visual TCAD Tool. We have also thoroughly examined the short channel effects like Sub-threshold effect, DIBL. The results show that DGMOSFET have better results than conventional MOSFET. From the above discussions we conclude that as we scale down the devices, threshold voltage of the device decreases, to adjust the threshold voltage and other short channel effects within the permissible limits we can do channel engineering.

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