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# Power Quality Improvement using Canonical Switching Cell Converter Fed BLDC motor drive

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**Abstract**: Power factor correction (PFC) methods shapes the input current to maximise the real power from the supply mains. And they are also employed in present power supplies to comply with regulatory requirements. The rectifier circuits with power factor correction generally employs boost converters and as a result the output voltage becomes limited. To expand the controlled voltage range, buck-boost or Cuk converter types should be utilized. The converter which is advantageous over other converters must be utilised. Here the 'canonical switching cell' (CSC) converter is employed and it is advantageous over other converters. In this paper, the design and simulation of a reduced sensor based CSC converter fed brushless dc motor (BLDCM) drive for low-power household applications is discussed. The BLDCM is electronically commutated for reduced switching losses in voltage source inverter (VSI) due to low-frequency switching. By varying the dc-bus voltage of VSI, the speed of BLDCM is controlled. A front-end CSC converter operating in discontinuous inductor current mode (DICM) is used for dc-bus voltage control with unity power factor at ac mains, then voltage follower method can be effectively used. Since voltage follower method is used for the control, only one voltage sensor is needed which is advantageous. And also it is a cost-effective method. From the simulation analysis it is observed that the THD is improved drastically by employing this converter and the analysis of the circuit is also performed.

**Keywords**: Brushless dc motor (BLDCM), canonical switching cell (CSC) converter discontinuous inductor current mode (DICM), power factor correction (PFC).

## I. INTRODUCTION

The brushless dc motors (BLDCM) are mostly preferred due to their advantages over the other motors. It is also known as an electronically commutated motor (ECM) since an electronic commutation based on rotor position via a three-phase voltage source inverter (VSI). Therefore, the problems associated with brushes, such as sparking and wear and tear of the commutator assembly are eliminated. The BLDC motor is widely used in applications including appliances, automotive, aerospace, consumer, medical, automated industrial equipment and instrumentation.
The BLDC motor is electrically commutated by power switches instead of brushes. Compared with a brushed DC motor or an induction motor, the BLDC motor has many advantages:

- Higher efficiency and reliability.
- Lower acoustic noise.
- Smaller and lighter.
- Greater dynamic response.
- Better speed versus torque characteristics.
- Higher speed range.
- Longer life.

BLDC motor is a trapezoidal permanent magnet synchronous motor. The air gap flux is constant as permanent magnet is employed. The stator has concentrated windings and rotor has wide pole arc. The constructional features cause the induced voltage to have a trapezoidal shape. Also, the stator and rotor fields are stationary with respect to each other. The main disadvantage of this motor is that it is costlier compared to other motors and the construction is complex.
A motor drive system normally consists of a power circuit, a motor and a control unit. For a BLDC motor drive, the power circuit consists of a Diode Bridge Rectifier, a DC-DC converter [1] and a VSI. The power electronic circuits increase total harmonic distortion (THD) and power factor of the system. Therefore power factor correction (PFC) is required to reduce distortions in line current. It uses a dc–dc converter topology, for e.g. buck, boost, buck–boost, fly back, forward, push–pull, Cuk, Luo, SEPIC, Zeta etc.to obtain unity power factor with improved performance, such as reduction of ac mains current harmonics, reduction of acoustic noise and electromagnetic pollution, maximum efficiency, utilisation of the full input voltage range etc.

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A conventional scheme of BLDCM drive fed by an uncontrolled rectifier and a dc-link capacitor followed by a three-phase pulse width modulation (PWM)-based VSI is used for feeding the BLDCM. This type of scheme draws peaky, harmonic rich current from the supply and leads to a high value of total harmonic distortion (THD) of supply current and very low power factor at ac mains as shown in fig 1. A very high THD of supply current of 65.3% and a very poor power factor of 0.72 is achieved which is not acceptable by International Electro-technical Commission (IEC) 61000-3-2[2]. The increasing preference of BLDC motors for numerous low-power applications has raised power quality concern in customers. Therefore the drive systems having inherent power factor correction (PFC) are more in demand and PFC converters have become preferred features of new applications. A front-end PFC converter is used after the diode bridge rectifier (DBR) for improving the quality of power and achieving a near unity power factor at ac mains.

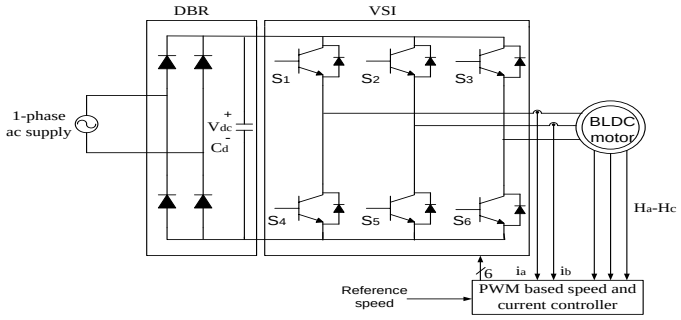


Fig 1. Conventional DBR-fed BLDCM drive.

Many topologies of a PFC-based BLDCM drives [3] are present. In PFC buck converter, the output voltage is always lower than the input voltage, therefore the voltage control range for feeding BLDC motor is very limited and it further reduces for a lower value of supply voltage. Moreover, for a PFC boost converter, the output voltage is always higher than input voltage and becomes relatively much higher for high value of supply voltage. A boost PFC converter has been the most popular configuration for feeding BLDCM drive [4], [5] &[6] as shown in fig 2. A constant dc-link voltage is maintained at the dc-link capacitor and a PWM-based VSI is used for the speed control. Hence, the switching losses in VSI are very high due to high switching PWM signals and require huge amount of sensing for its operation. Therefore, the controls of BLDC motor fed by PFC buck or boost converter by controlling the DC link voltage is difficult. Hence, PFC buck-boost or Cuk or CSC converters with variable dc-link voltage for speed control are employed.

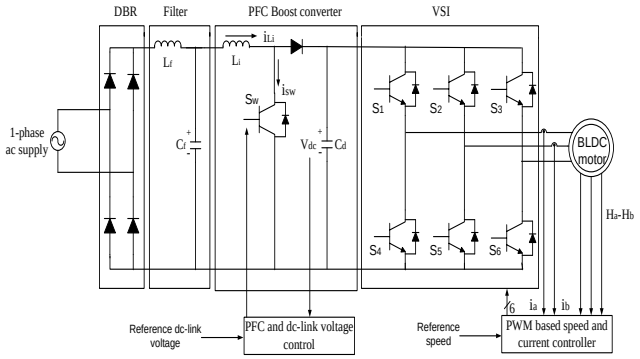


Fig 2. A conventional PFC boost converter-fed BLDCM drive.

Another configuration is the active rectifier-based BLDC motor drive requires complex control and is suitable for higher power applications. Various configurations are present with reduced parts for PFC operation [7], however it uses PWM-based VSI, so the switching losses are high. A buck chopper operating as a front-end converter for feeding a BLDC motor drive. It also has higher switching losses associated with it due to high-frequency switching.

Another topology is a PFC Cuk Converter-Fed BLDC Motor Drive. The speed control in this topology is done through voltage follower method, so it requires only one sensor which an advantage. The disadvantage is the number of components used in this topology is more. So, this makes the drive bulkier as well as costlier.
A configuration of boost half bridge PFC-based BLDCM drive is advantageous that it uses VSI with four switches. This also requires a necessary PWM operation of VSI and PFC half bridge boost converter, which introduces high switching losses in the overall system. These switching losses are reduced by using a concept of variable dc-link

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voltage for speed control of BLDC motor. This utilizes the VSI to operate in low-frequency switching required for electronic commutation of BLDC motor, hence reduces the switching losses associated with it. The front-end buck boost [8]-[9], SEPIC, CSC [10]-[11], Cuk [12]-[13], Luo [14] converters feeding a BLDC motor using a variable voltage control but it has the disadvantage that two current sensors are employed in continuous conduction mode, whereas the number of sensors required is minimum when the converter is operating in discontinuous conduction mode.Another topology is the NI-BIBRED [15] (non-isolated boost integrated buck rectifier/ energy storage DC-DC) converter. In this topology also single sensor is employed, which is an advantage. But the number of components is more, making it bulkier.So .Canonical switching cell converter is selected since when compared to other converters it has minimum number of components. The converter is operated in discontinuous mode which makes it cost effective since only one sensor is employed.

## II. CSC CONVERTER FED BLDC MOTOR

The dc- dc converter used here is Canonical Switching Cell (CSC) converter. The main advantage of using this converter is that the number of sensors used is less when compared to other converters.

*A.* Model circuit diagram

A PFC converter [16]-[17] is used after the DBR for improving the quality of power and achieving a near unity power factor at ac mains. The converter used here is Canonical Switching Cell converter. The mode of operation of the CSC converter is a critical issue as it directly affects the cost of overall system. The two basic modes of operation of converter is continuous inductor current mode (CICM) and the discontinuous inductor current mode (DICM). A control of current multiplier is normally used for PFC converter operating in CICM and requires three sensors (2-V, 1-C) for the operation which is not cost-effective for low-power applications, whereas, a CSC converter operating in DICM [18] uses a voltage follower control which requires sensing of dc-link voltage for voltage control and inherent PFC is achieved at ac mains. This is the main advantage of the CSC converter circuit

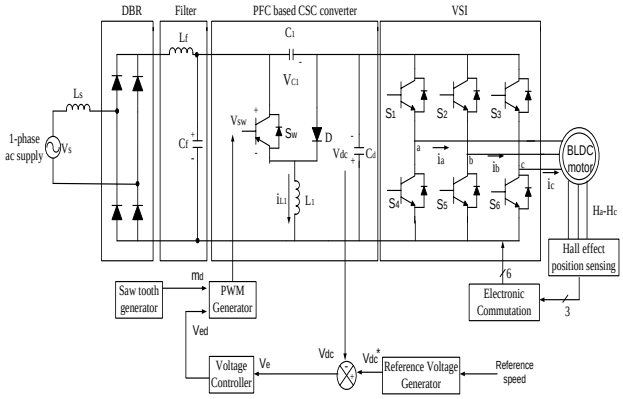


Fig. 3: The BLDCM drive using CSC converter.

Here the switch $S_w$ is triggered using the closed loop control as shown in the fig 3. And also a voltage sensor is only used over here. This dc link voltage and the voltage corresponding to the motor speed is fed to voltage controller. The output from this and the output from the saw tooth generator is fed to the PWM generator is fed to the switch to trigger it.

## III.MODES OF OPERATION OF CSC CONVERTER:

There are 3 modes of operation as given below:

Mode I: Here when switch is turned ON, the energy from the supply and stored energy in the intermediate capacitor are transferred to inductor. In this process, the voltage across the intermediate capacitor reduces, while inductor current and dc-link voltage are increased, the designed value of intermediate capacitor is large enough to hold enough energy such that the voltage across it does not become discontinuous.

Mode II: The switch is turned OFF in this mode of operation. The intermediate capacitor is charged through the supply current while inductor starts discharging hence voltage starts increasing, while current decreases in this mode of operation. Moreover, the voltage across the dc-link capacitor continues to increase due to discharging of inductor.

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Mode III: DCIM Mode of CSC Converter

This is the discontinuous conduction mode of operation as inductor is completely discharged and current becomes zero as shown in figure above. The voltage across intermediate capacitor continues to increase, while dc-link capacitor supplies the required energy to the load, hence starts decreasing.

The waveform of the CSC converter is given in the fig .4.

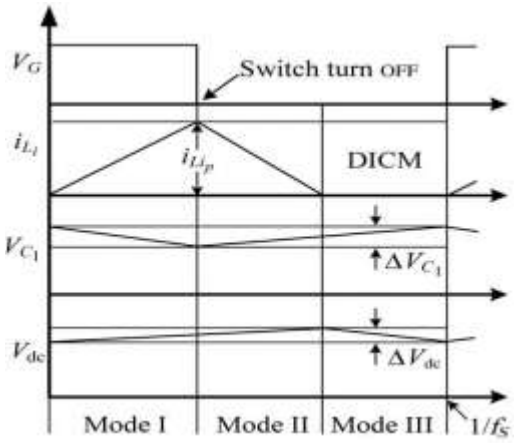


Fig.4. Waveform of the CSC converter.

## IV. DESIGN OF CSC CONVERTER:

The proposed BLDCM drive uses a PFC-based CSC converter operating in DICM. The BLDC motor is rated at 200 V and 250 W. The converter is designed for 400W, to accommodate losses in the inverter circuit. The PFC rectifier is fed from 220V, 50Hz 1Φ ac supply. The front-end PFC-based CSC converter BLDCM. The dc-link voltage has to be controlled from 50 V ($V_{dcmin}$ ) to 200 V ($V_{dcmax}$ ) with a nominal voltage of 200 V ($V_{dcn}$ ). For the supply voltage ($V_s$) of 220 V the design equations involved are:

The input voltage after the DBR is given by:

$$V_{in}=\frac{2\sqrt{2}}{\pi}V_s \qquad (1)$$

The nominal value of duty ratio corresponding to the nominal value of dc voltage selected is given by:

$$d_n = \frac{V_{dcn}}{V_{dcn} + V_{in}} \qquad (2)$$

The design of a CSC converter is very similar to a non-isolated Cuk converter with a single inductor and a switching cell which is a combination of a switch, diode, and an intermediate capacitor. The critical value of inductance to operate at boundary condition is given as:

$$L_{ic} = \frac{V_{in} d_{nom}}{2 I_{in} f_s} \qquad (3)$$

where$I_{in}$ is inductor current, and $f_s$ is switching frequency.

Now to operate this converter for PFC even at very low duty ratio, the value of inductor is taken around 1/10th of the critical value.

Hence, it is;

$$L_1 = L_{ic}/10 \qquad (4)$$

An intermediate capacitor $C_1$is designed for permitted ripple voltage $\Delta V_{C1}$ of across it and it is taken as 10% of $V_C$ [where $V_C$ is the voltage across intermediate capacitor].

The intermediate capacitor:

$$C_1 = \frac{V_{dcnom} d_{nom}}{f_s R_L \Delta V_{C1}} \qquad (5)$$

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where$R_L$ is the equivalent emulated load resistance which is given as ( $V_{dcn} * V_{dcn}$ )/$P$.
Now for a permitted ripple of 1% of the nominal dc-link voltage across the dc-link capacitor ($C_d$ ), the value of dc-link capacitor is calculated as:

$$C_d = \frac{I_d}{2\omega_L \Delta V_{dc}} \quad (6)$$

To avoid the reflection of high-order harmonics in supply system, a low-pass inductive-capacitive (LC) filter is designed whose maximum value, $C_{max}$ is calculated as:
The capacitance of filter:

$$C_{max} = \frac{I_{peak}}{\omega_L V_{peak}} \tan\theta \quad (7)$$

Now, the value of filter inductor is designed by considering the source impedance ($L_f$ ) of 4%–5% of the base impedance. Hence, the additional value of inductance required is given as:The filter inductance:

$$L_f = L_{req} + L_s = \frac{1}{4\pi^2 f_c^2 C_f} \quad (8)$$

A. Design of BLDC motor:
The BLDC motor[19]-[22] is designed for output power ($P_{out}$ ) of 250W with rated speed of 1900rpm and rated torque of 1.3Nm.
Let the efficiency of motor be 95% with 5% loss.
Then input power,$P_{in}$ = $P_{out}$ / Efficiency.
= 250/.95
= 263.157 W.
To find viscous damping, B:
Viscous power = 4% of input power.
$T_B\omega$ = (4/100) x 263.157
(B $\omega$ ) $\omega$ = 10.52
B = 2.65x$10^{-4}$ Nms.
To find moment of inertia, J:
Assuming time period, $t_1$ and $t_2$ to be 1.1 and 1 sec each. And speeds $N_1$ and $N_2$ to be 1500 and 1000 rpm respectively. Then,
J =-B($t_1$ -$t_2$ )/ln($N_1$ /$N_2$ )
=-2.65x$10^{-4}$(.1)/ ln(1500/1000)
J =6.53x $10^{-5}$kg $m^2$.

## V. CONTROL OF PFC CSC CONVERTER FED BLDC MOTOR:

The control of the PFC CSC converter fed BLDC motor drive is classified into two parts as follows.

A. Control of Front-End PFC Converter:
The control of the front-end PFC converter generates the PWM pulses for the PFC converter $switch$ ($S_w$)for dc link voltage control with PFC operation. A single voltage control loop(Voltage follower approach) is utilized for the PFC CSC converter operating in DICM. A reference DC link voltage ($V_{dc}$*) is generated as,

$$V_{dc}^* = k_v \omega^* \quad (9)$$

where$k_v$ is motor's voltage constant and $\omega^*$is reference speed.
Reference DC link voltage ($V_{dc}$*) is compared with sensed DC link voltage ($V_{dc}$) to generate voltage error signal ($V_e$) given as,

$$V_e(k) = V_{dc}^*(k) - V_{dc}(k) \quad (10)$$

where k represents the $k^{th}$sampling instant.
This error voltage signal ($V_e$) is given to the voltage PI controller to generate a controlled output voltage ($V_{ee}$) as,

$$V_{ee}(k) = V_{ee}(k-1) + k_p\{V_e(k) - V_e(k-I)\} + k_i V_e(k) \quad (11)$$

where$k_p$ and $k_i$ are proportional and integral gains of the voltage PI controller.

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Finally, output of voltage controller is compared with a high frequency saw-tooth signal (md) to generate the PWM pulses as,

$$\text{if} m_d(\text{t}) < V_{cc}\ (\text{t}) \text{ then } S_w = \text{'ON'} \quad (12)$$

$$\text{if} m_d(\text{t}) > V_{cc}\ (\text{t}) \text{ then } S_w = \text{'OFF'} \quad (13)$$

where $S_w$ represent the switching signal to the switch of PFC converter[23]-[24].

*B.* Control of BLDC Motor: Electronic Commutation:

An electronic commutation of the BLDC motor includes the proper switching of VSI in such a way that a symmetrical DC current is drawn from the DC link capacitor for 120 degrees and placed symmetrically at the centre of each phase. A rotor position on a span of 60 degrees is required for electronic commutation; which is sensed by Hall Effect position sensors. The conduction states of two switches ($S_1$ and $S_4$) are shown in fig. 5. A line current $i_{ab}$ is drawn from the DC link capacitor which magnitude depends on the applied DC link voltage ($V_{dc}$), back emfs ($e_{an}$ and $e_{bn}$), resistance ($R_a$ and $R_b$) and self and mutual inductance ($L_a$ , $L_b$ and M) of the stator windings.

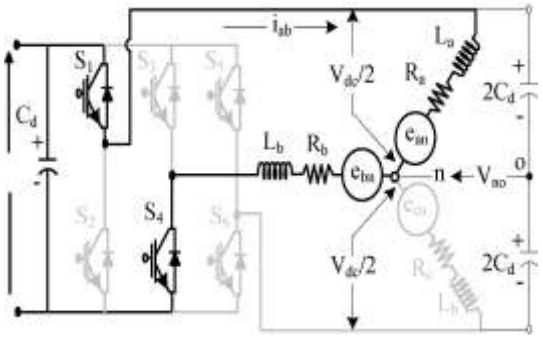


Fig. 5. A VSI feeding a BLDC motor.

Table-I shows the governing the different switching states of the VSI feeding a BLDC motor based on the Hall Effect position signals ($H_a$-$H_C$).

TABLE I PERFORMANCE OF CSC CONVERTER FED BLDC MOTOR DRIVE UNDER SPEED CONTROL.

| Ø(degrees) | Hall Signals | | | Switching states | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | $H_a$ | $H_b$ | $H_c$ | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ |
| NA | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0-60 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 60-120 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 120-180 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 180-240 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 240-300 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 300-360 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| NA | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

According to these switching signals the corresponding switches of the VSI will be turned ON and the corresponding winding will be excited. Thus the BLDC motor will be rotated. This is how the BLDC motor is rotated using the electronic commutation.

The electronic commutation is advantageous over mechanical commutators as the brushes and commutators are eliminated instead power electronic switches are employed. So proper maintenance is not required here. And the efficiency is also improved in the electronic commutation. But separate rotor position sensors are required for the closed loop control of the BLDC motor. But now sensorless based control is also present which is more advantageous.

## VI. SIMULATION RESULTS

Simulation study is used to analyse the circuit under various operating conditions and also it is used to design various circuit parameters in an acceptable form without causing any damage to practical hardware set up. This may include varying supply, load conditions, component values etc. If hardware circuits are used for analyzing operation under

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various conditions, components may get damaged. Hence it is feasible to carry out simulation study. But losses under practical conditions cannot be evaluated in this study as components are considered to be ideal in performing the simulation analysis.

A. Simulation of open loop CSC converter:
The open circuit CSC converter is simulated and the simulation model is given below.

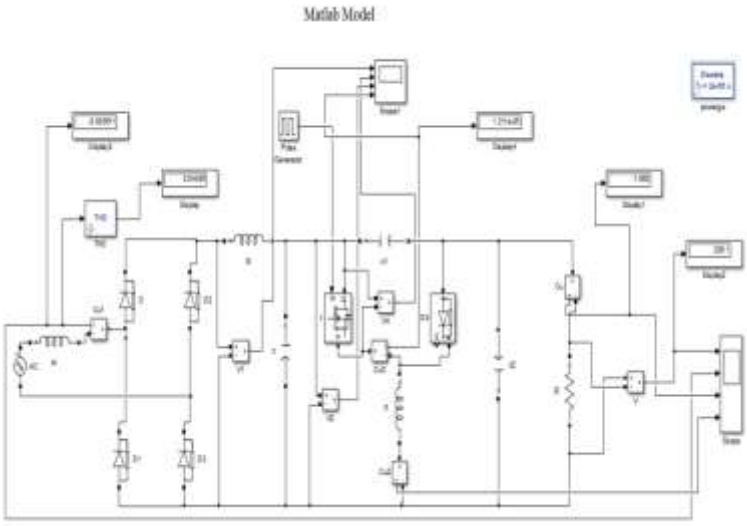


Fig.6 Simulink model of open loop CSC converter.

The converter is designed for 200Vas the nominal voltage and the simulation output of around 206V is obtained. The average output current of 1.95A.The power output of 407.1 W is obtained. The matlab model is shown in fig.6.

The output voltage, output current and the input current waveforms are shown below in fig.7. The output voltage obtained is 206V and the converter is designed for 200 V. The output voltage is obtained across a load resistor of 100 Ω .And also the output current that flows across the load resistor is also obtained.

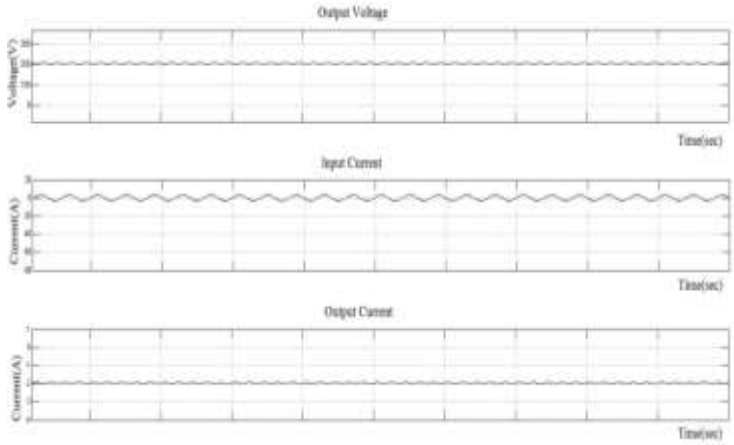


Fig 7 The output current, input current and output voltage of CSC converter.

The FFT analysis of the CSC converter is performed and THD of 2.95% is obtained.

The waveform of FFT analysis of the CSC converter is obtained. FFT analysis gives the harmonic spectrum which gives magnitude of each harmonic component as a percentage of the fundamental component. It also gives the THD of the waveform. From the above fig 8, it is clearly seen that the output waveform is distorted but it is nearly sinusoidal. And also the THD obtained is 2.95% which indicates the level of harmonics in the system is comparatively minimum. Since the obtained THD is less than 5% it is acceptable under the IEEE 519 standards.

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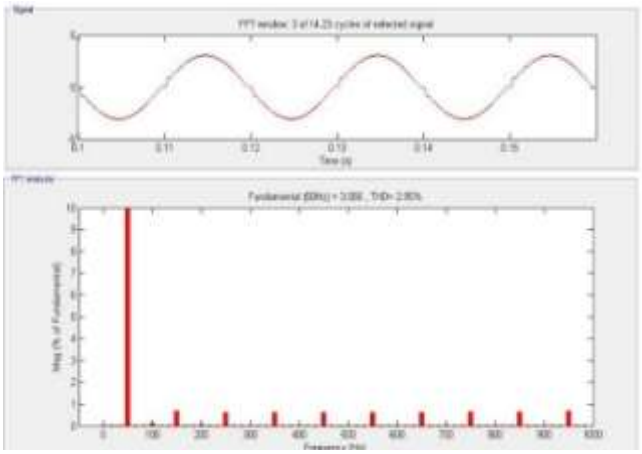

Fig. 8. FFT analysis of CSC converter (open loop).

B. Simulation of closed loop CSC converter:

The closed loop simulation of the CSC converter is performed and is shown in the fig. 9 below. The converter is designed for 200Vas the nominal voltage and the simulation output of around 200.2V is obtained.

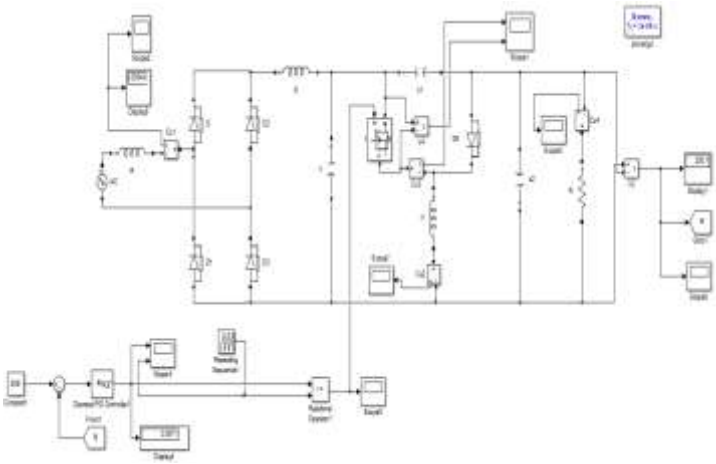

Fig. 9 Simulink model of closed loop CSC converter.

The output voltage obtained is 200.2V and the converter is designed for 200 V is shown in the fig.10. The output current obtained is about 2.4A. The output is obtained across a load resistor of 100 Ω .

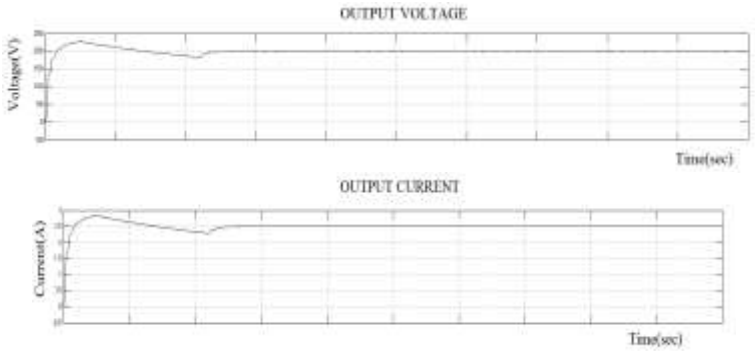


Fig. 10 Output voltage and current waveform of closed loop CSC converter.

The FFT analysis of the CSC converter is performed for the closed loop is as shown in the fig 11. It also gives the THD of the waveform and it is clearly seen that the output waveform is distorted. And also the THD obtained is 2.49% which indicates the level of harmonics in the system is comparatively minimum and is acceptable under the IEEE 519 standards.

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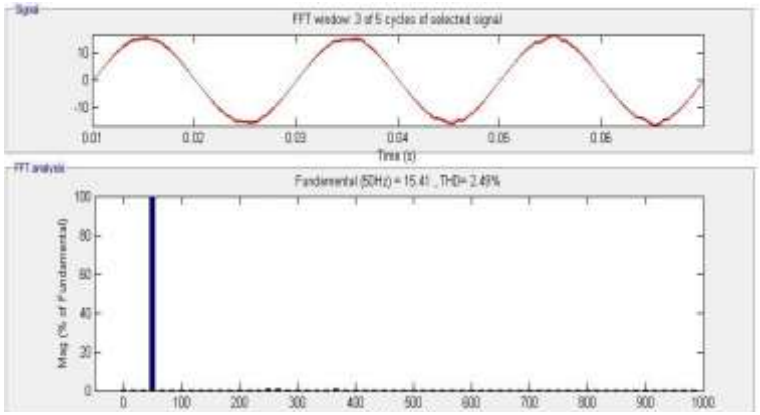


Fig. 11. FFT analysis of CSC converter (closed loop).

*C.* Simulation model of CSC converter fed BLDC motor:

The simulation model of the CSC converter fed BLDC motor drive is developed with a closed loop control and is shown in the fig 12 below.

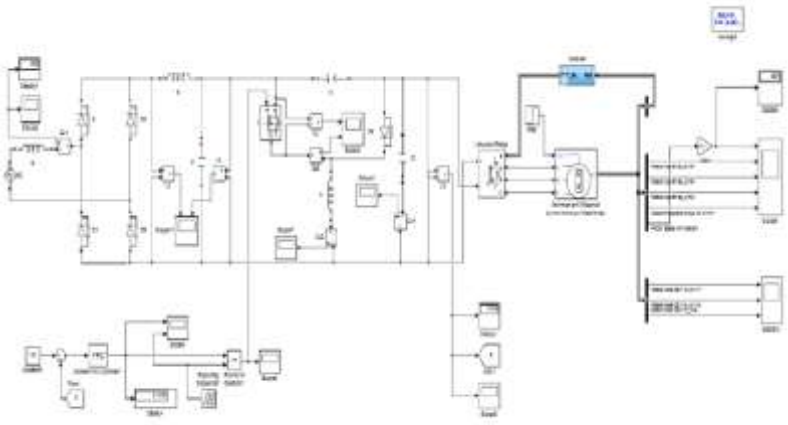

Fig. 12. Simulation model of CSC converter fed BLDC motor.

The decoder circuit model is also set up as shown in the fig 13 below which act as the output from the hall effect sensors.

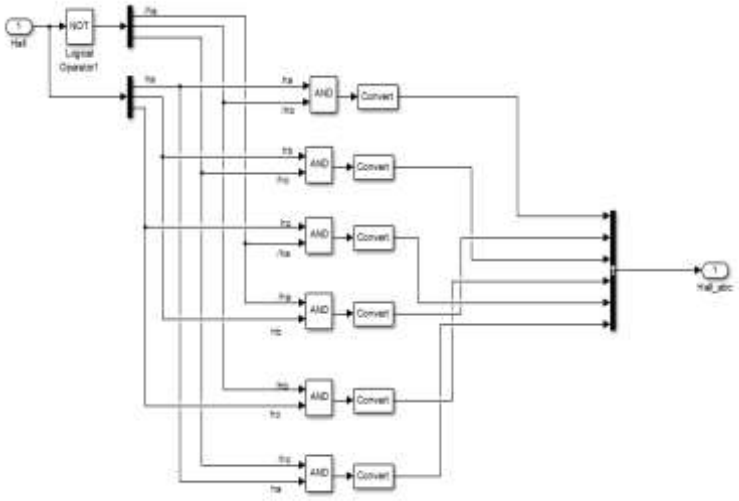


Fig.13. Decoder circuit model.

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The motor output speed, current and torque is obtained as shown in the fig 14 below. The speed of motor obtained is 1902 rpm which matches with the designed value. The motor torque obtained is 1.4 Nm.

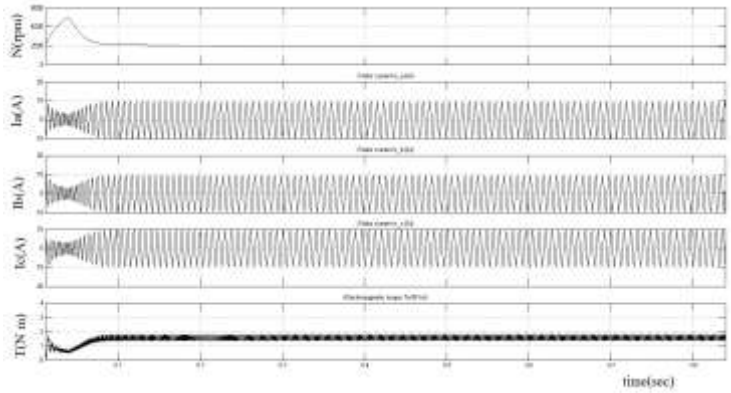


Fig. 14 Motor speed, current and torque waveform of CSC converter fed BLDC motor.

The motor back emf obtained is as shown in the fig. 15. The obtained shape of the waveform is trapezoidal which depicts the characteristics of the BLDC motor.

Also, we have,

The output power, P $= 2\pi NT/60$

$=2*3.14*1902*1.3/60 \quad =255.25W.$

The output power obtained is 255.25 W.

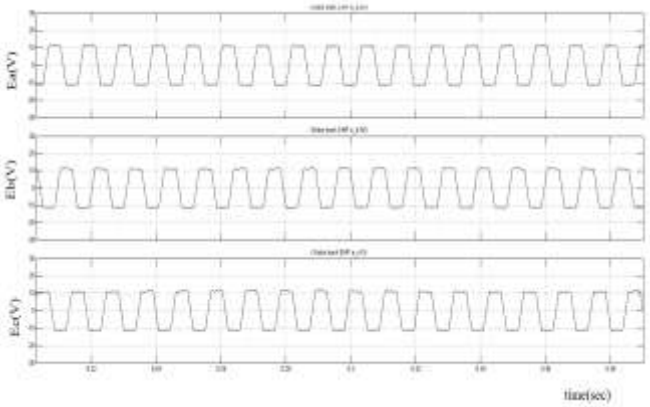


Fig.15 Emf waveform obtained of CSC converter fed BLDC motor.

The output voltage obtained is 197 V when the reference voltage given is 200V. Input current and inductor current waveform is also shown in the fig 16. The input current obtained is 2.1A.

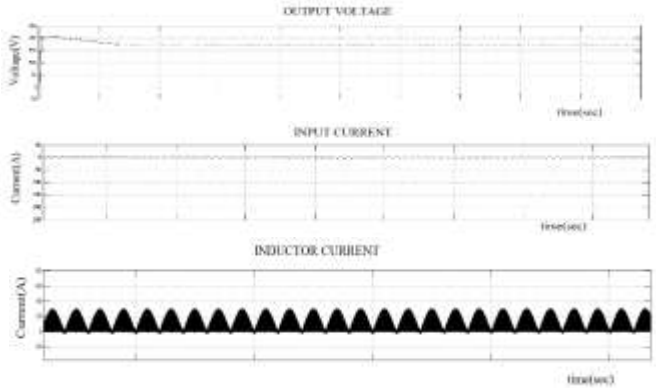


Fig.16 Output voltage, input current and inductor current waveform of CSC converter fed BLDC motor.

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The THD obtained for the input current is 3.55% and the FFT analysis. The inductor current waveform is also shown which depicts the discontinuous inductor current mode of the CSC converter.The FFT analysis of the CSC converter fed BLDC motor is performed and the waveform as shown in fig. 17. FFT analysis gives the harmonic spectrum which gives magnitude of each harmonic component as a percentage of the fundamental component. It also gives the THD of the waveform. From the fig.17, it is clearly seen that the output waveform is distorted but it is nearly sinusoidal. And also the THD obtained is 3.55% which indicates the level of harmonics in the system is comparatively minimum. It is also acceptable under the IEEE 519 standards.

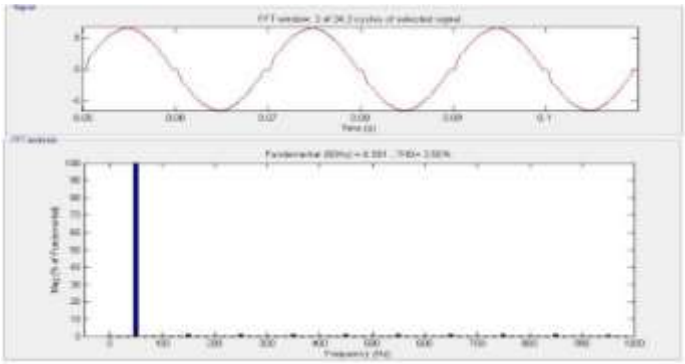

Fig. 17. FFT analysis of CSC converter fed BLDC motor.

*D.* Comparative study of the DBR fed BLDC motor and a PFC CSC converter fed BLDC motor:

A comparative study is performed with the DBR fed BLDC motor and a PFC converter ie, here it is CSC converter fed BLDC motor. The matlab model of DBR fed BLDC motor is shown in fig 18 below.

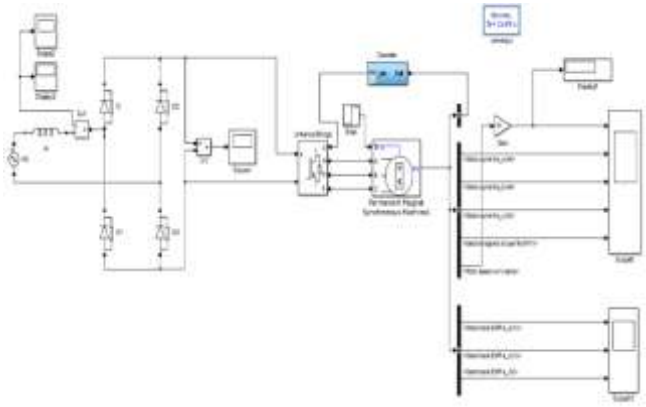

Fig. 18. Matlab model of DBR fed BLDC motor.

The FFT analysis of the DBR fed BLDC motor is performed and the waveform as shown in fig. 19. The THD obtained is 55.34% which is not accepted by the IEEE 519 standards and it is highly distorted.

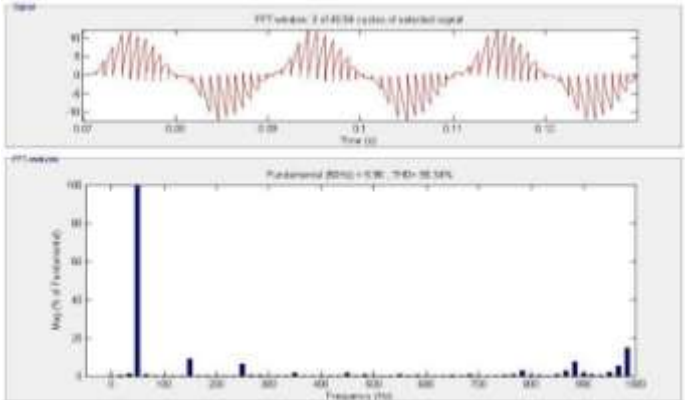

Fig. 19. FFT analysis of CSC converter fed BLDC motor.

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The FFT analysis of CSC converter fed BLDC motor shows that the THD is just 3.55% where as for the DBR fed BLDC motor it is 55.34%. Thus by the comparative study we can conclude that by incorporating the PFC converters the power quality can be improved to a great extent, such that the THD can be brought below 5% and the distortion can be reduced, thus power factor can be improved.

*E.* Performance analysis of the CSC converter fed BLDC motor:
For different reference voltage simulation study is being conducted which clearly depicts the action of the closed loop as shown in the table.II. So, according to the reference voltage which corresponds to the speed by which we have to rotate the BLDC motor, the motor can be operated successfully. Since output voltage obtained is constant to the reference voltage applied.

Table II: COMPARISON OF REFERENCE AND OUTPUT VOLTAGE FOR THE CSC CONVERTER.

| Reference voltage applied(V) | Output voltage obtained (V) |
|---|---|
| 180 | 181 |
| 200 | 200 |
| 220 | 219 |
| 250 | 251 |

*F.* Performance of the CSC converter fed BLDC motor under varying supply voltage:
The performance of the CSC converter for varying supply voltage is analysed and is shown in the table III below. And it is found that even though the supply voltage is varied the output voltage is maintained constant according to the reference voltage given. Here the reference voltage applied is 200V. This performance also indicates the proper working of the closed loop.

Table III PERFORMANCE OF CSC CONVERTER FED BLDC MOTOR FOR VARYING SUPPLY VOLTAGE

| Supply Voltage(V) | Converter output voltage(V) |
|---|---|
| 220 | 201 |
| 200 | 200 |
| 180 | 200 |
| 150 | 199 |

The Simulation parameters of the CSC converter fed BLDC motor drive is given in the table IV below:

TABLE IV SIMULATION PARAMETERS.

| Component | Value |
|---|---|
| $V_{ac}$ | 220V, 50 Hz |
| $L_1$ | 0.055mH |
| $C_1$ | 5μF |
| $C_f$ | 1μF |
| $L_f$ | 3mH |
| $C_d$ | 10mF |
| $L_s$ | 0.5mH |
| D | 0.5 |

## VII. CONCLUSION

As per the review, PFC-based CSC converter-fed BLDCM drive has been explained for targeting low-power household applications. A variable voltage of dc bus has been used for controlling the speed of BLDCM which eventually has given the freedom to operate VSI in low-frequency switching mode for reduced switching losses. A front-end CSC converter operating in DICM has been used for dual objectives of dc-link voltage control and achieving a unity power factor at ac mains. The performance of the proposed drive has been found quite well for its operation at variation of speed over a wide range and the Converter is advantageous compared to other converters.The closed loop circuit CSC converter is simulated and the simulation model is explained. The converter is designed for 200V as the nominal voltage and the simulation output of around 201V is obtained. The output current obtained is 2A.And the THD is

obtained as2.94%.The CSC converter fed BLDC motor is simulated. The output power obtained is 255.25W and the motor speed obtained is 1902rpm. The THD is 3.55% which is acceptable under IEEE 519 standards.

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## BIOGRAPHY

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