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Single phase active front end rectifier system employed in three phase variable frequency drive

Shruti K K[1], Valsalan T [2], Poorani S [3]

Student, Electrical &Electronics Department, Govt. College of Engineering, Kannur, Kerala, India [1]

Research Scholar, Karpagam University, Coimbatore, Tamil Nadu, India [2]

Professor, Karpagam University, Coimbatore, Tamil Nadu, India [3]

Abstract: In many countries single-phase power is used for rural power distribution which limits the use of three phase variable frequency drives (VFDs). Three-phase VFDs are often required to operate from a single-phase ac source. The aim of this project is to design and implement a circuit that can be used for three phase VFDs operating from single phase ac source. Powering up of three-phase VFDs from single-phase ac source requires addressing many issues: higher RMS value of input diode current, higher ripple voltage across the dc bus capacitor, higher peak input current, higher input current distortion, lower power factor and poor system efficiency. All of these lead to severe derating of VFDs for single-phase applications. A new low-cost single-phase active circuit based on injecting current into the midpoint of the dc bus employing only one bidirectional switch can be used to address the aforementioned problems. This method shows that VFDs need not be derated to achieve rated output power.

Keywords: Drives for rural applications, single-phase active filter, single-phase input drives, single-phase-to-three-phase converter.

I. INTRODUCTION

A new trend to adjust the speed of a three phase induction motor is by using variable frequency drives. Generally, an induction motor can run at its rated speed when it is connected directly to the rated supply voltage. However, many applications need variable speed operations. In most of the applications the input power is directly proportional to the cube of motor speed. In certain applications like induction motor-based centrifugal pump, a speed reduction of 20% results in an energy saving of approximately 50%. The two important constraints in today's modern era are driving and controlling the induction motor efficiently. With the new innovations developed in the semiconductor fabrication technology, the size and the price of semiconductors have drastically gone down, which means that the end user can replace an energy inefficient mechanical motor drive and control system using a Variable Frequency Drives (VFD). The VFD not only controls the motor speed, but can improve the motor's dynamic and steady state characteristics as well. In addition, the VFD can reduce the system's average energy consumption. Rural irrigation used for water pumping and pumps used for extracting oil from deep wells are some of the typical applications that require powering up three-phase(VFDs) from single-phase ac source. In remote locations, three phase ac power may not be available. Many VFD manufacturer impose restrictions on the rating of the VFD for use with a single-phase ac source. Important concerns while operating a three-phase VFD from a single-phase ac source are that the RMS value of the input ac is at least twice that when a three-phase supply is used for a given load. The input diodes have to handle the higher current demand for a given load. Also in a diode rectifier with a large dc bus capacitor, the current flows only when the instantaneous value of the input voltage is higher than the dc bus voltage, the current flow is intermittent and has a significant peak when the input is a single-phase ac source. The higher peak current through the rectifier diode causes undesirable thermal stress in the diodes and may lead to premature failure. Another issue is that higher input current affects the input ac power terminal blocks. Even if the diodes are able to handle the higher current, the terminal blocks may not be rated to handle the higher RMS current continually. Input current harmonic distortion is also high when single-phase input is used to power three-phase inverters. Higher harmonic content is associated with a lower input power factor and poor system efficiency. Single-phase ac supply results in higher ripple voltage across the dc bus. Higher ripple voltage translates to higher ripple current through the capacitor and more heating of the capacitor. The inverter is typically derated to handle the higher capacitor ripple current. Hence, there is a need to address all these issues. For this, a non-regenerative circuit is added in between the rectifier and inverter to enable three phase VFD use from a single ac supply. There are many techniques employed to address the issues faced when single-phase ac supply is used to power three-phase VFDs [1]–[7]. The conventional active boost topology used for powering VFDs has some disadvantages. The main drawback of voltage ripple is overcome by using interleaving of boost converters topology [2]. In [3],a bridgeless rectifier that has high power density employing coupled inductors is discussed. In such

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topologies, the boost inductor is on the input ac side. However, an important drawback of most bridgeless rectifiers is that they need high-speed fast-recovery diodes in the rectifier circuit, which makes them expensive. In [4], a dc bus midpoint is created using two capacitors in series.

One of the phases of the three-phase ac motor is also connected to the dc bus midpoint. The remaining two phases are connected as usual to two of the output phases of a typical output stage of a four-switch H-bridge topology. The topology of [4] is also inherently regenerative, which can be an important advantage in certain applications. The topology discussed in [5] uses the structure which is known as the B4 topology as its base. In [5] modifications to the base topology is suggested by adding extra switches to create three additional interconnection options for the motor windings, known as B4f, B4vf, and B4vfzin [5]. In two of these new variations (B4f and B4vfz), one needs to access the neutral point of the ac motor, which makes them impractical from the industrial application point of view. In addition, the extra switches make the topologies the same cost as a traditional six switch (B6) topology. Various versions of the base topology have been well exploited in [6] to result in interesting low-cost topologies. In all the topologies discussed in [4]–[6], one or more motor windings are connected to the input single-phase ac supply. The third phase is controlled in a pulse width-modulated manner to generate positive sequence voltages. Common-mode voltage and EMI conducted back into the source remain the major issues with the added drawback of requiring larger voltage ratings for the switches in the topology.

This paper presents a low-cost active solution that attempts to address the problems associated with the conventional methods of powering VFDs. Cost and size considerations are also given higher importance in this paper.

II. THREE PHASE VFD USING SINGLE PHASE AC SOURCE

The topology of non-regenerative single phase active front end circuit is shown in Fig. 1.

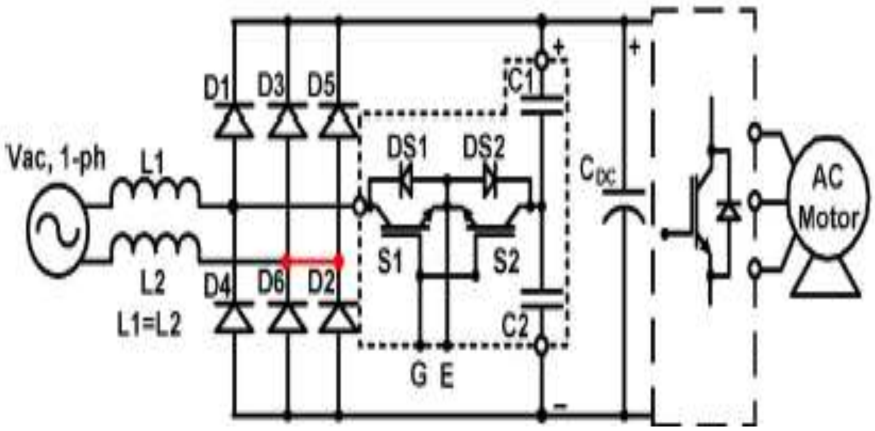


Fig.1 Non-regenerative single-phase active-front-end circuit

This is possible since the voltage is applied across the phase and the dc bus midpoint. The current flow is limited by an external inductor, which behaves similarly to a boost inductor boosting the main dc bus voltagewhen the switch is forced to turn off at the peak of input ac voltage. The boost inductor is large in size since the charging cycle occurs only twice every input cycle. The switching frequency is hence two times the supply frequency (100 Hz for a 50-Hzac source). Low switching frequency helps in avoiding the need to employ additional EMI filtering in the input. In figure 1, the components within the dotted box and the inductors L_1 and L_2 are external to the VFD. The dotted box can be thought of as an external add-on unit connected between one input terminal and the dc bus positive and negative terminals of the VFD, thus ensuring that there are no drive modifications. Two of the three legs of inputs are shorted to augment the corresponding diode conduction.

A. Principle of operation

A bi-directional switch made up of two switches S_1 and S_2 connected in a common emitter configuration is used to channel current from the ac source to the dc bus midpoint in a bi-directional manner. To ensure equal performance in each half of the input ac cycle, two inductors of the same value are used in between the ac source and the diode rectifier unit. Again, to ensure equal conduction, the filter capacitors forming the dc bus midpoint are also of same value and same voltage rating. The basic operation is described referring to the theoretical waveforms shown in figure 2. Two distinct modes of operation are identified, and the description of each mode will help in highlighting the features of the proposed topology.

Mode 1: Mode 1 starts when switch S_1 is turned on and current flows through S_1 and DS_2. This happens when the instantaneous line–line voltage is greater than the dc bus midpoint voltage. Current linearly increases and is limited by the inductance of the external inductor L_1. Current is seen to flow through L_1, S_1, DS_2, and filter capacitor C_2, and returns back through diode D_2, into the source via external inductor L_2, as shown in figure 3(a).

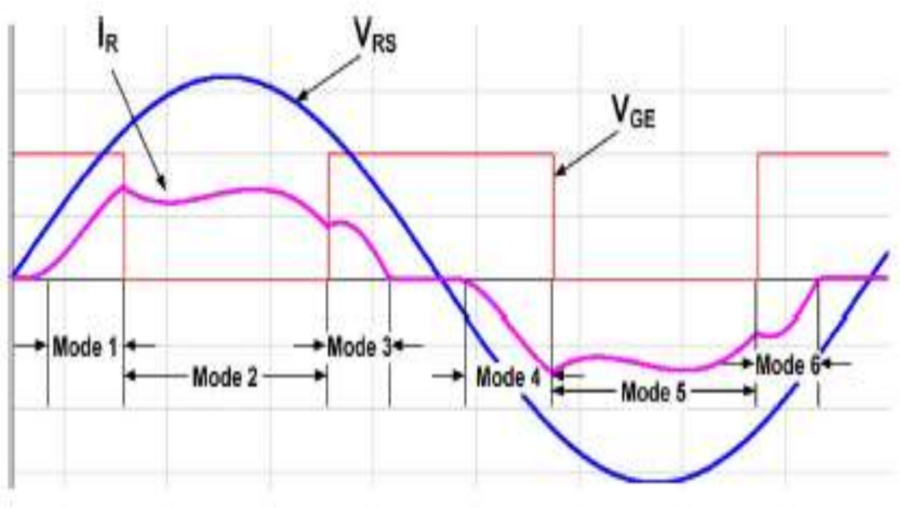


Fig.2 Typical waveforms at various points in the circuit

The equation for the flow of current through L_1 and L_2 during mode 1 is derived as follows.

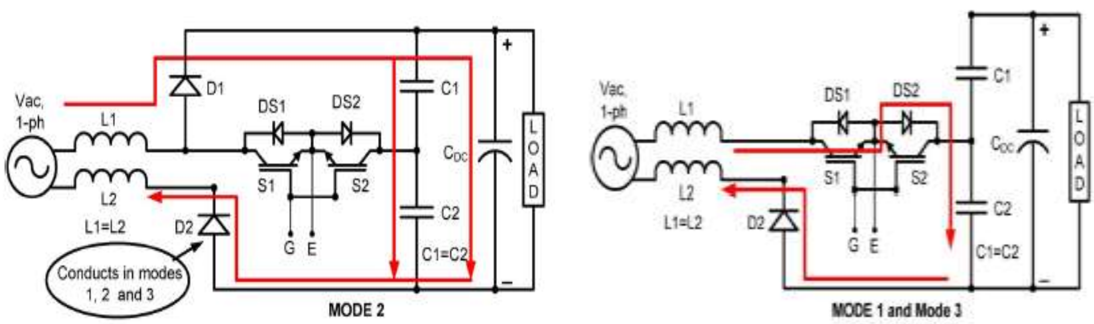
$$V_m \sin(\omega t) - \frac{V_{DC}}{2} = (L_1 + L_2)\frac{di}{dt}$$

$$i = \left(\frac{V_m}{\omega.(L_1+L_2)} \int_{\frac{\pi}{6}}^{t} \sin(\omega t)\, d(\omega t)\right) - \frac{V_{DC}}{2.\omega.(L_1+L_2)}.\left(\omega t - \frac{\pi}{6}\right)$$

$$i = \left(\frac{V_m}{\omega.(L_1+L_2)}\left(\frac{\sqrt{3}}{2} - \cos(\omega t)\right)\right) - \frac{V_{DC}}{2.\omega.(L_1+L_2)}.\left(\omega t - \frac{\pi}{6}\right) \quad \ldots\ldots\ldots\ldots\ldots..(1)$$

$$\frac{\pi}{6} \leq \omega t \geq \frac{\pi}{2}$$

At the end of mode 1, switch S_1 is deliberately turned off. The duration of mode 1 depends on the dc bus voltage.



(a) (b)

Fig.3 Equivalent circuit for (a) modes 1 and 3 (b) mode 2

The dc bus voltage is constantly monitored, and the pulse width corresponding to the duration of mode 1 is adjusted to maintain the desired dc bus voltage value. The ramification of limiting the duration of mode 1 is discussed in the following. Mode 1 is the charging duration. The longer the duration, the more energy is stored in the input ac inductor. During mode 1, the dc bus keeps discharging into the load since the main bus is not being charged in this mode. Consequently, the longer theduration of mode 1, the deeper is the sag of the dc bus voltage, for a given load condition.

When the switch S_1 is turned off at the end of mode 1, the energy stored in the inductor is transferred to the main dc bus. The longer the duration of mode 1, the more energy is stored in the inductor; therefore, when switch S_1 is turned off at the end of mode 1, the voltage becomes higher and the dc bus is charged. Increasing the duration of mode 1 causes a deeper sag and higher boost of the dc bus voltage. In other words, the peak-to peak ripple of the dc bus voltage increases. Hence, the duration of mode 1 cannot be arbitrarily increased. The duration of mode 1cannot be made very small either since the energy stored in the boost inductor reduces, and consequently, the dc bus voltage may not get boosted enough to support a given load condition.

By equating the current at the end of mode 1 to the peak value of the rated input current for a given power rating, one can limit the duration of mode 1 and, at the same time, calculate the value of the input inductor needed to achieve the desired operation. Going through this exercise yields a value for the input inductor, as given in (2). The total combined inductance of $L_1 + L_2$ is represented by L_{in} in the following derivation. Z_{pu} is the rated impedance of the system and is defined as the ratio of the rated line–neutral voltage to the rated input current.

$$L_m.\frac{di}{dt} = V_m\, sin(\omega t) - \frac{V_{DC}}{2}$$

$$Z_{p.u} = \frac{V_{LL}}{\sqrt{3}.I_L}$$

$$I_m = \frac{V_m}{\omega.L_{in}}\left(\frac{\sqrt{3}}{2}\right) - \left(\frac{V_{Dc}}{2.\omega.L_{in}}.\left(\frac{\pi}{3}\right)\right), at\ \omega t = \frac{\pi}{2}$$

$$Z_{in} \approx 0.211 Z_{pu} \ldots\ldots..(2)$$

Since Z_{in} is made up of two equal inductors L_1 and L_2, it can be said that each inductor needs to have an impedance of about 0.1 p.u. or 10% of the rated impedance of the load reflected onto the ac source.

Mode 2: The start of this mode occurs when switch S_1 is turned off. The current through the inductors L_1 and L_2 cannot stop instantaneously; therefore, the inductor current flows into diodeD_1, charges up the dc bus, supplies energy to the load, and returns back through diode D_2 into the source via inductor L_2. In other words, during mode 2, the energy in the two inductors is returned to the dc bus and is used up by the load, as shown in figure 3(b).

Mode 3:The start of mode 3 occurs when switch S_1 is turned on again toward the end of the first half-cycle of the input voltage, as shown in figure 3. The current is naturally coming down, indicating that the energy in the inductor is completely transferred to the dc bus. However, this natural drop off can be interrupted by turning on S_1 again. This forces the current to keep flowing beyond its natural zero point. It allows the increase in current flow duration, which helps improve the input power factor. The current flow through inductors L_1 and L_2 during mode 3 diverts the current from charging the main dc busand forces the current into the dc bus midpoint. This action reduces the peak-to-peak ripple of the dc bus. Modes 4, 5, and 6 are mirror images of modes 1, 2, and 3, respectively, repeated for the negative half of the ac supply.

B. Asymetrical conduction of rectifier diodes

The diode D2 carries current during modes 1, 2, and 3, whereas diode D1 carries current only during mode 2. Similarly, diode D5 carries current during modes 4, 5, and 6, whereas diode D4 carries current only during mode 5. Since, in most VFDs, the input section is a three-phase rectifier bridge with six diodes, it is prudent to employ the unused diode pair to assist diodes D2 and D5 during their conduction. This is achieved by shorting two of the input terminals so that diodes D6 and D2 are in parallel and diodes D5 and D3 are in parallel, as shown in Fig. 1.

C. Separation of filter capacitor from dc bus capacitor

This topology makes use of external capacitors that form the dc bus midpoint. Since these external capacitors carry only the ripple current, one need not use electrolytic capacitors. By separating the ripple carrying capacitor from the bulk electrolytic capacitors, there is room for optimization in size and cost. The selection of the value of the capacitor is defined by the energy stored in the boost inductor. This is the same energy that circulates between the boost inductor and each of the filter capacitor. In other words, the surge impedance of the inductor capacitor network should match the ratio of the peak voltage $V_m/2$ across the inductor–capacitor network formed by L_{in} and C_2 (or C_1) to the peak current through it I_m. The equation for selecting the capacitor is derived in the following.

$$Z_{surge} = \sqrt{\frac{L_{in}}{C_1}} = \frac{V_m}{2.I_m}$$

$$\sqrt{\frac{L_{in}}{C_1}} = \frac{\sqrt{3}.Z_{pu}}{2}$$

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$$C_1 = \frac{4}{3} \cdot \frac{L_{in}}{{Z_{pu}}^2}$$
$$Z_C = \frac{1}{\omega . C_1}$$
$$Z_C \approx 3.554\, Z_{pu} \dots \dots \dots \dots (3)$$

From the equation, it is evident that value of the capacitor is quite small compared with the main dc bus capacitor. In most practical cases, tests have shown that the filter capacitor is only 7%–8% of the main dc bus capacitor.

D. Control strategy of the converter

The load dc bus voltage is sensed and fed back into the controller where it is compared with a reference value. The error is fed into a proportional–integral (PI) controller with a limiter. The output from the first PI controller is compared with the switch current. These are compared and an error signal is generated which is further given to the next PI controller. The output of thisPI controller is treated as the actual duty-cycle control signal.

E. Design of the converter

The design of the converter consists of designing the input inductance and the dc bus capacitance. The specifications of the system are given in the table 1.

Table 1 Specifications of the system

Supply Voltage	$230V_{ac}$
Number of phases	1
Motor Rated Power	3Hp
Motor phases and Rated voltage	3-ph,415 V
Rated current	15 A

Based on the specifications discussed above, selection of inductor and capacitor is made as follows.

1) Inductor Selection

Based on the specifications listed in Table 1 and using equation, the value of energy storage inductor L_{in}, is given as shown below.

$$Z_{pu} = \frac{V_{LL}}{\sqrt{3}.I_L} = \frac{230}{(15).\sqrt{3}} = 8.85\ \Omega$$
$$Z_{in} \approx 0.211.Z_{pu} \approx 1.86\Omega$$
$$L_{in} = \frac{1.86}{2.\pi.50} = 5.94mH$$
$$L_1 = L_2 = \frac{L_{in}}{2} = 2.97mH \dots \dots \dots \dots . . (4)$$

2) Capacitor Selection

Similar to the procedure used for selecting the energy storage inductor, the filter capacitor is given in the following

$$Z_C \approx 3.554.Z_{pu} = 31.45\ \Omega$$
$$C_1 = C_2 = \frac{1}{\omega.Z_C} = 101.2\mu F \dots \dots \dots \dots \dots . (5)$$

In this chapter, the design and the control aspects of the converter is discussed.

III. SIMULATION

The Simulink results obtained in MATLAB are discussed here. The source current and dc link capacitor voltage of the conventional VFD is shown in figure 4.

The THD value of the source current is about 89.91 %. The FFT analysis of source current is shown in figure 5.

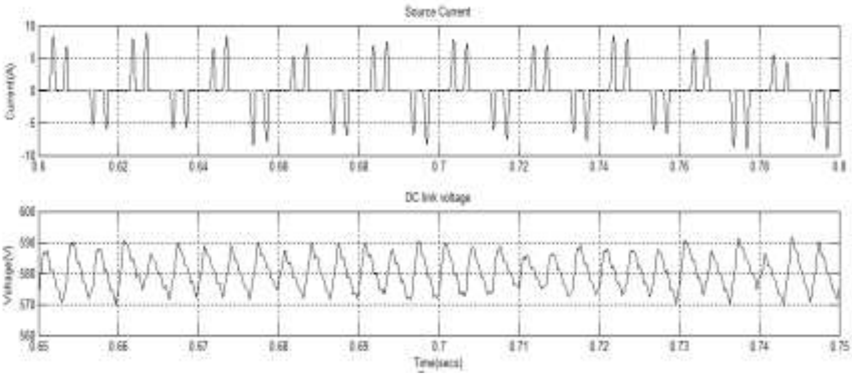

Fig 4 Source current and DC link voltage waveforms of the conventional VFD

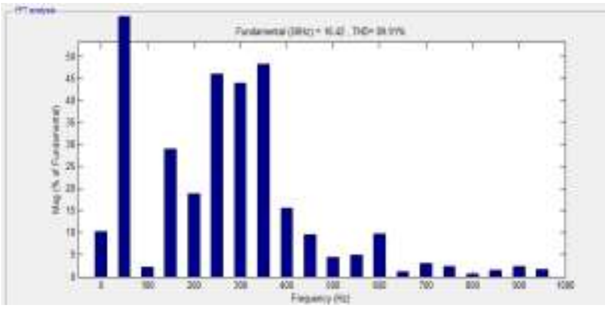

Fig 5 THD spectrum of source current for conventional VFD

The source current and dc link capacitor voltage of the conventional VFD fed from a single phase ac source is shown in figure 6.

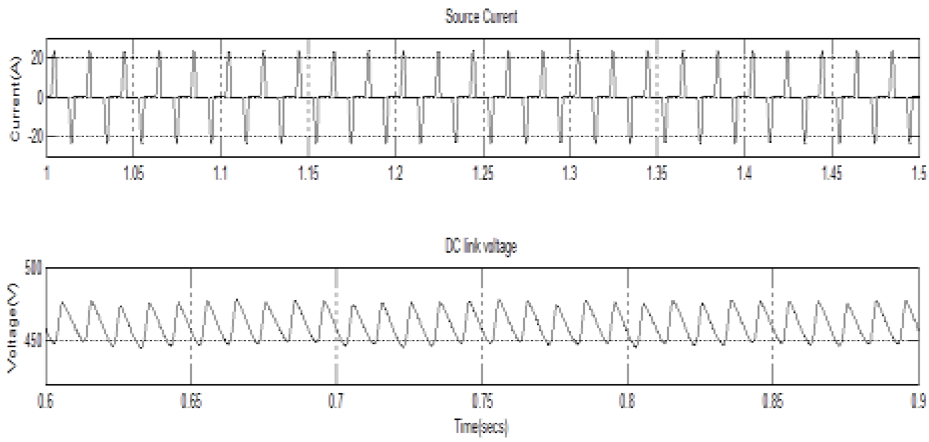

Fig 6 Source current and DC link voltage waveforms for conventional VFD fed from a single phase ac source

The THD value of the source current is about 87.11 %.The FFT analysis of source current is shown in figure 7.

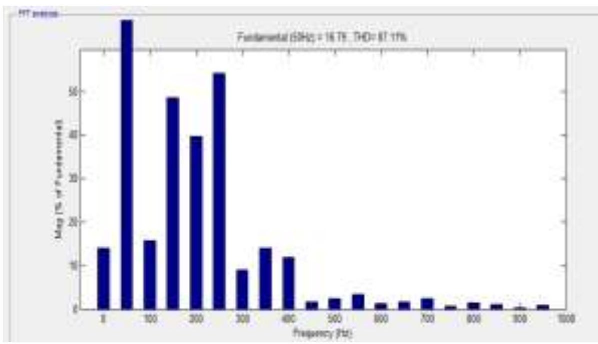

Fig 7 THD spectrum of source current for conventional VFD fed from a single phase ac source

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The above model was simulated in a MATLAB-Simulink environment. The output waveforms for torque, rotor speed and stator current were obtained as shown in figure 8.

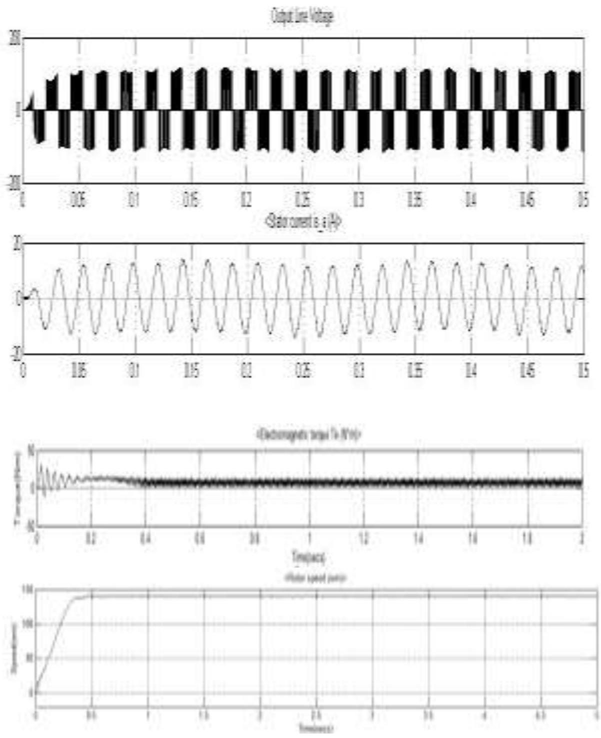

Fig 8 Stator current, Torque, rotor speed waveforms of the new converter

The waveforms for source current and dc link voltage are shown in figure 9.

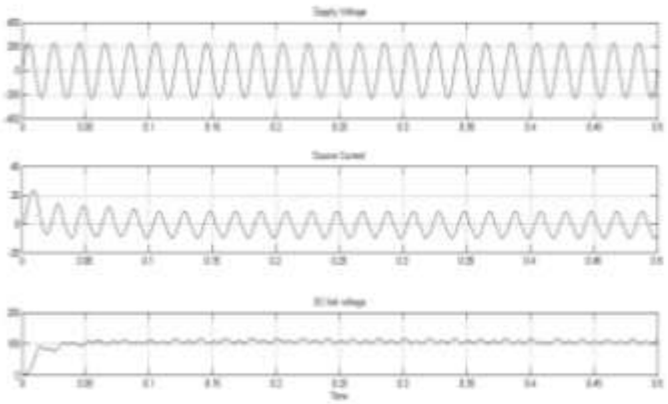

Fig. 9 Source current and dc link voltage waveform of the new converter

As can be seen, the induction motor exhibits very high transients during starting. At steady-state the torque first rises to maximum value called the breakdown torque after which it settles down. It is also observed that the rotor speed increases to its rated value and stays constant at that value. The stator currents exhibited high transients during the starting of the motor. They then settled down to low amplitude sinusoidal oscillations. The torque, speed and current settle to a steady value after some transient oscillations as shown in figure 8. By performing FFT analysis for the source current, THD is observed to be about 8.53%.

The simulated results of the converter is explained in this chapter. It is seen that THD is higher for the conventional converter.

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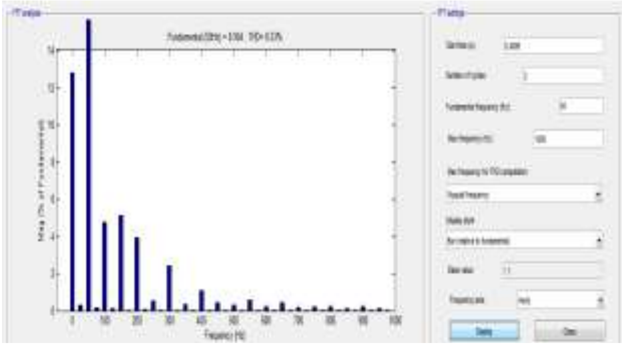

Fig10 THD spectrum of the source

On comparing the active front end topology with three phase VFD and from a single phase source the following results were obtained.

Table 2 Comparison performance of three phase VFD with active front end converter

SOURCE	INPUT RMS CURRENT	INPUT CURRENT THD
With three phase input	10.37 A	89.91%
With single phase input	6.35 A	87.71%
With new topology	4.96 A	8.53%

From the waveforms and the results shown in table 2, it is seen that the input peak current and input harmonics are better in case of the VFD powered from the single phase ac source with the non-regenerative active front end circuit are reduced significantly.
From these results, it can be concluded that the new topology is better than the existing conventional ones.

IV. CONCLUSION

The non-regenerative circuit aims at reducing the ripple across the dc bus capacitor and reducing the peak current flowing through the rectifier diodes. The main idea is based on storing energy in an external inductor and retrieving it at the appropriate time to transfer it to the load in an efficient and optimal manner. The external components used are not very large and can be accommodated within a VFD enclosure. The presence of three phase diode bridge rectifier helps to better distribute the higher input root-mean-square current so that the diodes need not carry current higher than their nominal rating. The THD of the supply current decreased from 87.11% to 8.53%. By separating the filter capacitor from the main dc bus capacitors, common dc bus application is easy to implement. The dc bus capacitor can be astandard electrolytic capacitor, while the higher ripple current is handled by the ac filter capacitors.

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REFERENCES

[1] E. C. dos Santos, C. B. Jacobina, E. R. C. da Silva, and N. Rocha, “Single phase to three-phase power converters:
[2] State of the art,” IEEE Transactions on Power Electronics., vol. 27, no. 5, pp. 2437–2452, May 2012.
[3] M. Lazic, M. Zivanov, and B. Sasic, “Designing of multiphase boost converter for hybrid fuel cell/battery power sources,” in Paths to Sustainable Energy, J. Nathwani and A. Ng, Eds. Rijeka, Croatia: InTech,Dec. 30, 2010, ch. 19.
[4] Y. Jang and M. M. Jovanic, “A bridgeless PFC boost rectifier with optimized magnetic utilization,” IEEE Transactions on Power Electronics., vol. 24, no. 1,pp. 85–93, Jan. 2009.

[5] P. N. Enjeti and A. Rahman, "A new single-phase to three-phase converter with active input current shaping for low cost AC motor drives," IEEE Transactions on Industrial Applications., vol. 29, no. 4, pp. 806–813, Jul./Aug. 1993.

[6] T. B. Bashaw and T. A. Lipo, "B4 topology options for operating three phase induction machines on single phase grids," in Proc. IEEE Applied Power Electronics Conerence. Expo., Mar. 2005, pp. 1894–1902.

[7] P. N. Enjeti, A. Rahman, and R. Jakkali, "Economic single-phase to three-phase converter topologies for fixed and variable frequency output," IEEE Transactions on Power Electronics., vol. 8, no. 3, pp. 329–335,Jul. 1993.

[8] D. M. Divan, "A new topology for single UPS systems," in Conf. Rec.IEEE IAS Annu. Meeting, 1989, pp. 931–936.

[9] M. Swamy, "An improved single-phase active front end rectifier system for use with three-phase VFDs," U.S. Patent Application, Jan. 2013.

[10] A. I. Maswood and F. Liu, "A novel unity power factor input stage for AC drive applications," IEEE Transactions on Power Electronics, vol. 20, no. 4, pp. 839–846, Jul. 2005.

[11] M. Swamy and S. Schifko, "An improved active front end non regenerative rectifier system employing a five-limb inductor," in Proceedings IEEE IEMDC, May 2013, pp. 1241–1248.

[12] S. M. Metev and V. P. Veiko, Laser Assisted Microtechnology, 2nd ed., R. M. Osgood, Jr., Ed. Berlin, Germany: Springer-Verlag, 1998.

[13] J. Breckling, Ed., The Analysis of Directional Time Series: Applications to Wind Speed and Direction, ser. Lecture Notes in Statistics. Berlin, Germany: Springer, 1989, vol. 61.

[14] S. Zhang, C. Zhu, J. K. O. Sin, and P. K. T. Mok, "A novel ultrathin elevated channel low-temperature poly-Si TFT," IEEE Electron Device Lett., vol. 20, pp. 569–571, Nov. 1999.

[15] M. Wegmuller, J. P. von der Weid, P. Oberson, and N. Gisin, "High resolution fiber distributed measurements with coherent OFDR," in Proc. ECOC'00, 2000, paper 11.3.4, p. 109.

[16] R. E. Sorace, V. S. Reinhardt, and S. A. Vaughn, "High-speed digital-to-RF converter," U.S. Patent 5 668 842, Sept. 16, 1997.

[17] (2002) The IEEE website. [Online]. Available: http://www.ieee.org/

[18] M. Shell. (2002) IEEEtran homepage on CTAN. [Online]. Available: http://www.ctan.org/tex-archive/macros/latex/contrib./supported/IEEEtran/

[19] FLEXChip Signal Processor (MC68175/D), Motorola, 1996.

[20] "PDCA12-70 data sheet," Opto Speed SA, Mezzovico, Switzerland.

[21] A. Karnik, "Performance of TCP congestion control with rate feedback: TCP/ABR and rate adaptive TCP/IP," M. Eng. thesis, Indian Institute of Science, Bangalore, India, Jan. 1999.

[22] J. Padhye, V. Firoiu, and D. Towsley, "A stochastic model of TCP Reno congestion avoidance and control," Univ. of Massachusetts, Amherst, MA, CMPSCI Tech. Rep. 99-02, 1999.

[23] Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specification, IEEE Std. 802.11, 1997.

BIOGRAPHY

Shruti K K received the B. Tech degree in Electrical & Electronics Engineering from Coimbatore Institute of Technology in 2013. She is currently M. Tech student at Govt. College of Engineering, Kannur.