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Single Phase Multilevel Inverter for Induction Motor Drives

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Abstract: Conventional inverters require numerous DC voltage sources, switches and increased converter cost for high voltage applications. In high power and high voltage applications, the two level inverters have some limitations mainly due to switching losses, dv/dt and di/dt stresses and constraint of the semiconductor power device ratings. To overcome these issues multilevel inverters can be employed. Multilevel approach gives reduced stress on semiconductor switches, lower Total Harmonic Distortion (THD) at output, low switching losses, high voltage capability, and ease of control. Hence multilevel inverters are gaining more importance and detailed research and studies are still going on in this area.
In this paper design and simulation results of single phase seven level, inverter fed induction motor drive is presented. The seven level output is obtained by an improved inverter topology with less number of circuit components and reduced output voltage THD. The multilevel inverter is controlled with phase disposition pulse width modulation. The simulation of single phase seven level inverter fed induction motor model is done by using MATLAB. The DC link capacitor voltage is balanced by using Resonant Switched Capacitor Converter (RSCC). From the simulation result it is observed that the output waveforms are better than that of a conventional inverter fed induction motor drive and output voltage THD is further reduced by employing RSCC circuit.

Keywords: Multilevel Inverters, Voltage Balancing Circuits, Resonant Switched Capacitor Converter (RSCC), Phase Disposition Pulse Width Modulation (PDPWM).

I. INTRODUCTION

Renewable energy based clean and non-pollutant power generation systems are gaining more importance and have rapidly developed in recent years. These alternative energy generation systems are powered by micro sources such as fuel cells, photovoltaic (PV) systems, and batteries [1]. Inverters for alternative energy generation are realized using a two-stage power processing scheme, comprised of a high step-up dc– dc front-end converter followed by a grid tied dc–ac inverter. The general concept involves utilizing a higher number of active semiconductor switches to perform the power conversion [2]. But high power and high voltage applications inverters have some limitations. In order to overcome these problems, multilevel inverters are used.
Multilevel inverters have been widely accepted for high power high voltage applications. Their performance is highly superior to that of conventional two level inverters due to reduced harmonic distortion, lower electromagnetic interference, and higher dc link voltages. However, it has some disadvantages such as increased number of components, complex pulse width modulation control method, and voltage balancing problem. An important feature of multilevel converters is that the semiconductors are wired in a series type connection, which allows operation at higher voltages. The series connection is typically made with clamping diodes, which eliminates overvoltage concerns. Since the switches are not truly series connected, their switching can be staggered, which reduces the switching frequency and thus the switching losses.
A number of inverter topologies have been introduced for various applications. These are with respect to the number of power stages, location of power-decoupling capacitors, use of transformers, and types of grid interface [3]–[4]. But they suffer from certain drawbacks like limited-lifetime of electrolytic capacitors for power decoupling [5], high ground leakage current when the unipolar PWM scheme is used in a transformer less PV system [6], low system efficiency if an additional high-frequency bidirectional converter is employed and increased cost. Three basic topologies are diode clamped multilevel inverters, flying capacitor multilevel inverters and cascaded multilevel inverters.
Diode clamped multilevel inverters are used in conventional high power ac motor drive applications like conveyors, pumps, fans, and mills [7]. But the number of clamping diodes will increase with the increase in the number of levels. Flying capacitor multilevel inverters been used in high bandwidth, high switching frequency applications such as medium voltage traction drives. But, voltage control is difficult for all the capacitors. Capacitors are expensive than diodes. Cascaded multilevel inverters can be used where high power quality is essential such as static synchronous compensators, active filters and reactive power compensation applications. Also, there are various emerging multilevel

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inverter topologies like mixed level hybrid multilevel cells, asymmetric hybrid multilevel cells, soft switched multilevel inverters, etc. For increasing voltage levels the number of switches required will increase. Hence the switching losses will increase and the circuit becomes complex [8]-[10]. With reduced number of power components a seven level inverter is studied. Phase Disposition Pulse Width Modulation (PDPWM) is used to control the circuit.

II. SEVEN LEVEL INVERTER

Fig.1 shows the seven level inverter. An input voltage divider is composed of three series capacitors C_1, C_2, and C_3. The divided voltage is transmitted to H-bridge by four MOSFETs, and four diodes. The voltage is send to output terminal by H-bridge which is formed by four MOSFETs. The new multilevel inverter generates seven level ac output voltages with the appropriate gate signals design.

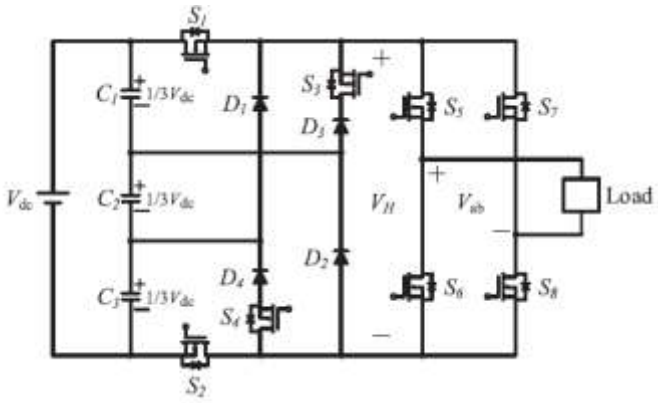

Fig.1.: Seven level inverter topology

A. Operating Principles

The required seven voltage output levels ($\pm1/3V_{dc}$, $\pm2/3V_{dc}$, $\pm V_{dc}$, 0) are generated as follows.

1) To generate a voltage level $V_o = 1/3V_{dc}$, S_1 is turned on during the positive half cycle. Energy is provided by the capacitor C_1 and the voltage across H-bridge is $1/3V_{dc}$. S_5 and S_8 are turned on, and the voltage applied to the load terminals is $1/3V_{dc}$. Fig.2 shows the current path in this mode.

2) To generate a voltage level $V_o = 2/3V_{dc}$, S_1 and S_4 are turned on. Energy is provided by the capacitors C_1 and C_2. The voltage across H-bridge is $2/3V_{dc}$. S_5 and S_8 are turned on, and the voltage applied to the load terminals is $2/3V_{dc}$. Fig.3 shows the current path in this mode.

3) To generate a voltage level $V_o = V_{dc}$, S_1 and S_2 are turned on. Energy is provided by the capacitors C_1, C_2, and C_3. The voltage across H-bridge is V_{dc}. S_5 and S_8 are turned on, and the voltage applied to the load terminals is V_{dc}. Fig.4 shows the current path in this mode.

4) To generate a voltage level $V_o = -1/3V_{dc}$, S_2 is turned on at the negative half cycle. Energy is provided by the capacitor C_3, and the voltage across H-bridge is $1/3V_{dc}$. S_6 and S_7 are turned on, and the voltage applied to the load terminals is $-1/3V_{dc}$. Fig.5 shows the current path in this mode.

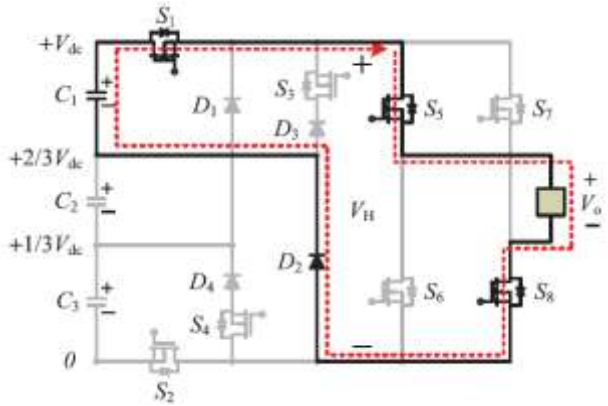

Fig.2: Switching combination of output voltage level $1/3V_{dc}$.

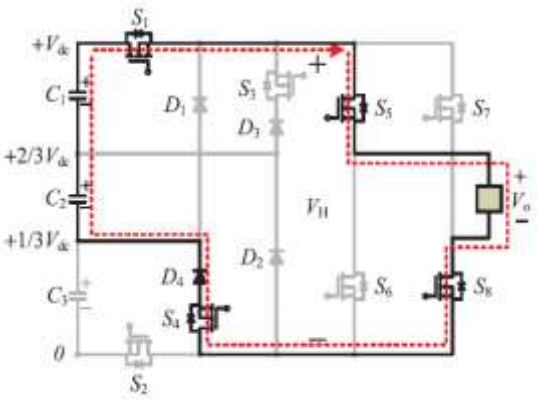

Fig.3: Switching combination of output voltage level $2/3V_{dc}$.

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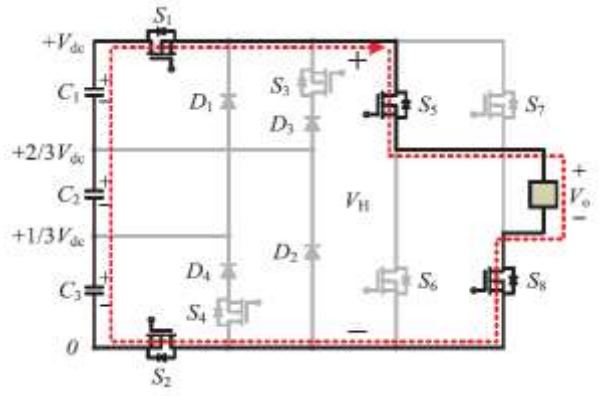


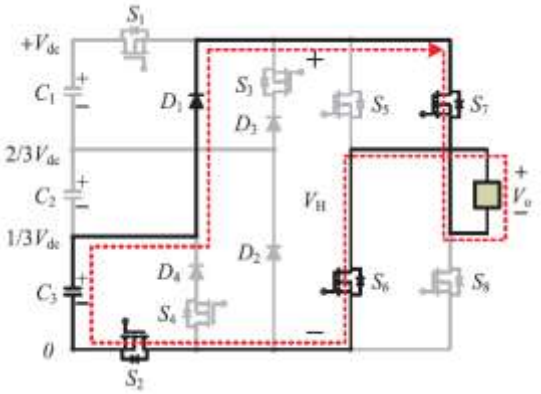
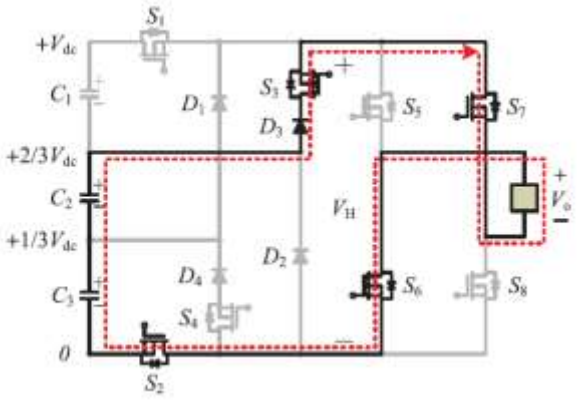


Fig.4: Switching combination of output voltage level V_{dc}. Fig.5: Switching combination of output voltage level $-1/3V_{dc}$.

5) To generate a voltage level $V_o = -2/3V_{dc}$, S_2 and S_3 are turned on. Energy is provided by the capacitors C_2 and C_3. The voltage across H-bridge is $2/3V_{dc}$. S_6 and S_7 are turned on, and the voltage applied to the load terminals is $-2/3V_{dc}$. Fig.6 shows the current path in this mode.
6) To generate a voltage level $V_o = -V_{dc}$, S_1 and S_2 are turned on. Energy is provided by the capacitor C_1, C_2, and C_3, the voltage across H-bridge is V_{dc}. S_6 and S_7 is turned on, the voltage applied to the load terminals is $-V_{dc}$. Fig.7 shows the current path in this mode.
7) To generate a voltage level $V_o = 0$, S_5 and S_7 are turned on. The voltage applied to the load terminals is zero. Fig.8 shows the current path in this mode.



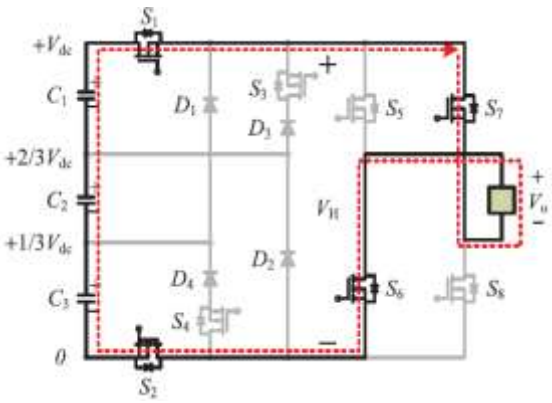


Fig.6: Switching combination of output voltage level $-2/3V_{dc}$. Fig.7: Switching combination of output voltage level $-V_{dc}$.

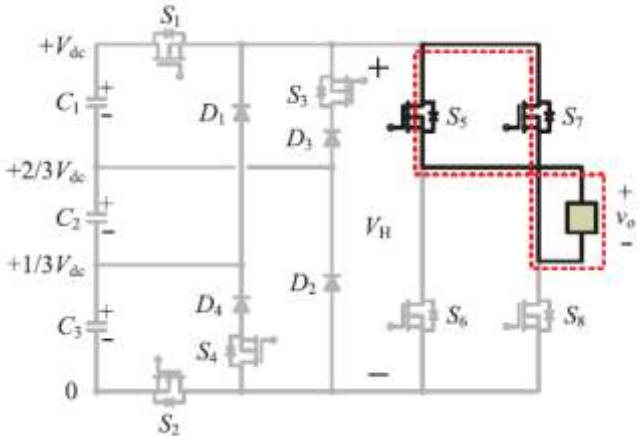


Fig.8: Switching combination of output voltage level 0.

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B. Topology Comparison

Table I presents the number of components required to implement a seven level inverter using the introduced topology and three other topologies that can be considered as the standard multilevel configurations, the diode clamped inverter, the capacitor clamped inverter, and the cascaded multilevel inverter. Table I shows that new topology achieves the reduction in the number of power devices. Table II shows the voltage stress comparison between different types of inverters.

TABLE I Components Comparison between Four different configurations of Seven-level Inverters

	Introduced	Diode- Clamped	Capacitor- Clamped	Cascaded
Input Sources	1	1	1	3
Input Capacitors	3	6	2	3
Clamped Capacitors	0	0	5	0
Power Switches	8	12	12	12
Diodes	4	10	0	0

TABLE II Voltage stress Comparison between Four different configurations of Seven-level Inverters

	Introduced	Diode Clamped	Capacitor Clamped	Cascaded
Input Sources	V_0	$2V_0$	$2V_0$	$V_0/3$
Input Capacitors	$V_0/3$	$V_0/3$	$V_0/2$	$V_0/3$
Power Switches	V_0	$V_0/3$	$V_0/3$	$V_0/3$
Diodes	$2V_0/3$	$3V_0/2$	-	-

C. Voltage Balancing Circuit based on RSCC

Multilevel inverter topology helps to reduce the number of switching devices and to reduce the switching losses and THD. Since the voltage deviation causes larger harmonics distortion in the output voltage, voltage balancing circuits are necessary for the capacitors in the multilevel inverters. Two possible solutions for the voltage imbalance problem are installing of voltage balancing circuits on the dc side of the inverter or modifying the converter switching pattern according to a control strategy [11]–[13].

However, these methods work only in a low range of the output voltage and result in increased harmonic distortion and/or switching frequency [14]–[15]. For balancing the input capacitor voltage, Resonant Switching Capacitor Converter (RSCC) is found to be a better option [16]-[18]. Fig.9 shows the circuit configuration of a unit of RSCC. These methods select an appropriate switching state from redundant switching states or adjust the hysteresis bandwidth in the current controller. Switching sequence of control for RSCC circuit is shown in Fig.10.

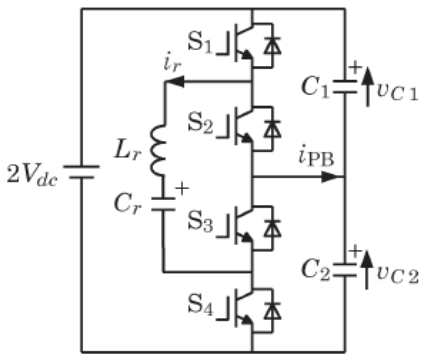

Fig.9: RSCC Voltage Balancing Circuit

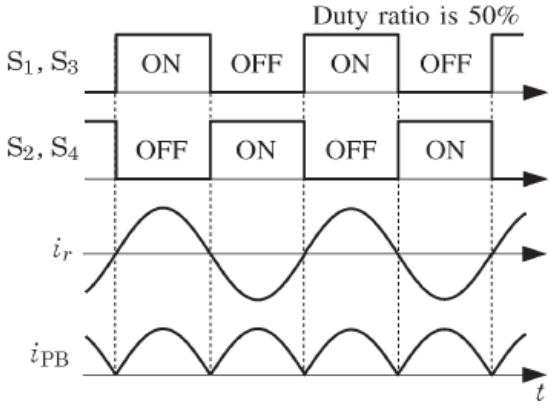

Fig.10: Switching Sequence of control for RSCC circuit

Fig.11 shows the configuration of seven level inverter with RSCC. To apply RSCC at seven level configuration, two switches S_{b5} and S_{b6}, resonant inductor L_r, and resonant capacitor C_r are added. In this application, switches S_{b1}, S_{b3}, and S_{b5} are turned on at the same time. S_{b2}, S_{b4}, and S_{b6} are turned on simultaneously. The duty cycle of each switch is equal to 50%.

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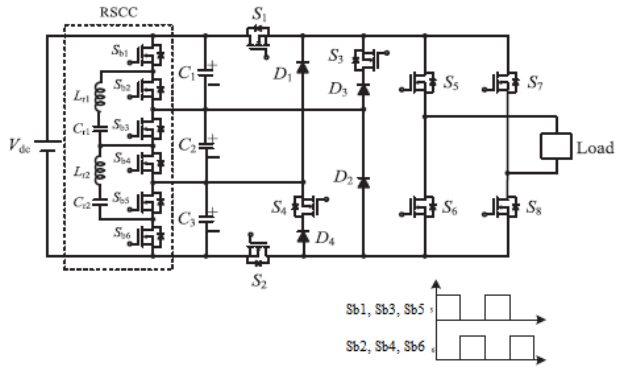

Fig.11: Configuration of Seven Level Inverter with RSCC

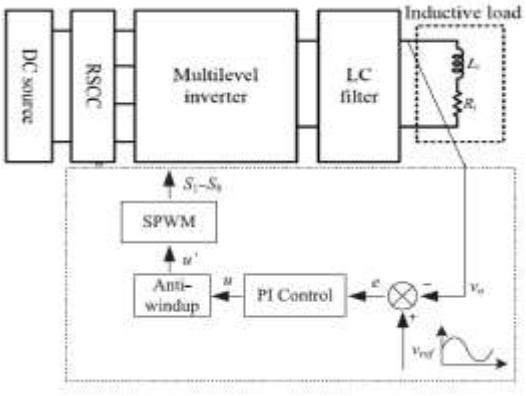

Fig.12: Seven level inverter with Control Algorithm

Fig.12 shows seven level inverter and control block. It detects the output voltage and compares it with a built-in reference signal. The error signal is fed back to the PI controller and the control signal is generated. A low pass filter is necessary to reduce the THD of the sinusoidal output voltage.

III.CONTROL STRATEGY

Several modulation techniques and control strategies have been developed for multilevel inverters including the following: multilevel Sinusoidal Pulse Width Modulation (SPWM), Multi level Selective Harmonic Elimination and Space Vector Modulation (SVM), etc [19], [20]. A very popular method in industrial applications is the classic carrier based sinusoidal PWM (SPWM) that uses the phase-shifting technique to reduce the harmonics in the load voltage. Several multicarrier techniques are developed to reduce the distortion, based on the classical SPWM with triangular carriers. Some methods use carrier disposition and others use phase shifting of multiple carrier signals. They are phase shifted (PS), phase disposition (PD), Phase opposition Disposition (POD) and Alternative Phase Opposite Disposition (APOD) [21].

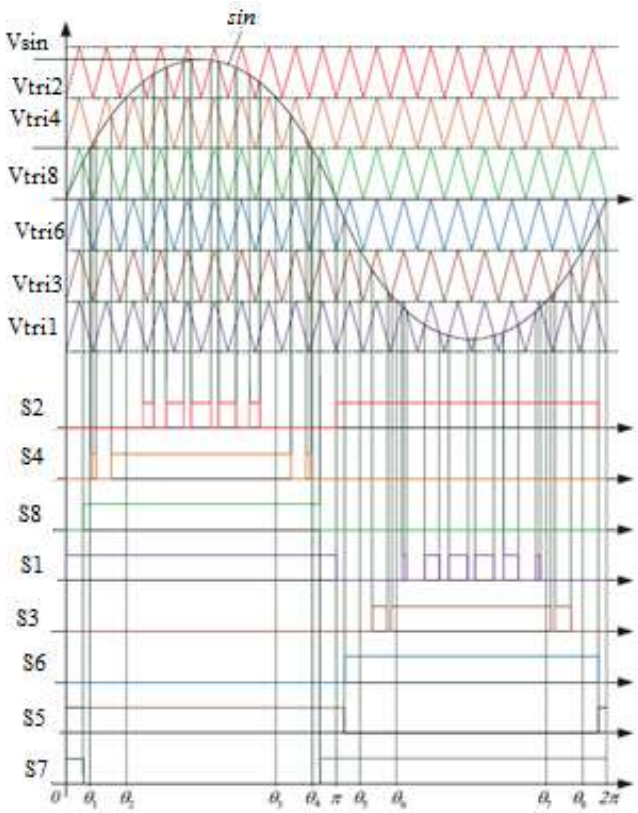

Fig.13. Control signals of switches.

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In this paper PDPWM is used to generate the control signals. In PD PWM all the carrier signals are in phase. The carrier signals are disposed in different bands. These carrier signals are compared with a reference sine waveform v_{sin} to get switching signals. For seven level inverter six carrier signals are required. Fig.13 shows the reference sine wave, carriers and control signals of switches.

IV. SIMULATION STUDY

To analyze the performance of the single phase seven level inverter fed induction motor. Initially the single phase seven level inverter is simulated. The pulse is generated by phase disposition technique. Fig. 14 shows the simulink model of seven level inverter. 400 V DC supply is used. DC link capacitors C_1, C_2, C_3 are selected as 250µF. a resistive load of 100 Ω is used. In the Fig.14, the simulink model shows that the divided voltage is given to the H –bridge through four MOSFETs and four diodes.

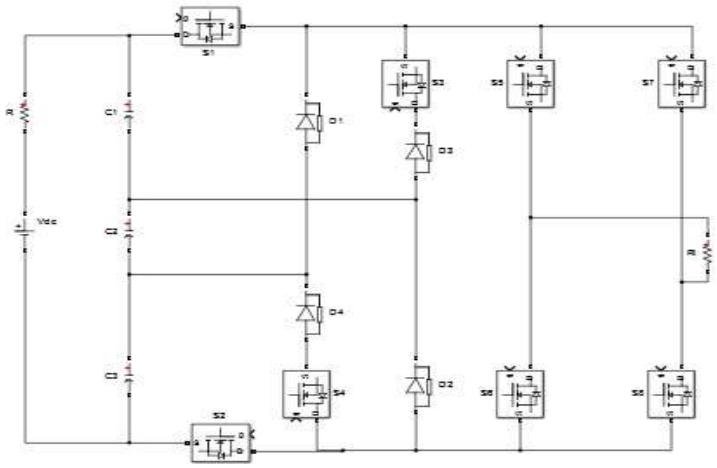

Fig.14: Simulink model of circuit configuration of Seven Level Inverter

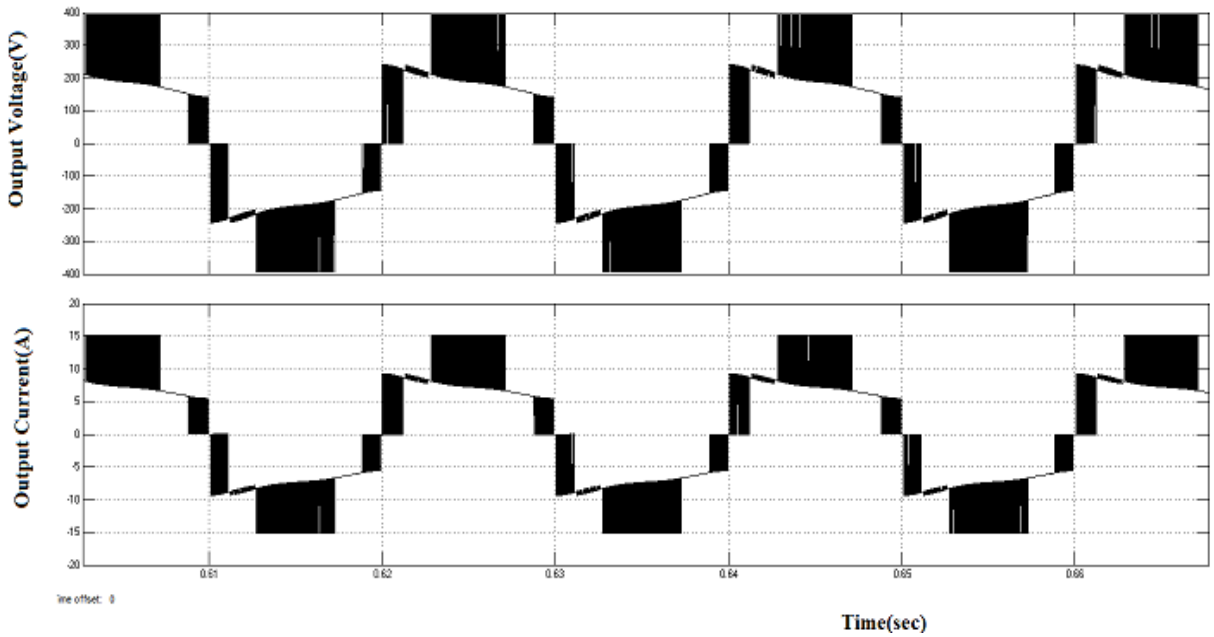

Fig.15: Output Voltage and Current waveforms

The output voltage and output current wave forms are shown in Fig.15. Some voltage levels are not obtained in the output, due to the voltage imbalance of dc capacitors. Hence voltage balancing circuits are necessary. From Fig.15 it can be seen that some voltage levels are not present in the output. The THD of output voltage is found to be 13.98%. Since the voltage deviation causes larger harmonic distortion in the output voltage, the dc link capacitor voltage is balanced [18]–[20].

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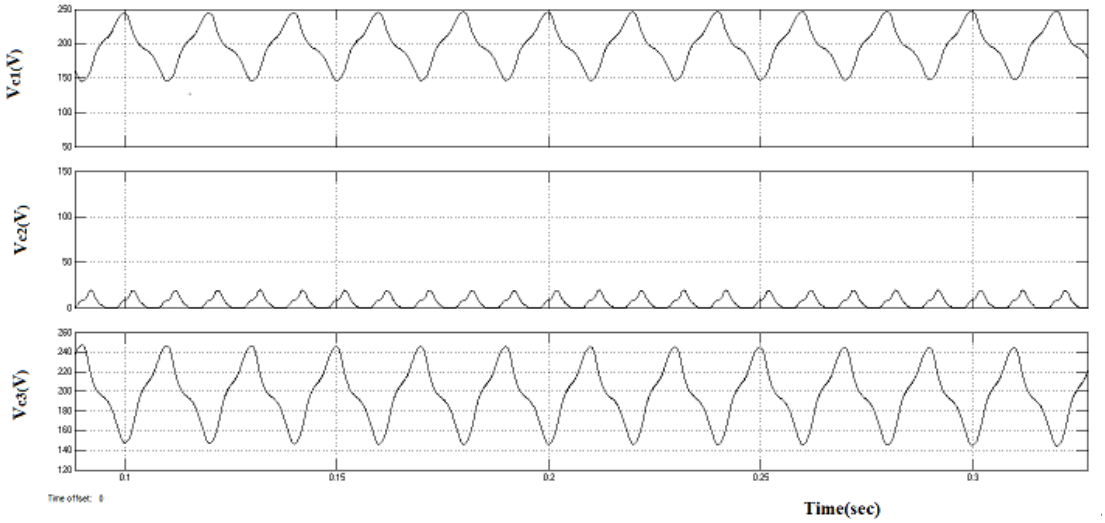

Fig.16: Voltage across the DC link Capacitors

The voltage across the dc link capacitors are shown in Fig.16. Fig. 16 shows that the voltage across the DC link capacitors is unbalanced. This causes distortion in the output waveforms. By using RSCC, the voltage balance of input capacitors is achieved. Balanced voltage across the DC link Capacitors are shown in Fig.17.The duty cycle of switches in RSCC circuit is equal to 50%.

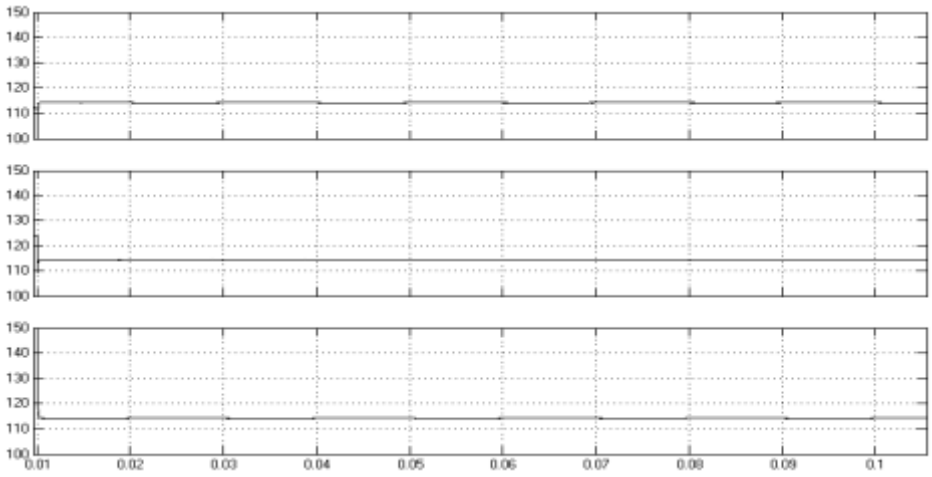

Fig.17: Balanced voltage across the DC link Capacitors

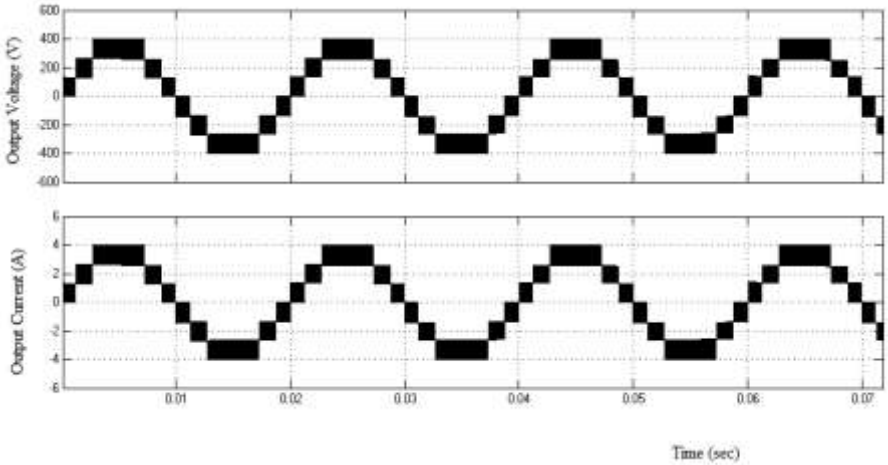

Fig.18: Output voltage and current waveforms of seven level inverter with RSCC

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If voltage across the capacitor C_1 is greater than that of the capacitor C_2, then the RSCC circuit charges the resonant capacitor C_r. Then the capacitor C_2 is charged by using C_r. The multilevel output voltage and current waveforms of seven level inverter with RSCC circuit is shown in Fig.18. The seven levels (±400, ±267, ±133, and 0 V) are obtained in the output.

By using RSCC voltage balancing circuit THD of output voltage is obtained as 9.83%. The fundamental value is obtained as 329.6 V. As the order of harmonics increases the magnitude of harmonic component is decreased. By using an LC filter (L= 10mH and C= 1µH) sinusoidal output can be obtained. The output voltage and current waveforms are shown in Fig.19. The obtained output waveform has a peak value of 320 V. The RMS value of output voltage is obtained as 225 V.

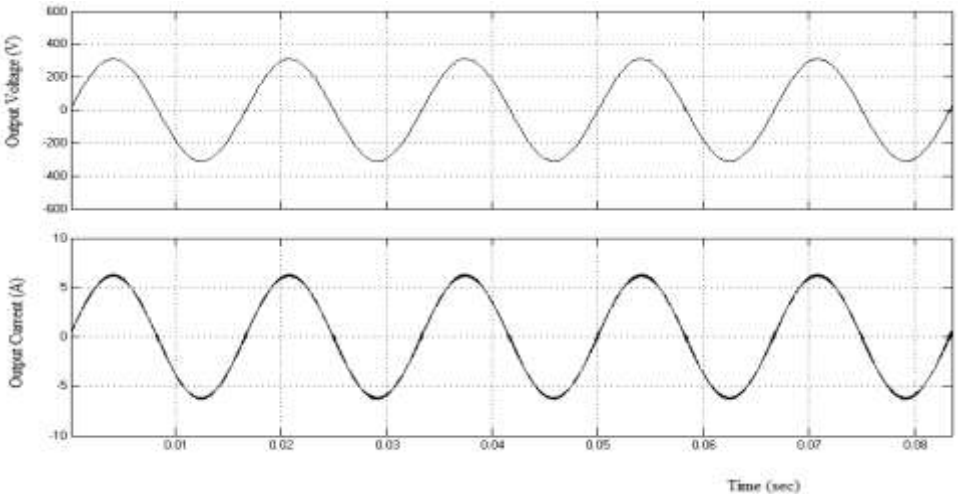

Fig.19: Filtered output voltage and current waveforms

The multilevel output voltage harmonic spectrum is shown in Fig.20. The THD of filtered output voltage waveform is obtained as 0.68%. It is shown in Fig.21. Fig. 22 shows the simulink model of seven level inverter fed induction motor. The filtered output of seven level inverter is fed to the induction motor (0.25HP, 220V, 50 Hz, 4 Pole, disconnection speed is taken as 75% of synchronous speed).Fig.23 shows the current, speed and electromagnetic torque of single phase Induction motor.

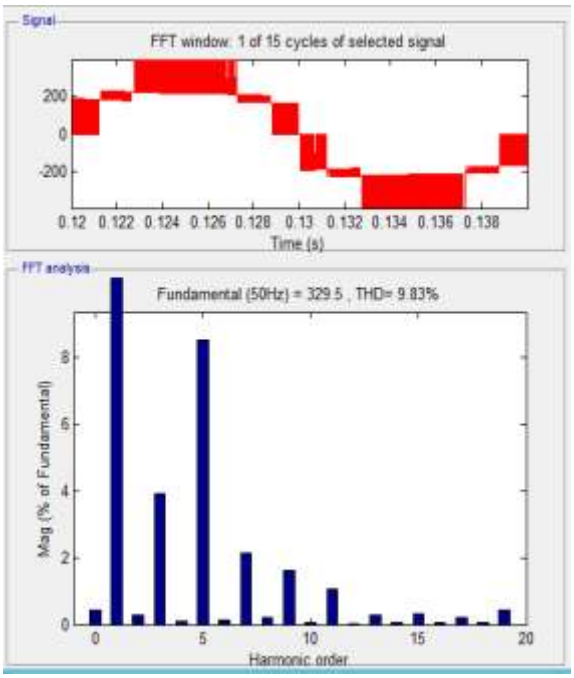

Fig.20: Multilevel Output voltage harmonic spectrum

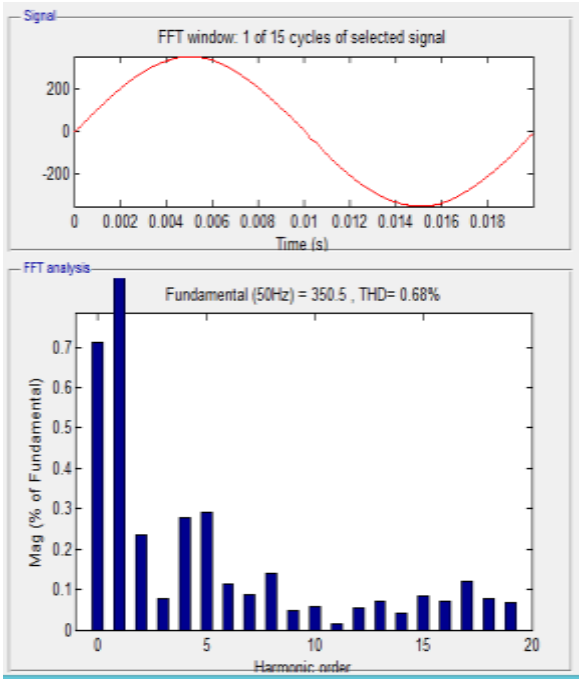

Fig.21: Output voltage harmonic spectrum

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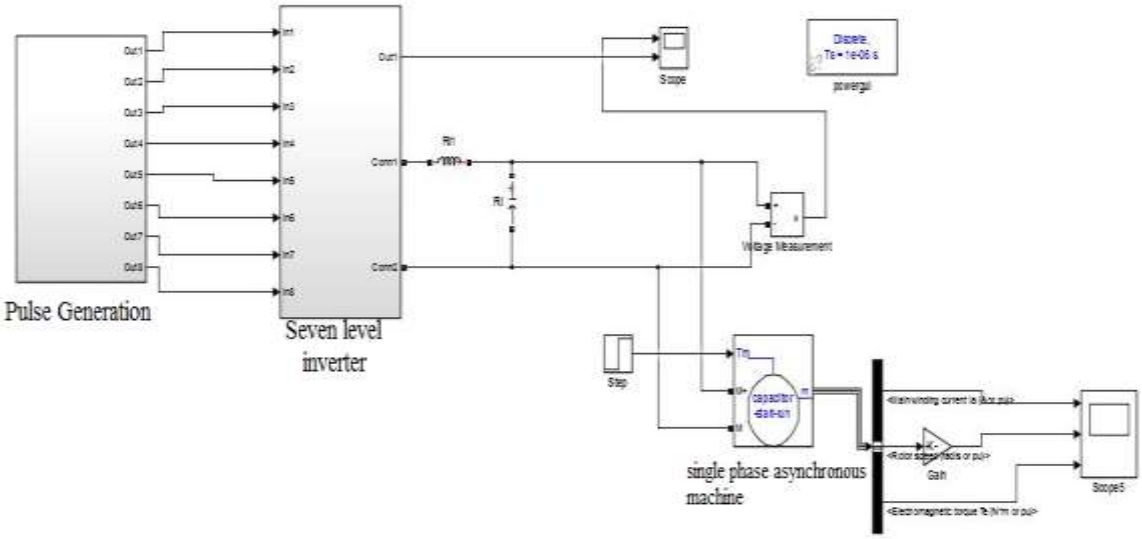

Fig.22: Simulink model of seven level inverter fed induction motor

Fig.22 shows the seven level inverter fed induction motor drive. The obtained torque and speed of the induction motor is also shown. It is verified that the studied seven level inverter is suitable for induction motor drive.

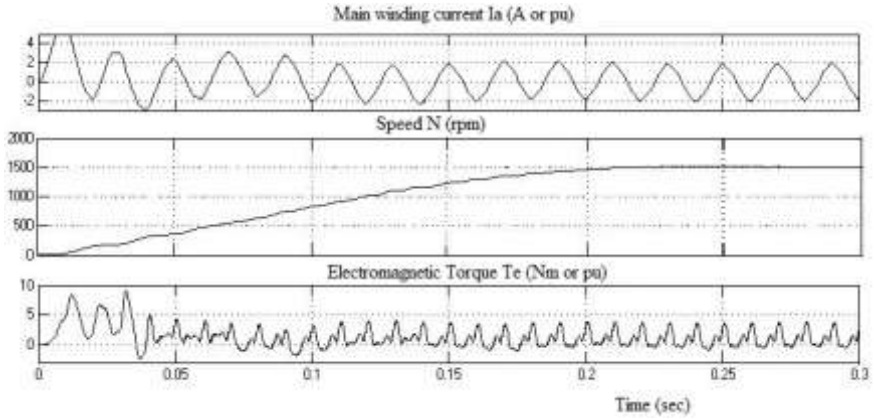

Fig.23: Current, Speed and Electromagnetic torque of Induction motor

V. CONCLUSION

Multilevel inverters are essential in high power and high voltage applications. Various multilevel inverters and control techniques are available. However the number of switching devices and complexity of control increases as the number of level increases. And, balancing of capacitor voltage is a problem to be solved since it causes harmonics and increased switching losses. With reduced number of power devices a seven level inverter is studied . Seven level inverter with RSCC voltage balancing circuit is simulated. The phase disposition technique is used to generate control signals. By using RSCC and an LC filter the THD is reduced. The seven level inverter fed induction motor is also simulated.

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