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Single-Inductor Series-Switch Five-Level Dual Buck Full Bridge Inverter

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Abstract: The conventional inverters are used to convert the DC from non-renewable sources to AC required for grid. The problems faced by these inverters are unexpected occurrence of shoot-through within the bridge arms and failure of reverse recovery during freewheeling mode. The dual buck inverters (DBI) will not suffer the problems due to shoot through and reverse recovery. In order to improve the efficiency and quality of output, dual buck multilevel inverters are used. They can provide better AC output with lower number of components than conventional multilevel inverters. In this paper a comparison of three level dual buck inverter and series-switch five level dual buck full bridge inverter is discussed. A novel topology of series-switch five-level dual buck full bridge with single inductor is proposed. The proposed topology requires single inductor and hence the size is reduced. Simulation is carried out using MATLAB/SIMULINK. The results obtained validate the performance of the proposed topology.

Keywords: Dual Buck Inverter, Multilevel Inverter, Three-Level Dual Buck Inverter, Series-Switch Five-Level Dual Buck Inverter, Single-Inductor.

I. INTRODUCTION

The global demand of electrical energy is constantly growing along with the declining production of fossil fuels, due to the environmental problems created by them. Thus the attention has changed to the clean and renewable energy resources such as solar arrays and wind generators. In recent years, due to the developments in power electronics, the energy extraction became easier and widespread. Among a variety of the renewable energy sources, photovoltaic (PV) sources have no supply limitations and reliability. It offers an option for clean, pollution free energy source, with almost no running and maintenance cost. The output of the PV system is a DC quantity. To utilize this energy in our daily life an inverter is required for DC to AC conversion of energy.The conventional inverters are used to invert the DC from these nonrenewable sources to AC required for grid. The defects of this topology are: 1) the shoot-through possibility of the bridge arms degrades reliability of the inverter; 2) the weight and volume of the inverter are hard to be reduced because the switching frequency is limited to the body diode of the power switch; 3) complicated control strategies should be employed to solve the unbalanced load problem. Shoot through problem of the power devices is a major threat to the reliability. As is known, a traditional method to solve the shoot through issue is by setting dead time. However, the dead time will cause a distortion of the output current. Also, during the dead time, the current may flow through the body diode of the switch which can cause the failure of the reverse recovery. Inverters developed on the dual buck concept can overcome these disadvantages. Fig 1 shows the basic structure of a dual buck inverter. Various dual buck inverters with different control strategies are developed so far [1]-[7].

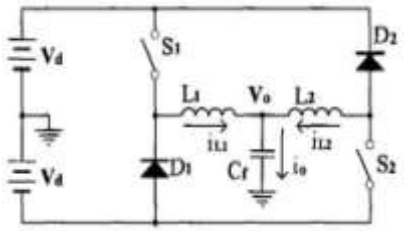

Fig. 1 Dual Buck Half Bridge Inverter

The multilevel technique is an effective way to achieve high power density. Many power generating systems are now utilizing different multilevel techniques. The conventional multilevel inverters [8] like the neutral point clamped or diode clamped multilevel inverter, the flying capacitor multilevel inverter, and the cascaded H-bridge multilevel inverter can provide better AC waveforms. But it involves more number of switching devices and complex control circuits.

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Multilevel inverters can be developed using dual buck inverter concept. Fig 2 and 3 shows three level [9] and five-level dual buck multilevel inverters [10], [11].

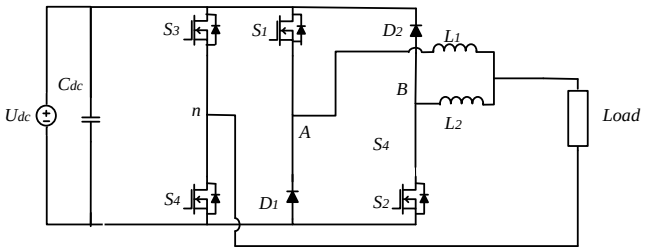

Fig. 2 Three-Level Dual Buck Full Bridge Inverter

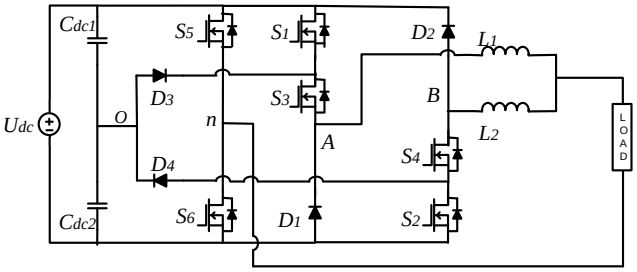

Fig. 3 Series-Switch Five-Level Dual Buck Full Bridge Inverter

II. COMPARISON OF THREE-LEVEL AND FIVE-LEVEL DUAL BUCK INVERTERS

Three-level full bridge dual buck inverter is a combination of half bridge inverter and dual buck half bridge inverter[11]. Combining three-level full bridge inverter with a capacitor voltage divider circuit consisting of two clamping branches forms a series switch five-level dual buck full bridge inverter [11]. It consists of two filter inductors which makes the inverter bulky. Both three-level and five-level mentioned here is having a branch consisting of two switches in series. This could be avoided by replacing a half bridge inverter arm with a dual buck half bridge inverter.

III.PROPOSED TOPOLOGY

The proposed topology of five-level DBFBI is shown in Fig. 4. It is derived from the three-level DBFBI combining with a two split dc bus capacitors (Cdc_1, Cdc_2) and neutral point clamped branch. Compared to Fig. 3, this topology has a single inductor [12] in the output side, which will reduce the size and cost. Two diodes are connected in series [13] to the nodes A and B and an inductor L is connected in between the diodes as shown in Fig.4 instead of two inductors. Thus a total of six switches and six diodes with 2 capacitors and one inductor is required for the basic circuitry model. Since the inductor number is reduced and thereby size, the proposed model can be utilized in the practical circuits.

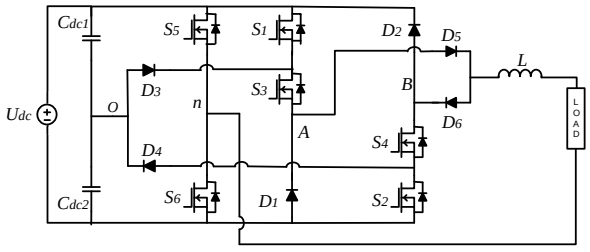

Fig. 4 Single-Inductor Series-Switch Five-Level Dual Buck Full Bridge Inverter

The key waveforms of the series switch five-level DBFBI are shown in Fig. 5. Two reference signals u_{r1} and u_{r2} are compared with a carrier signal u_{st} to produce pulse width modulation signals for the switches. u_{gS1} –u_{gS6} represent the gate drive signals of power switches S_1 to S_6. In order to avoid the shoot-through problem, the dead time has been set within the drive signals of the switches S_5 and S_6 .u_{An} represents the voltage difference between the node A and node n, and u_{Bn} is the voltage difference between the node B and node n. The output voltage before filter is$u_{AB\text{-}n}$ andis represented as

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$$u_{AB-n} = \frac{u_{An} + u_{Bn}}{2} \quad (1)$$

A. Modes of Operations

Single-Inductor series-switch five-level dual buck inverter has basically six modes of operation as shown in Fig. 6

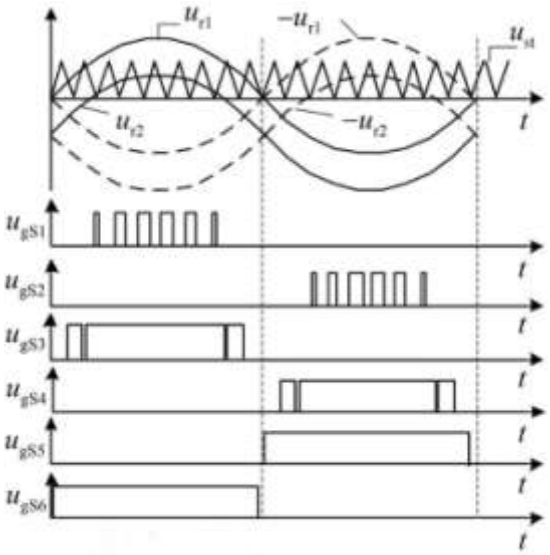

Fig. 5 Key Waveforms for switching pulses.

Mode 1 [Refer to Fig. 6(a)]: Maximum positive output, u_{An} = U_{dc} . There is no current flowing through the diode D_6; thus, the voltage across the diode D_6 is equal to zero, and u_{Bn}= u_{An}+u_{D5}. As a result, $u_{AB\text{-}n}$ = U_{dc}.S_1 , S_3, and S_6 are turned ON, and the other switches are turned OFF. The active current path at this state is shown in Fig. 6(a). The reverse blocking voltage on D_3 is equal to $0.5U_{dc}$, and the reverse blocking voltage on D_1 is equal to U_{dc}. The drain– source voltage on S_5 is equal to U_{dc} . During this state, the inductor current i_L increases linearly.

$$L\frac{di_L}{dt} = U_{dc} - u_o \quad (2)$$

Mode 2 [Refer to Fig. 6(b)]: Half-level positive output, u_{An} = $0.5U_{dc}$. There is no current flowing through the diode D_6; thus, the voltage across the diode D_6 is equal to zero, and u_{Bn}= u_{An}+u_{D5}. As a result, $u_{AB\text{-}n}$ = $0.5U_{dc}$. S_3 and S_6 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig. 6(b). The drain–source voltage on S_1 is equal to $0.5U_{dc}$, and the reverse blocking voltage on D_1 is equal to $0.5U_{dc}$. During this state, the inductor current i_L decreases linearly when the output voltage is higher than $0.5U_{dc}$.

$$-L\frac{di_L}{dt} = \frac{U_{dc}}{2} - u_o \quad (3)$$

The inductor current i_L increases linearly when the output voltage of the utility grid is lower than $0.5U_{dc}$

$$L\frac{di_L}{dt} = \frac{U_{dc}}{2} - u_o \quad (4)$$

Mode 3 [Refer to Fig. 6(c)]: Zero output at the positive half period of the utility grid, u_{An} = 0. There is no current flowing through the diode D_6; thus, the voltage across the diode D_6 is equal to zero, and u_{Bn} = u_{An}+u_{D5}. As a result, $u_{AB\text{-}n}$ = 0. S_6 is turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig. 6(c). Both the drain– source voltages on S_1 and S_3 are equal to $0.5U_{dc}$. During this state, the inductor current i_L decreases linearly

$$L\frac{di_L}{dt} = -u_o \quad (5)$$

Mode 4 [Refer to Fig. 6(d)]: Zero output at the negative half period of the utility grid, u_{Bn} = 0. There is no current flowing through the diode D_5; thus, the voltage across the diode D_5 is equal to zero, and u_{An} = u_{Bn}+u_{D6}. As a result, $u_{AB\text{-}n}$ = 0. S_5 is turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig. 6(d). Both the drain–source voltages on S_2 and S_4 are equal to $0.5U_{dc}$. During this state, the inductor current i_L increases linearly

$$L\frac{di_L}{dt} = -u_o \quad (6)$$

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Mode 5 [Refer to Fig. 6(e)]: Half-level negative output, $u_{Bn} = -0.5U_{dc}$. There is no current flowing through the diode D_5; thus, the voltage across the diode D_5 is equal to zero, and$u_{An} = u_{Bn}+u_{D6}$. As a result, $u_{AB\text{-}n} = -0.5U_{dc}$. S_4 and S_5 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig. 6(e). The drain–source voltage on S_2 is equal to $0.5U_{dc}$, and the reverse blocking voltage on D_2 is equal to $0.5U_{dc}$. During this state, the inductor current i_L decreases linearly when the output voltage is lower than $0.5U_{dc}$.

$$-L\frac{di_L}{dt} = -\frac{U_{dc}}{2} - u_o \quad (7)$$

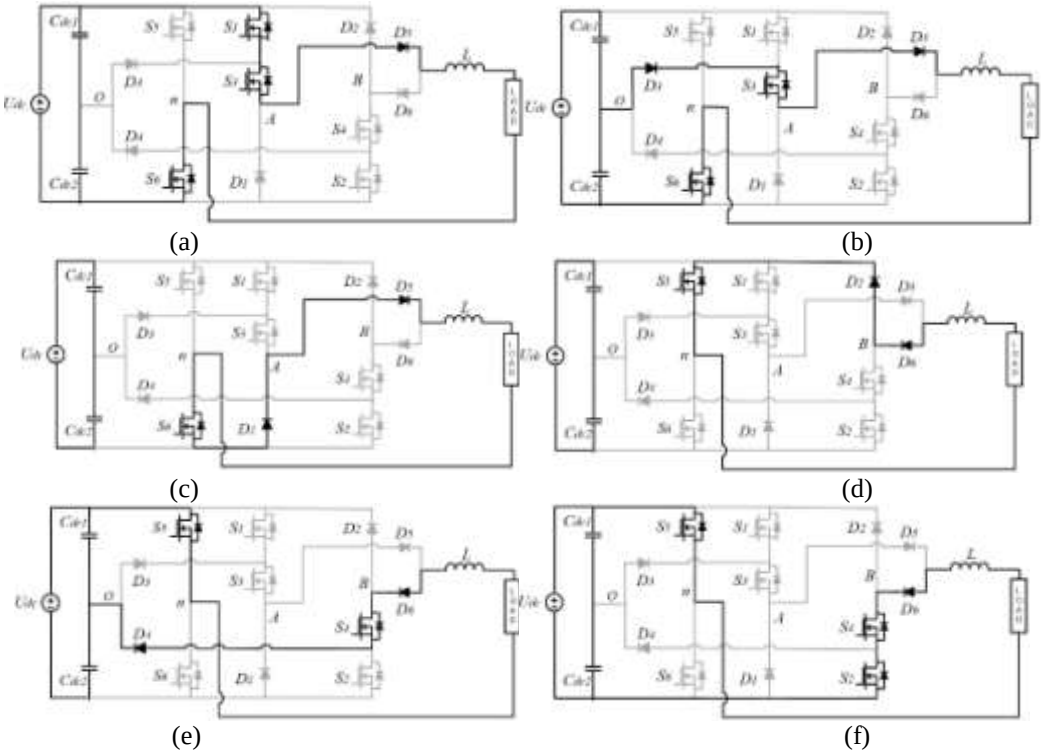

Fig. 5 Equivalent circuits of switching state. (a) Mode 1 (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

The inductor current i_L increases linearly when the output voltage is higher than $0.5U_{dc}$.

$$L\frac{di_L}{dt} = -\frac{U_{dc}}{2} - u_o \text{ b} \quad (8)$$

Mode 6 [Refer to Fig. 6(f)]: Maximum negative output,$u_{Bn} = -U_{dc}$. There is no current flowing through the diode D_5; thus, the voltage across the diode D_5 is equal to zero, and $u_{An} = u_{Bn}+u_{D6}$. As a result,$u_{AB\text{-}n} = -U_{dc}$. S_2, S_4, and S_5 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig. 6(f). The reverse blocking voltage on D_4 is equal to $0.5U_{dc}$, and the reverse blocking voltage on D_2 is equal to U_{dc}. During this state, the drain–source voltage on S_6 is equal to U_{dc}. In this mode, the inductor current i_{L2} decreases linearly

$$-L\frac{di_L}{dt} = -U_{dc} - u_o \quad (9)$$

Based on (2.2)–(2.9), it can be seen that the voltage jump of filter inductors is $0.5U_{dc.}$

B. Voltage Stress Analysis

The maximum drain–source voltages on the switches S_5 and S_6 are equal to U_{dc}. The maximum reverse blocking voltages on the diodes D_1 and D_2 are equal to U_{dc} as well. The maximum drain–source voltage across the switches S_1 and S_3 is U_{dc}. Since the switch S_1 is series connected with the switch S_3, the maximum drain–source voltage across each switch will be $0.5U_{dc}$.

Similarly, maximum drain–source voltage across the switches S_2 and S_4 is U_{dc}. Since the switch S_2 is series connected with the switch S_4 the voltage is divided among the two switches. Therefore, the maximum drain–source voltages on the switches, S_1, S_2, S_3, and S_4, are equal to $0.5U_{dc}$. The maximum reverse blocking voltages on the diodes, D_3 and D_4, are equal to $0.5U_{dc}$.

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IV. SIMULATION RESULTS

Three-level and five-level shown in Fig. 2 & 3 are simulated in MATLAB with a switching frequency of 40 kHz. A load resistance of 50 Ω with filter inductor 2 mH is used. The results obtained are as shown below.

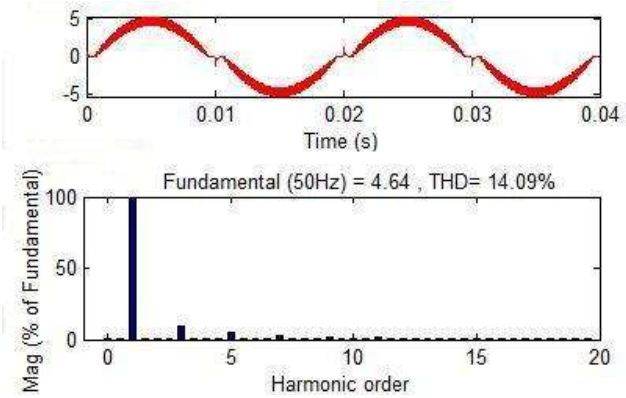

Fig. 7 Harmonic spectrum of three-level dual buck full bridge inverter

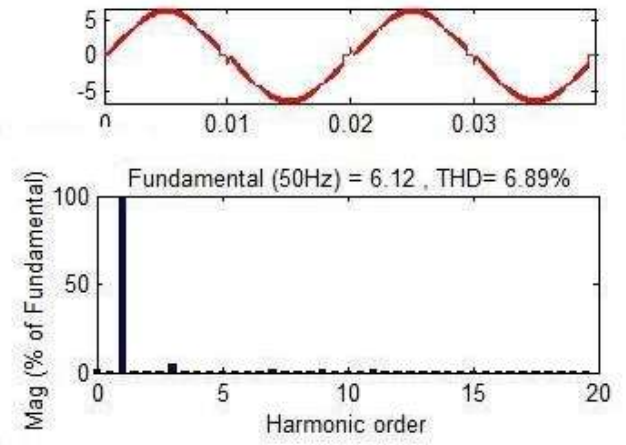

Fig. 8 Harmonic spectrum of series-switch five-level dual buck full bridge inverter

Fig. 7 & 8 shows the current THD of Three-level and five-level DBFBI. Three-level full bridge inverter is having 14.09 % and Five-level series -switch full bridge inverter with a THD of 6.89%. To attain a better THD in three-level, a higher value of filter inductor has to be placed.The proposed topology is simulated in the same conditions mentioned above. Fig. 9 shows output voltage waveform before and after filtering. Current THD is shown in Fig. 10. THD of single-inductor series -switch five-level dual buck full bridge inverter simulated in same conditions is 6.88%.

The voltage waveforms across switches S_1, S_3 and D_1 are shown in the Fig.11. It is clear that the maximum voltage across switch S_1 and S_3 are 0.5 U_{dc}. Maximum voltage stress across the diode D_1 is U_{dc}.

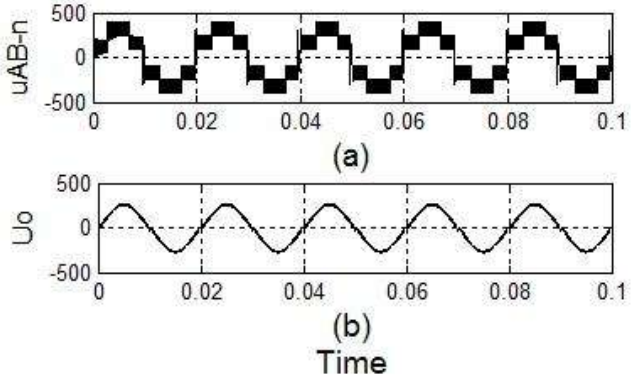

Fig. 9 Output voltage waveforms (a) with filter (b) without filter

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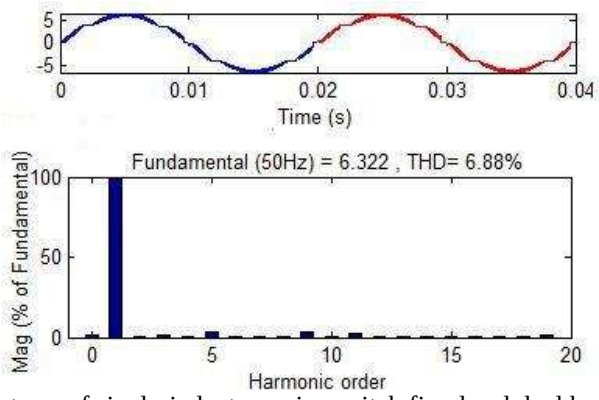

Fig. 10 Harmonic spectrum of single-inductor series switch five-level dual buck full bridge inverter

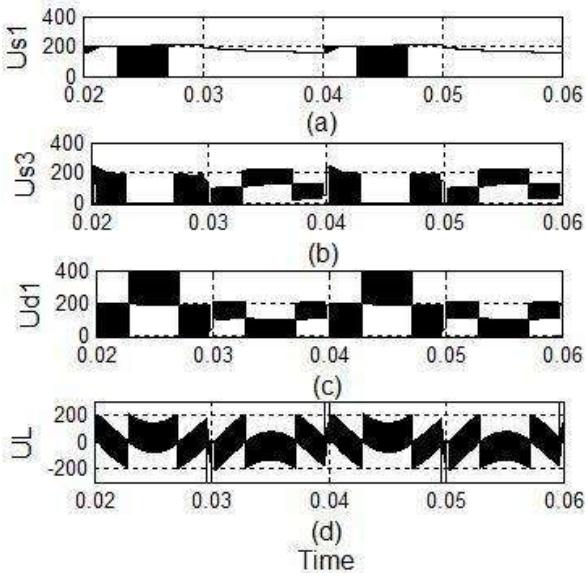

Fig. 11 Voltage waveforms across (a) switch S1 (b) switch S3 (c) diode D1(d) inductor (L)

The maximum voltage stress of inductor is 0.5Udc as shown in Fig.11.Since switch ratings are equal to half of the DC supply, the proposed topology can be utilized economically. The simulation results verify the theoretical analysis.

V. CONCLUSION

In this paper, a three-level dual buck full bridge inverter is compared with series-switch five-level dual buck full bridge inverter. Simulation results verify that for a better sinusoidal output (lesser THD) larger filter inductors are required. A novel five-level inverter topology having single-inductor is proposed in this paper. The proposed topology results in cost reduction and installation area since there is only one filter inductor. There is also a reduction in number of switches and diodes compared to conventional multilevel inverters. Reduction in voltage stress across switches operating at high frequency is another added advantage of the proposed topology. The simulation results for proposed multilevel inverter topology validates its satisfactory performance. The proposed topology finds application in areas where high reliability is required.

REFERENCES

[1] Z.Yao, L.Xiao, and Y.Yan, "Dual-buck full bridge inverter with hysteresis current control," *IEEE Trans. Ind. Electron*., vol.56, no.8, pp.3153–3160, Aug. 2009.
[2] Z. Yao and L. Xiao, "Two-switch dual-buck grid-connected inverter with hysteresis current control," *IEEE Trans. PowerElectron*., vol. 27, no. 7, pp. 3310–3318, Jul. 2012.
[3] Jun Liu, Yanyangguan, "A Novel Hysteresis Current Controlled Dual Buck Half Bridge Inverter," Journal of Nanjing University of Aeronautics Astronautics, vol. 36. no.2, 2003.
[4] Henghua Zhu, Fanghua Zhang, Yangguang Yan,, "A Novel Split Phase Dual Buck Half Bridge Inverter", *IEEE Appl. PowerElectron*. Conf., pp. 845849. Mar. 2005.

[5] P. Sun, C. Liu, J-S. Lai, and C-L. Chen, "Cascade dual buck inverter with phase-shift control," *IEEE Trans. Power Electron*., vol. 27, no. 4, pp. 2067–2077, Apr. 2012.
[6] P. Sun, C. Liu, J-S. Lai, and C-L. Chen, "Grid-tie control of cascade dual buck inverter with wide-range power flow capability for renewable energy applications," *IEEE Trans. Power Electron*., vol.27, no.4, pp.1839–1849, Apr. 2012.
[7] Baifeng Chen, Bin Gu, Jih-Sheng Lai, WensongYu, Chien-Yu Lin, and Cong Zheng, "Current Distortion Correction in Dual BuckPhotovoltaic Inverter with a Novel PWM Modulation and Control Method", *IEEE Appl. Power Electron*. Conf., p. 727 – 731, 2013.
[8] José Rodríguez, Jih-Sheng Lai, and Fang Zheng Peng, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications",*IEEE Trans. Ind. Electron*., vol. 49, no. 4, pp. 724–738, Aug.2002.
[9] Jun Liu, Huizhen Wang, YangguangYan, "A Novel Three Level Dual Buck Half Bridge Inverter", *IEEE Power Electron*. Conf., p. 483 – 487, 2008.
[10] Nong Sun, Li Zhang, Yan Xing, Ming Xu, Yu Fang, Xudong Ma, "A Five Level Dual Buck Full Bridge Inverter with Neutral Point Clamp for Grid Connected PV Application", *IEEE Conf. Ind. Electron*., pp. 1041 - 1045, Nov. 2011.
[11] Li Zhang, Kai Sun, Yan Xing,and Jinquan Zhao, "A Family of Five Level Dual Buck Full Bridge Inverters for Grid-Tied Applications" , *IEEE Trans. Power Electron*., vol. 31, no. 10, pp. 7029 - 7042, year. 2016.
[12] F. Hong, J. Liu, B. Ji, Y. Zhou, J. Wang, and C. Wang, "Single inductor dual buck full-bridge inverter," *IEEE Trans. Ind. Electron*., vol. 62, no. 8, pp. 4869–4877, Aug. 2015.
[13] Liwei Zhou, Feng Gao, "Dual Buck Inverter with Series Connected Diodes and Single Inductor", *IEEE Appl. Power Electron*. Conf., pp. 2259 - 2263. Mar. 2016.

BIOGRAPHIES

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