

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering



NCAEE 2017 National Conference on Advances in Electrical Engineering NMAM Institute of Technology, Nitte Vol. 5. Special Issue 2. April 2017

Two Input Boost Stage, High Gain DC-DC Converter

Ashwini.K.P¹, Mahabaleshwara Sharma K²

PG scholar, Electrical and Electronics Engineering, NMAMIT, Nitte, India¹

Assistant professor, Electrical and Electronics Engineering, NMAMIT, Nitte, India²

Abstract: A two input boost stage power electronic DC-DC converter with high voltage gain is put forward. From the input sources, a continuous current is being drawn using proposed topology. Using the proposed converter it is easy to attain a gain of 20 along with the advantage of drawing continuous current from input. The procedure for selection of components and design of components for the proposed converter is described. The suggested converter with V_{in} =20, V_{out} =400V and power rating 400W is verified by simulating in MATLAB.

Keywords: renewable energy source, boost converter, high voltage gain, voltage multiplier stage.

I. INTRODUCTION

application of dc-dc converter with high voltage gain is multiplying stages increases, there is rapid increase in increasing in green energy system. They find applications in high intensity discharge lamp for automobile headlamps, servo motor drives, X-ray power generators, regulation and converter efficiency [17]. computer periphery power supplies and uninterruptible power supplies [1].

In classical buck-boost, boost converter large switch duty ratios are needed to attain a high voltage gain. High current stress is created due to large duty cycle in the boost switch. Parasitic resistive components limit the maximum voltage gain in the circuit and because of large duty ratio efficiency is dramatically decreased. Furthermore converter efficiency is decreased due to large ripples on the output voltage and input current [2]. Usually to attain high conversion ratios of voltage, use of coupled inductor or high frequency transformer is in practice [3-12]. To attain large gains, transformers need higher number of understanding, proposed topology with four voltage winding turns. This results in complicated design of transformer and increased leakage inductances because of which voltage spikes are seen across the switch. To suppress these voltage spikes voltage clamping methods are used.

A new DC-DC converter with high voltage gain is presented to attain high voltage conversion ratio. Like a multiport converter, the new converter is able to draw power from two independent dc sources [13,14]. Low current ripple continuous input current is drawn from input sources and which is necessary in applications like solar. To minimise voltage stress on the switches numerous diode capacitor stages are cascaded which also boost voltage gain of converter.

Cockcroft-Walton voltage multiplier, interleaved boost converter is also a similar converter[15,16]. The

As use of renewable sources is increasing rapidly, disadvantage of this converter is that as the number of output impedance. For higher gains output impedance increases, which directly affect the output voltage

II. OVERVIEW OF TOPOLOGY AND OPERATING MODES

The presented topology in this paper is motivated from Dickson charge pump[20]. Two interleaved boost stages are cascaded with capacitor diode voltage multiplier stages. The purpose of voltage multiplier stage is to amplify the output from two boost stages in overall to attain higher voltage gain. Total number of voltage multiplier stages and switch duty ratio of boost stage decides the overall voltage gain of converter. For good multiplier stage is shown fig 1. Similar study is possible for N stage converter.



(2)



International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering **NCAEE 2017**



National Conference on Advances in Electrical Engineering

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During operation of proposed topology when both switches are conducting, there is always overlapping time which means either of the switches is always conducting as shown in fig 2. Therefore topology has 3 operating modes.



Fig. 2.Switching signals for input boost stage

A. MODE 1

Switches S1 and S2 are always conducting in this mode of operation. Input sources V_{ip1}, V_{ip2} are continuously charging inductors which result in linear increase in current through inductor. Voltage multiplier stage diodes and output diode D_{op} are not conducting since they are reverse biased. Only means of supplying load is output capacitor Cop because the voltages of capacitors of voltage multiplier stage are unaltered.

B. MODE 2

Only switch S2 is conducting in this mode of operation. Since switch S2 is ON it forward biases all odd numbered diodes. All the odd numbered capacitors charged and even numbered capacitors are discharged due to the flow of inductor current IL1. Output diode Dop reverse biases, output capacitor supplies load when there are odd number of voltage multiplier stages otherwise output diode forward biases and charges output capacitor when number of voltage multiplier stages are even.

C. MODE 3

Only switch S1 is conducting in this mode of operation. Since switch S1 is ON it forward biases all even numbered diodes. All the odd numberedcapacitors discharged and even numbered capacitors are charged due to the flow of inductor current IL2. Output diode Dop reverse biases, output capacitor supplies load when there are even number of voltage multiplier stages otherwise output diode forward biases and charges output capacitor when number of voltagemultiplier stages are odd.

III.CONVERETR VOLTAGE GAIN

Voltage multiplier stage continuously transfers charge from input to output.

Node voltages of upper boost stage

$$V_{C1} = V_{C3} - V_{C2} = V_{op} - V_4 = \frac{V_{ip1}}{1 - D_1}$$
(1)
where D₁ is duty cycle of switch 1.

Node voltages of lower boost stage

 $V_{C2} - V_{C1} = V_{C4} - V_{C3} = \frac{V_{ip2}}{1 - D_2}$ Where D_2 is duty cycle of switch 2. From (1) and (2)

$$V_{C1} = \frac{V_{ip1}}{1 - D_1}$$

$$V_{C2} = \frac{V_{ip1}}{1 - D_1} + \frac{V_{ip2}}{1 - D_2}$$

$$V_{C3} = \frac{2V_{ip1}}{1 - D_1} + \frac{V_{ip2}}{1 - D_2}$$

$$V_{C2} = \frac{2V_{ip1}}{1 - D_1} + \frac{2V_{ip2}}{1 - D_2}$$
Output voltage from equation (2)

Outp

$$\begin{split} V_{op} &= V_{C4} + \frac{V_{ip1}}{1 - D_1} \\ V_{op} &= \frac{3V_{ip1}}{1 - D_1} + \frac{2V_{ip2}}{1 - D_2} \end{split}$$

Generalised equations for capacitor voltages of P number of voltage multiplier stages

$$V_{Cq} = \left[\frac{q+1}{2}\right] \frac{V_{ip1}}{(1-D_1)} + \left[\frac{q-1}{2}\right] \frac{V_{ip2}}{(1-D_2)}$$

where q is odd and q<=P
$$V_{Cq} = \left[\frac{q}{2}\right] \frac{V_{ip1}}{(1-D_2)} + \left[\frac{q}{2}\right] \frac{V_{ip2}}{(1-D_2)}$$

$$V_{Cq} = \left\lfloor \frac{1}{2} \right\rfloor \frac{1}{(1 - D_1)} + \left\lfloor \frac{1}{2} \right\rfloor \frac{1}{(1 - D_2)}$$

where q is even and q<=P

Output voltage equation depending on whether number of stages is even or odd

$$V_{op} = V_{CP} + \frac{V_{ip2}}{(1 - D_2)}$$
$$V_{op} = \left[\frac{P + 1}{2}\right] \frac{V_{ip1}}{(1 - D_1)} + \left[\frac{P + 1}{2}\right] \frac{V_{ip2}}{(1 - D_2)}$$
en P is odd

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$$V_{op} = V_{CP} + \frac{V_{ip1}}{(1 - D_1)}$$
$$V_{op} = \left[\frac{P + 2}{2}\right] \frac{V_{ip1}}{(1 - D_1)} + \left[\frac{P}{2}\right] \frac{V_{ip2}}{(1 - D_2)}$$

when P is even

IV.CHOICE OF COMPONENTS

A. Selection of inductor

Procedure for inductor design is same as that of regular boost converter. Choice of value of inductor should be such that continuous conduction mode of boost stage is ensured.

Minimum value of inductor required is calculated as below

$$L_{1min} = \frac{V_{ip1}D_1(1-D_1)}{(P+1)I_{op}F_s}$$

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Vol. 5, Special Issue 2, April 2017

$$L_{2min} = \frac{V_{ip\,2}D_2(1-D_2)}{(P+1)I_{op}\,F_s}$$

L

when P is odd
$$V_{ip1}D_1(1-D_1)$$

$$\frac{1}{(P+2)I_{op}F_s}$$

(P+2) $I_{op}F_s$
when P is even

 $L_{2min} = \frac{V_{ip\,2}D_2(1-D_2)}{(P)I_{op}\,F_s}$

where P is the number of voltage multiplier stages.

B. Selection of capacitor

The choice of capacitor relies on the factor that how much quantity of charge the specific capacitor can transfer to output for required output voltage ripple and is given by

$$q_{op} = C_{op} \Delta V_{op} = \frac{I_{op}}{F_s} (1 - D)$$

Where D can be D_1 or D_2 depending on the number of voltage multiplier stages.

V. SIMULATION RESULTS

Switching frequency of converter is 100KHz. Components list for experimental prototype is given below.

Component	Reference	Rating	Part no
Inductor	L_{1}, L_{2}	100µH	
MOSFET	<i>S</i> ₁ , <i>S</i> ₂	55V,45A	IRFZ44N
		$R_{DS(on)} =$	
		$17.5 \text{m}\Omega$	
Diode	D_1, D_2, D_3, D_4	400-	MUR840/
	D_{op}	600V,8A	860
Capacitor	C_1, C_2, C_3, C_4	20µf	
Capacitor	C _{op}	22µf	

TABLE I COMPONENT LIST

A comprehensive simulation model of two input boost stage power electronic DC-DC converter with high voltage gain is presented below.



Fig.3. MATLAB model for proposed topology

Here batteries are used for both the input sources. Output voltage of converter is compared with constant value to generate error signal. This error signal is given to PID controller. The error signal compared with a reference signal to generate PWM signal. Generated PWM signal is given as gate pulses for switches.





VI.CONCLUSION

The main feature of this topology is diode capacitor voltage multiplier stage. Number of voltage multiplier stage decides the voltage gain. It can draw continuous current from input sources. This topology can be connected to independent energy sources. Successful simulation of the converter was conducted and for input voltage of 20V, an output of 400V was obtained with a gain of 20.

ACKNOWLEDGMENT

I would like to thank my guide **Mr.Mahabaleshwara Sharma K,** Assistant Professor, NMAMIT, Nitte. I sincerely express my gratitude to our Project Coordinator **Mr.K.VasudevaShettigar**, Associate Professor and our HOD **Dr.NageshPrabhu**, Professor and Head, Department of E&EEngg, N.M.A.M Institute of Technology, Nitte for their timely scheduling of the project work and encouraging us to present papers.



International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering NCAEE 2017



National Conference on Advances in Electrical Engineering

NMAM Institute of Technology, Nitte Vol. 5, Special Issue 2, April 2017

REFERENCES

- [1] Esam H. Ismail, Mustafa A. Al-Saffar, Ahmad J. Sabzali, and Abbas A. Fardoun, "A Family of Single-Switch PWM Converters With High Step-Up Conversion Ratio," IEEE Trans. on Circuits and Systems-I: Regular Papers, vol. 55, no. 4, pp. 1159–1171, May 2008.
- [2] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, 2nd ed. Norwell, MA: Kluwer Academic Publishers, 2001.
- [3] W. Li, and, and X. He, "A family of interleaved DC-DC converters deduced from a basic cell with winding-cross-coupled inductors (WCCIs) for high step-up or step-down conversions," IEEE Trans. on Power Electronics, vol. 23, no. 4, pp. 1791-1801, Jul. 2008.
- [4] W. Li, and X. He, "An interleaved winding-coupled boost converter with passive lossless clamp circuits," IEEE Trans. on Power Electronics, vol. 22, no. 4, pp. 1499-1507, Jul. 2007.
- [5] W. Li, Y. Zhao, Y. Deng, and X. He, "Interleaved converter with voltage multiplier cell for high step-up and high-efficiency conversion," IEEE Trans. on Power Electronics, vol. 25, no. 9, pp. 2397-2408, Sep. 2010.
- [6] Yi-Ping Hsieh, Jiann-Fuh Chen, Tsorng-Juu Liang, and Lung-Sheng Yang, "A novel high step-up DC–DC Converter for a microgrid system," IEEE Trans. on Power Electronics, vol. 26, no. 4, pp. 1127-1136, Apr. 2011.
- [7] R. Xie, W. Li, Y. Zhao, J. Zhao, X. He, and F. Cao, "Performance analysis of isolated ZVT interleaved converter with winding-crosscoupled inductors and switched-capacitors," in Proc. IEEE Energy Conversion Congress and Exposition (ECCE), Atlanta, USA, 2010, pp. 2025-2029.
- [8] Wuhua Li, Weichen Li, Xiangning He, David Xu, and Bin Wu, "General derivation law of nonisolated high-step-up interleaved converters with built-in transformer," IEEE Trans. on Industrial Electronics, vol. 59, no. 3, pp. 1650-1661, Mar. 2012.
- [9] Kuo-Ching Tseng, Chi-Chih Huang, and Wei-Yuan Shih, "A high step-up converter with a voltage multiplier module for a photovoltaic system," IEEE Trans. on Power Electronics, vol. 28, no. 6, pp. 3047-3057, Jun. 2013.
- [10] Wuhua Li, Yi Zhao, Jiande Wu, and Xiangning He, "Interleaved high step-up converter with winding-cross-coupled inductors and voltage multiplier cells," IEEE Trans. on Power Electronics, vol. 27, no. 1, pp. 133-143, Jan. 2012.
- [11] Kuo-Ching Tseng, and Chi-Chih Huang, "High step-up highefficiency interleaved converter with voltage multiplier module for renewable energy system," IEEE Trans. on Industrial Electronics, vol. 61, no. 3, pp. 1311-1319, Mar. 2014.
- [12] Kuo-Ching Tseng, and Chi-Chih Huang, "A high step-up passive absorption circuit used in non-isolated high step-up converter," in Proc. IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, USA, 2013, pp. 1966-1971.
- [13] K. Gummi and M. Ferdowsi, "Synthesis of double-input DC-DC converters using single pole triple throw switch as a building block," in Proc. IEEE Power Electronics Specialists Conf. (PESC), Rhodes, Greece, 2008, pp. 2819-2823.
- [14] V. A. K. Prabhala, D. Somayajula and M. Ferdowsi, "Power sharing in a double-input buck converter using dead-time control", in Proc. IEEE Energy Conversion Congress and Exposition (ECCE), San Jose, USA, 2009, pp. 2621-2626.
- [15] Sanghyuk Lee, PyosooKim,andSewan Choi, "High step-up softswitched converters using voltage multiplier cells," IEEE Trans. on Power Electronics, vol. 28, no. 7, pp. 3379-3387, Jul. 2013.
- [16] Chung-Ming Young, Ming-Hui Chen, Tsun-An Chang, Chun-Cho Ko, and Kuo-Kuang Jen, "Cascade Cockcroft–Walton Voltage Multiplier Applied to Transformerless High Step-Up DC–DC Converter," IEEE Trans. on Industrial Electronics, vol. 60, no. 2, pp. 523-537, Feb. 2013.
- [17] John F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," IEEE Journal of Solid-State Circuits, vol. 11, Issue: 3, pp. 374-378, Jun. 1976.