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### SITES

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## A Five Level Three Phase Cascaded Inverter

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Abstract: This paper present the five level three phase cascaded inverter. This paper focuses on improving the efficiency of the multilevel inverter and quality of output voltage waveform. The modified PWM technique is also developed to reduce harmonics. Five level reduced switches topology has been implemented with only 24 switches. Fundamental Switching scheme and Selective Harmonics Elimination were implemented to reduce the Total Harmonics Distortion (THD) value and switching losses. The simulation diagrams of multilevel inverter are carried out in MATLAB (R2013A) / Simulink environment to evaluate the performance of the system.

Keyword: Multilevel Inverter, Sinusoidal Pulse Width Modulation, Total Harmonics Distortion.

### **I. INTRODUCTION**

Several industrial and commercial applications have begun also can be decrease the dv/dt protection; consequently to require large power appliances in recent years. Some electromagnetic compatibility (EMC) problems can be high and medium voltage motor drives and utility reduced. applications require voltage and megawatt power level. • Common-mode (CM) voltage: Multilevel inverters For a grid voltage and current, it is difficult to use only produce slighter CM voltage; therefore, the stress in the one power semiconductor switch directly [1-2]. As a bearings of a load connected to a multilevel load drive can result, a multilevel power inverter structure has been be reduced. [11]. introduced for alternative in high power and medium • Input current: Multilevel inverters can draw input voltage condition. A multilevel inverter not only achieves current with low harmonics distortion. high power ratings, but also enables the use of renewable • Switching frequency: Multilevel inverters can operate at energy sources like photovoltaic, wind, and fuel cells can both fundamental switching frequency and carrier be easily interfaced to a multilevel inverter system for a high and medium power application [3].

The idea of multilevel inverters has been introduced since 1975 [4]. The term multilevel began with the 3-level multilevel inverter [5]. Subsequently, several multilevel inverter topologies have been developed [6-12]. However, the elementary concept of a multilevel inverter to achieve higher power is to use a series of power semiconductor switches with numerous lower voltage direct current (dc) sources to execute the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to get high voltage at the output.

A multilevel inverter (MI) has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel inverter can be briefly summarized as follows.

• Staircase waveform: Multilevel inverters not only can generate the output voltages with very low distortion, but

switching frequency PWM. It should be noted that lower switching frequency generally means lower switching loss and higher efficiency.

Unfortunately, multilevel inverters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed. Although lower voltage rated switches can be utilized in a multilevel inverter, each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex.

### **II. CONTROL APPROACHES**

The main aim of the modulation strategy of cascaded multilevel inverters is to produce the output voltage as close as possible to the sinusoidal voltage waveform. Various modulation approaches have been developed for harmonic reduction and minimization of switching losses. The modulation techniques used in cascaded multilevel inverters can be classified according to switching frequency. Methods that works with high switching frequencies has many commutations for the power semiconductors in one period of the fundamental output



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Gyan Ganga College of Technology Vol. 4, Special Issue 4, November 2016

voltage. A very accepted method in industrial and Fundamental output voltages can be controlled by commercial applications is the sinusoidal PWM (SPWM) changing a modulation index (ma) of referent signal; also, that uses the phase-shifting technique to reduce the the fundamental output frequency can be adjusted by harmonics in the load voltage.

### **III. SINUSOIDAL PULSE WIDTH MODULATION** (SPWM) CONTROL

The control techniques based on the PWM solve the problem of switching frequency of the VSI. They use a fix switching frequency which makes it easier to cancel the switching harmonics. The PWM can be realized using different techniques such as carrier based PWM, PWM with harmonics minimization, and space vector PWM. The carrier PWM can be natural PWM, symmetric PWM, and asymmetric PWM. The most simple and well known PWM technique is the sinusoidal PWM. This technique uses a controller which determines the voltage reference of the inverter from the error between the measured current and its reference. This reference voltage is then compared with a triangular carrier signal (with high frequency defining the switching frequency). The output of this comparison gives the switching function of the VSI. The choice of the ratio between the frequency of the reference signal and the frequency of the carrier signal is very important in the case of symmetric and periodic reference. As a consequence, in the case of sinusoidal reference, the ratio between the two frequencies must be integer to synchronize the carrier with the reference. Over more, it is preferable that the carrier frequency be odd to conserve the reference symmetry. In all cases this ratio must be sufficiently high to ensure the fast switching and to take the switching harmonics away from the fundamental produced by the inverter.

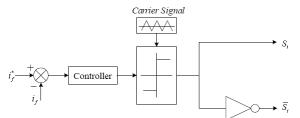


Fig 1. The principle of sinusoidal PWM control method

Recently, new control techniques called space vector PWM were implemented. The difference between this technique and the sinusoidal technique is that it doesn't use carrier signal to define switching orders [11].

### **IV. SIMULATION AND RESULTS**

The proposed system can be simulated using MATLAB (2013a) software. In this system MOSFET switches are used to operate CMI and total 24 mosfet switches are used.

changing frequency of the referent signal. The simulation results of the proposed five level inverter are shown in Fig.2 and the corresponding FFT analysis is shown in fig 7.

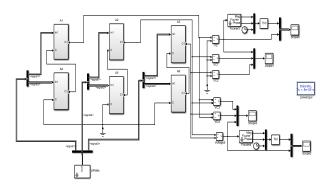


Fig 2. five level cascaded inverter simulink model

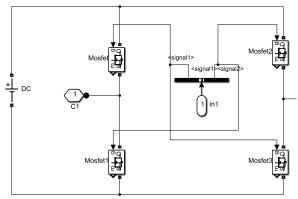


Fig 3. one H-bridge inverter

The pulse generator is shown in the Fig. 4 and those pulses generated are to drive the devices in to ON for a five level inverter topology.

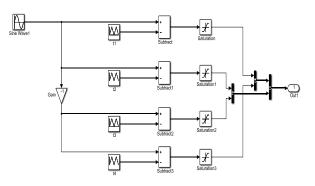


Fig 4. Sinusoidal pulse width modulation

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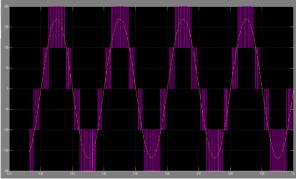


Fig 5. output voltage of the multilevel inverter

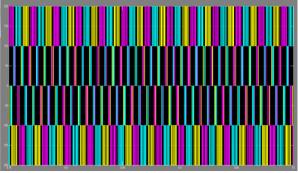


Fig 6. Phase to ground voltage of multilevel inverter

Total harmonic distortion, or THD, is the summation of all harmonic components of the voltage or current waveform compared against the fundamental harmonics component of the voltage or current signals. Total harmonics distortion (THD) calculations can be obtained from the SIMULINK.

The switching pattern that is used in this project for all of the multilevel inverters is Sinusoidal PWM technique. In this method the switching angles for switches should be calculated in such a way that the dominant harmonics are eliminated (minimized). For a 5-level inverter the 5th harmonic will be eliminated.

%THD = 
$$\sqrt{(v^2 + v^3 + v^4 - \dots + v^2)/v^2}$$
....(1)

Where, v1= Fundamental Voltage amplitude

- v2 = Magnitude of 2nd fundamental Harmonic
- v3 = Magnitude of 3rd fundamental Harmonic.
- vn = Magnitude of nth fundamental Harmonic

The formula above 1 shows the calculation for total harmonics distortion (THD) on a voltage signal. The end [3] result is a percentage comparing the harmonic components to the fundamental frequency component of a signal. The upper the percentage, the more distortion that is present on [4] the mains signal.

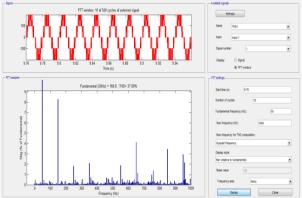
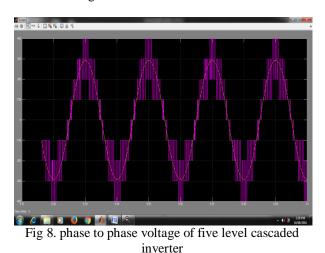


Fig 7. Total harmonic distortion



### **V. CONCLUSION**

A Five level cascaded multilevel Inverter is designed. The simple popular sinusoidal pulse width modulation technique with switching frequency of 2.5 KHz is considered for investigation. The results show that cascaded multilevel inverter topology can be applied for high power applications as a multilevel inverter. CMI received higher efficiency with less harmonics content. Simulation results have been validated.

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