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Simulation of High Static Gain Modified SEPIC Converter

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Abstract: In this paper modified SEPIC converter is preferred and based on preferred converter two types of step-up converters with high static gain are presented. These preferred converters are required to obtain high output voltage for applications which are supplied by low input voltage sources .The preferred converters are modified SEPIC converter without magnetic and with magnetic coupling . These two converters increases static gain and efficiency keeping switch voltage low. Also to limit crises of overvoltage at the output diode in the preferred converter with magnetic coupling, voltage multiplier is included in secondary part. This voltage multiplier raises static gain and it also considered as non-dissipative clamping circuit. The preferred converter with magnetic coupling comprises of leakage inductance of transformer and voltage multiplier which reduces losses. Simulation of these two proposed converters are done using MATLAB/SIMULINK and output results are compared.

Keywords: SEPIC converter , static gain , magnetic coupling , non-dissipative clamping circuit

I. INTRODUCTION

The converters having static gain which is high are required for many applications which are powered by low dc power sources. The renewable energy sources are low power sources [1] . To get high static gain the usual solution is isolated converters. In these type of converters transformer turns ratio raises static gain. But due to losses in transformer and leakage inductance there is reduction in efficiency . Converter weight and volume also raised due to the transformer. Therefore to increase efficiency, the usual solution is non isolated dc dc converters. However static gain (q = Vo /Vi) of these type of converters is limited for example conventional boost converter. In boost converter it is difficult to get high static gain and to increase efficiency simultaneously .

This is due to the presence of parasitic resistances, which decreases step-up ratio and efficiency as duty cycle increases. For this reason many solutions were considered to raise static gain of non isolated converter to obtain high efficiency and high power density solutions. Main solutions are the switched capacitors, switched inductors [2],[3] ,voltage multiplier cells[4]-[6] , inductor magnetic coupling [7]-[9] and combinations of these solutions. The modified SEPIC converter is presented in this paper to obtain high output voltage for applications which are provided by low input voltage sources .Thus there are two types of topologies based on modified SEPIC converter . One is modified SEPIC converter without magnetic coupling and other is with magnetic coupling .

The modified SEPIC converter without magnetic coupling presents a static gain which is approximately double of the static gain of boost converter and switch voltage is also equal to the half value of the boost converter for high values of duty cycle operation. The other preferred converter using a magnetic coupling includes a secondary winding in inductor of converter, which helps in increasing the static gain.

However in this part of the power which is generated by converter gets transfer to the output via coupling inductor and another part of power get transfer directly by non isolated converter and due to this losses of the transformer , weight and volume of converter gets reduce . Also the leakage inductance plays important role in this topology to get ZCS turn-on commutation and to limit reverse recovery current of diodes, which raises efficiency of converter. The simulations and comparison of both preferred converters are presented in this paper .

II. PREFERRED SEPIC CONVERTER WITHOUT MAGNETIC COUPLING

The SEPIC converter is shown in Fig. 1. Static gain of SEPIC converter can be step –up and step – down which is very important for different ranges of input voltage . Also total of input and output voltages is equal to voltage switch of SEPIC converter and due to this reason static gain is less than step –up converter i.e classical boost converter . For this reason SEPIC converter is modified to increase its static gain .

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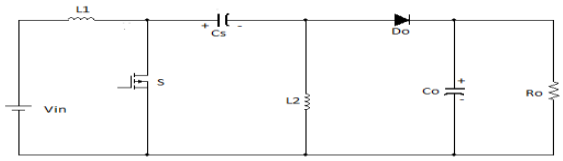

Fig.1. SEPIC converter

A. Preferred Converter without Magnetic Coupling

In this preferred converter D_m and C_m are included which increases static gain . Also output voltage of boost converter charges C_m and also polarity of C_s is changed .

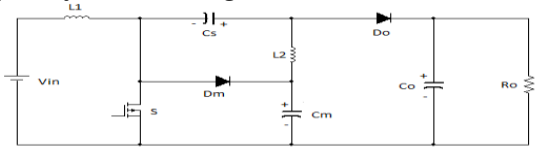

Fig.2. Preferred converter without magnetic coupling

B. Working Principle

Consider preferred converter without magnetic coupling conducts in continuous conduction mode and it includes two stages. For analysis assume all capacitors as a voltage source and semiconductors to be ideal First Stage : In this stage switch S turns-on the diodes D_m and D_o gets block and energy gets store in the inductors L_1 and L_2. Input voltage is given to input inductor L_1 and the voltage V_{cm} - V_{cs} is given to inductor L_2.

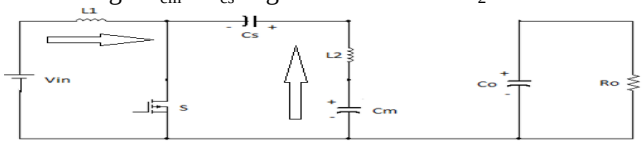

Fig.3. First stage

Second Stage : In this stage switch S is turns-off and the diode Dm and Do gets forward biased . The stored energy in L_1 gets transfer to the output through the C_s and D_o and also it gets transfer to C_m through D_m . Due to this the switch voltage is equal to the C_m voltage. Energy stored in L_2 gets transfer to output through Do.

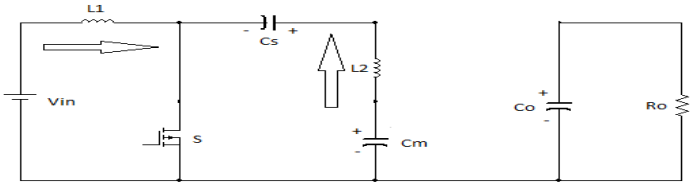

Fig.4. Second stage

Important characteristics of this topology are :

Voltage of all diodes and switch are nearly equal to C_m voltage.

Sum of the C_s and C_m capacitors voltage equal to output voltage.

Input current is equal to average L_1 inductor current and output current is equal to average L_2 inductor current .

Static gain is obtained by integrating the voltage across L_1 and L_2 over a time period T equal to zero yields

L1 : $V_{in}DT + (V_{in} - V_{cm})(1 - D)T = 0$

$V_{in}D + V_{in} - V_{in}D - V_{cm} + V_{cm}D = 0$

$V_{in} - V_{cm}(1 - D) = 0$

$V_{in} = V_{cm}(1 - D) = 0$

$V_{in} = V_{cm}(1 - D)$

$V_{cm} = V_{in}/(1 - D)$ (1)

L2: $(V_{cm} - V_{cs})DT + (V_{cm} - V_o)(1 - D)T = 0$

$V_{cm}D - V_{cs}D + V_{cm} - V_{cm}D - V_o + V_oD = 0$ (2)

As $V_o = V_{cm} + V_{cs}$ (3)

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Substitute equation (3) in (2)

$$-(V_o - V_{cm})D + V_{cm} - V_o + V_oD = 0$$
$$-V_oD + V_{cm}D + V_{cm} - V_o + V_oD = 0$$
$$V_{cm}(1+D) = V_o$$
$$V_{cm} = V_o / (1+D) \quad (4)$$

Comparing equation (1) & (4) we get

$$V_o / V_{in} = (1+D)/(1-D) \quad (5)$$

Comparing step –up converter i.e boost converter static gain is high .

Equation (1) represents capacitor C_m voltage and it is equal to maximum switch voltage . For this reason switch voltage is less than converter output voltage

Capacitor C_S voltage is calculated by

$$V_{cs} / V_{in} = D/(1-D) \quad (6)$$

C. Design Analysis

1. Switch Duty Cycle :$D = \frac{(V_o - V_{in})}{(V_o + V_{in})}$
2. Switch and Diodes Voltages $V_s = V_{DO} = V_{Dm} = \frac{V_{in}}{(1-D)}$
3. L_1 and L_2 Inductance $L_1 = L_2 = \frac{(V_{in} \times D)}{(\Delta iL \times f)}$
4. Capacitors C_s and C_m : Voltage ripple of the capacitors C_s and C_m are same. Assuming capacitor voltage ripple ΔV_C is approximately equal to 10 percent of voltage of the capacitor C_s , the capacitances of C_s and C_m are given as

$$C_s = C_m = \frac{I_o \times D}{(\Delta V_c \times f)} \quad \text{where } \Delta V_c = \frac{V_{in} \times D}{(1-D)} \times \left(\frac{10}{100}\right)$$

5. Diode Current : The average current of D_m and D_o are calculated as $I_{Do} = I_{Dm} = I_o = \frac{P_o}{V_o}$

III. PREFERRED SEPIC CONVERTER WITH MAGNETIC COUPLING

A. Preferred converter with Magnetic Coupling

The operation where duty –cycle is high ,static gain of preferred converter without magnetic coupling is twice of static gain of step –up converter i.e boost converter. However to get maximum static gain, the duty cycle of preferred converter without magnetic coupling must be high. Thus a secondary winding included in L_2 of preferred converter without magnetic coupling to raise static gain without raising voltage of switch and duty cycle , this inductor windings turns ratio (n) raises output voltage . The preferred converter with magnetic coupling is shown in Fig .5. However, preferred converter with magnetic coupling presents some limitation i.e due to D_o reverse recovery current , stored energy in leakage inductance causes voltage ring and high reverse voltage at D_o . Also the classical snubbers or dissipative clamping not able to control this overvoltage . For this reason the voltage multiplier is included at the secondary side. Voltage multiplier raises static gain of converter, also D_o voltage is decreased to value lesser than output voltage and stored energy in leakage inductance gets transfer to output. Thus voltage multiplier which includes D_{m2} and C_{S2} is consider as non dissipative clamping circuit for D_o. The preferred converter with magnetic coupling and output diode voltage clamping circuit shown in Fig.6 .

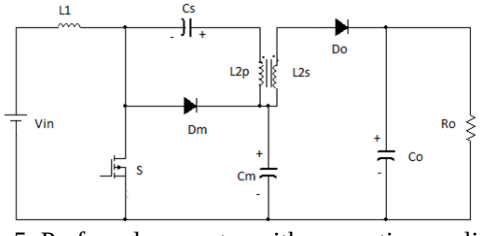

Fig.5. Preferred converter with magnetic coupling

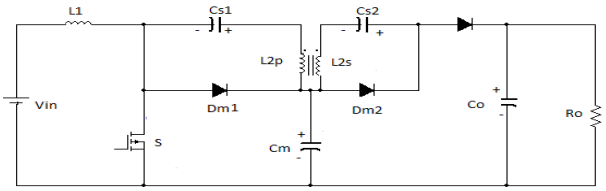

Fig.6. Preferred converter with magnetic coupling and output diode clamping

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B. Working Principle

Consider preferred converter with magnetic coupling and output diode clamping conducts in continuous conduction mode and it includes five stages. For analysis assume all semiconductors to be ideal and capacitors of converters as voltage source.

First Stage : In this stage switch S is in operating state and energy gets store in inductor L_1 . The C_{s2} gets charge by the L_{2s} and D_{m2} . Leakage inductance controls current and transfer of energy take place in a resonant way. The D_o gets block, and maximum D_o voltage is same as $(V_o - V_{cm})$. At end of this stage, when transfer of energy to the C_{S2} gets finish and D_{M2} gets block.

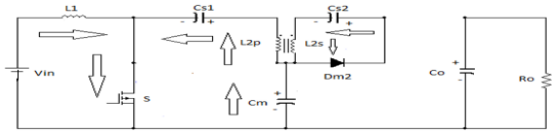

Fig.7. First stage

Second Stage : In this stage the D_{m2} gets block and energy gets store in L_1 and L_2 .

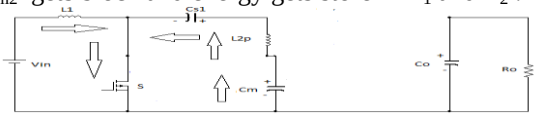

Fig.8.Second stage

Third Stage : In this stage , switch S turns OFF. The stored energy in L_1 gets transfer to C_m. Also, energy gets transfer to output via C_{S1}, C_{S2} , L_2 and D_O.

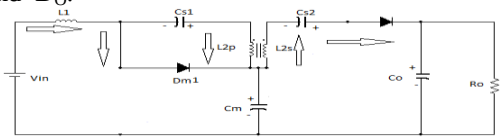

Fig.9. Third stage

Fourth Stage : In this stage when transfer of energy to the capacitor C_m gets finish, diode D_{m1} gets block. The transfer of energy to the output is retained till end of this stage.

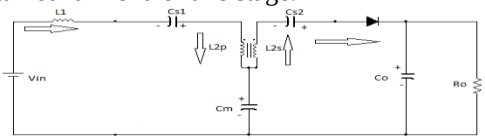

Fig.10. Fourth stage

Fifth Stage : In this stage , the switch gets turn ON and the current at the D_o linearly reduces and the transformer leakage inductance limits di/dt which limits reverse recovery current constraint of D_o . When the D_o gets block, converter returns back to the first stage.

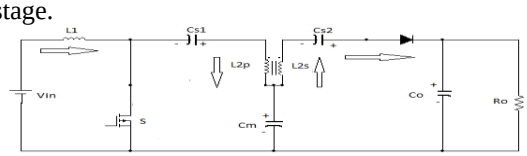

Fig.11. Fifth stage

The static gain is given by : $\frac{V_o}{V_{in}} = \frac{1}{(1-D)} \times (1 + n)$

Where (n) is inductor windings turns ratio which is given as $n = \frac{N_{L2S}}{N_{L2P}}$

Without raising switch voltage , the static gain can be raised by value of (n)

C. Design Analysis

1. Switch Duty Cycle is given as : $D = 1 - \frac{V_{in}}{V_o} \times (1 + n)$
2. Switch and Diodes Voltages are given as : $V_s = V_{Dm1} = \frac{V_{in}}{(1 - D)}$
3. The voltage of diode D_{m2} and diode D_o are equal and given as : $V_{Do} = V_{Dm2} = V_o - V_{cm} = n \times \frac{V_{in}}{(1 - D)}$

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4. L_1 and L_{2P}–L_{2S} Inductance: $L_1 = L_{2P} = \frac{(V_{in} \times D)}{(\Delta iL \times f)}$ $L_{2S} = n^2 \times L_{2p}$

5. Capacitors C_s and C_m : Assuming voltage ripple of capacitor C_{S2} is approximately equal to 10 percent of capacitor C_m voltage and value of capacitor C_{S2} is given as $C_{s2} = \frac{I_o \times D}{(\Delta V_c \times f)}$

Where $\Delta V_c = V_{in} \times \frac{D}{(1-D)} \times (10/100)$

The voltage ripple of capacitors C_{s1} and C_m are approximately equal . Assuming it is equal to be 15 percent of capacitor C_m voltage and value of capacitors C_{s1} and C_m is given as

$C_{s1} = C_m = \frac{(Io \times n \times D)}{(\Delta V_C \times f)}$ where $\Delta V_c = V_{in} \times \frac{D}{(1-D)} \times \frac{15}{100}$

6. Diode current : The average current of D_0 , D_{m1} , D_{m2} is given as $I_{Do} = I_{Dm1} = I_{Dm2} = I_o = \frac{P_o}{V_o}$

IV. SIMULATION RESULTS

Using MATLAB /SIMULINK model both preferred converters are simulated.
The parameters for preferred converter without magnetic coupling and with magnetic coupling are shown in this table.

Components required for preferred converter without magnetic coupling	Values of Components	Components required for preferred converter with magnetic coupling	Values of Components
Voltage Source	15V	Voltage Source	15V
Inductor L_1 & L_2	102µH	Inductor L_1	102µH
Capacitor C_s & C_m	3.37µF	Inductor L_{2p} & L_{2s}	102µH , 689.52µH
Capacitor C_o	1µF	Capacitor C_{s2}	3.3µF
Resistor	225 ohm	Capacitor C_{s1} & C_m	2.9µF
		Capacitor C_o	1µF
		Resistors	900 ohm

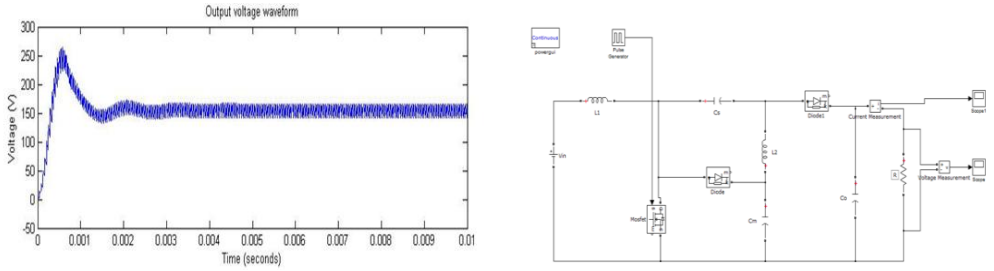

Fig.12. Simulation result of preferred converter without magnetic coupling

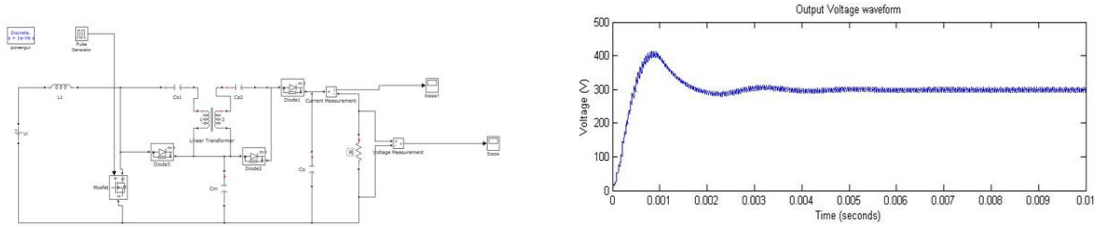

Fig.13. Simulation result of preferred converter with magnetic coupling

The simulation result are shown in Fig 12 and Fig 13 . From these results we observe that the output voltage which is obtained in preferred converter with magnetic coupling is double compared to preferred converter without magnetic coupling.

V. CONCLUSION

Two modified SEPIC converters having static gain which is high are introduced in this paper. The first preferred converter without magnetic coupling operate with a static gain higher than boost converter and second preferred converter with magnetic coupling operates with static gain higher than first preferred keeping voltage of switch low . Also output voltage of preferred converter with magnetic coupling is higher than preferred converter without

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magnetic couple .The leakage inductance of transformer and secondary voltage multiplier which considered as non dissipative clamping circuit to output diode limits losses of preferred converter with magnetic coupling .

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