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VLSI Implementation of Built-In Self Repair for Faulty Memory based on the Memory Address

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Abstract: In every application the memory is used to store the data and program etc. Based on the performance and requirement different memories are available. So the memory places almost direct impact on the performance of the application. During fabrication the fault may happen in the memory on the wafer or during use of the memory, due to some external disturbance or heat produced in the IC (Integrated Circuit) the memory may fail to work properly. So the memory testing is necessary even after fabrication and also during working of the memory by the user. If fault is found in the memory then repairing the fault is also important otherwise the application current work has to stop and the replacement of the IC is needed. So the implementation is done using built in self repair technique. Based on the address of each memory locations, if there is any fault in the memory then repairing is done by replacing the faulty memory with spare memories. Pointing the proper address is performed to access the proper data or to read from the memory.

Keywords: System on Chip (SoC), Built-In Self Repair (BISR), spare memory, Built-In Self Test (BIST)

I. INTRODUCTION

In the present scenario in System on Chip (SoC) memory places a large area than other circuitry [1] [3]. Memory is very important thing in these days to store any data, program and look up table etc. with this information many operations are performed for controlling, analysis, monitoring, comparison and entertainment etc. so the memory operation is very important, if memory fails to operate properly due to some external disturbance or heat produced in the IC then there is a chance of fail in the whole Operation of IC and replacement of the IC is needed. Also there is a chance of failure in the memory during fabrication so repairing is necessary.

The fault occurred in the fabrication is identified just after fabrication before embedding it in to the IC, the proper solution is taken just after fabrication. Let the other case if the memory is embedded into the IC and it is using in the field in the required application, let during this period the embedded memory fails. Then the solution is stop the current operation and change the IC by programming it again. Here there may be so much of loss occurs or any hazardous takes place, like in the military, automation field or in space application etc. this paper presents the solution for this type of fails occur in the memory.

If the fail is occurred in the embedded memory during operation and this is identified by the Built-In Self Test (BIST) circuitry then the Built-In Self Repair (BISR) circuitry will be activated to repair the faulty memory. There are so many techniques there to repair the memory, in this paper must repair analysis technique is used using solver circuitry for repairing the memory. In this method if there is any fault is found in the memory with respect to address of the memory then the faulty memory is replaced with the spare memory. The spare memory implementation again has different arrangements such as row spare memory, column spare memory and row & column spare memory. Here the column spare memory is implemented. When the fault is occurred in the embedded memory then solver circuitry first checks for the row addresses for whether the pointer is locating the proper row address or not, for data writing or for reading from the memory location [6]. If the pointer is not pointing to the proper location of the memory then it is corrected by this method [2]. The one more condition with respect to the memory address is column address, here if there is fault is found in the column address then that particular memory location is replaced with the spare memory. The spare memory has to be fabricated inside the IC along with solver and must repair circuitry.

II. DESIGN IMPLEMENTATION

The BISR implementation consists of two circuitries those are solver and must repair analyser. The BISR technique is online repair, means while processing is done by the IC then at the same time the repairing of the memory is performed if the memory location is faulty [5].

The block diagram of BISR is shown in figure 1 and the interconnection between solver and the must repair analyser is shown. Here the input is the address of the memory location which is given to solver the memory address pointing is dependent on the processing. The memory address is of thirty two bit in this both row

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address and column address is included. This address consist of both row and column address, based on this the memory location will be accessed. The solver circuit output is connected to the input of must repair analyser. The solver circuitry checks for row address and also column address for whether the address lies in the

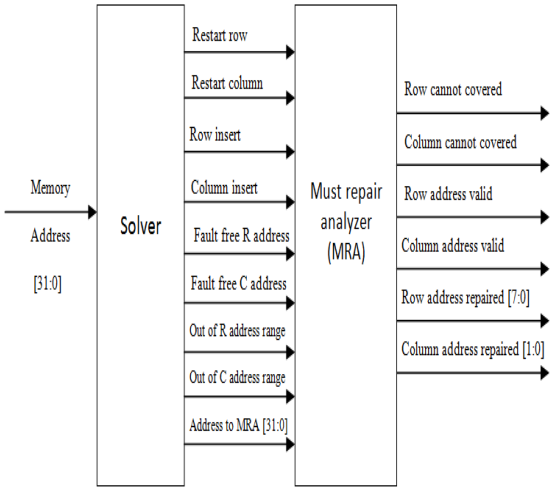

Fig. 1 Block diagram of built in self repair

preferred memory address or not is identified. While processing, if the memory is needed to access for writing the data or for reading from the memory the pointer will be locating the particular memory address. If the pointer is not pointing to the proper memory location then the solver circuitry will identifies that and gives signal to MRA. If it is pointing to proper address then no address will be sent to the MRA. When the input address is given to the solver then first it checks for whether the address lies in the memory location, if it is within the memory further process will be done otherwise not and the generated signal will be given to MRA by solver. The only signal given to the MRA will be out of row address range and out of column address range for repair. Similarly next it will check for row address as said early for proper pointing of the memory location, if it is not pointing to proper row address then for repairing of it the row address will be sent to MRA along with the signals restart row, row insert, fault free row address, out of row address range for repair. If row address is proper then MRA will not take any actions. Now after analysis of row address then it will start analysing of column address like same as did by the row address. First it will check for whether the column address lies in the proper memory range then check for the faulty column address. If it finds any fault in the column address then the signal will be sent to the MRA, those signals are restart column, column insert, fault free column address, out of column address and address to MRA.

Now the MRA gets faulty address of both row and column, this address is again processed in the must repair analyser for repair. First it will repair for the row address that is the address is considered as thirty two bit. It is divided as four eight bits each. So to access the whole thirty two bit it has to point to first eight bit memory address location. But here it is not pointing to the proper address so MRA will point to the proper memory location like this row address will be repaired. Now the row address will be checked for the repair. If the column address is faulty then that proper memory location will be replaced with the spare memory. Here the spare memory has to be fabricated based on the working environment of the particular IC and work load on IC. In the implementation total three spare memories are considered and it will be extended. The output of the MRA are row cannot covered, column can not covered, row address valid, column address valid, row address repaired and column address repaired. Here if the row address is out of range then the output row cannot covered signal will be high. Similarly same operation will be done for column address of the memory. If the row address is valid then the output signal related to it will be high that is row address valid signal will be high. If it is invalid then the row or column address will be repaired to the proper address and with the spare memory [8]. If the memory is repaired then the respected output signal will be high and the repaired memory address will be shown in the result.

III. RESULTS

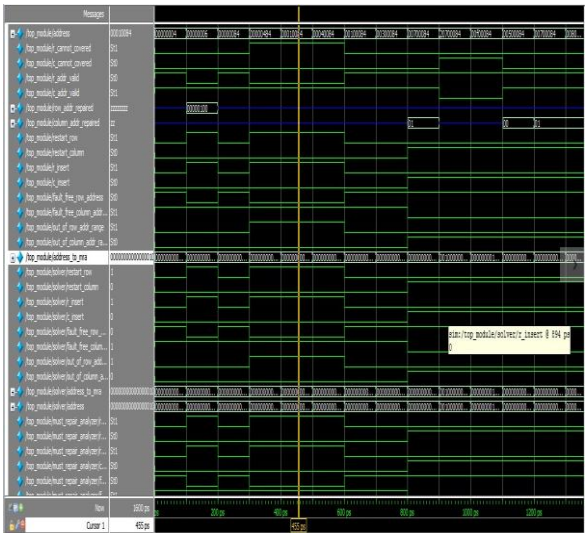

Fig. 2 Simulation waveform of built in self repair

The result of built in self repair is shown in the figure 2. Here all the conditions with respect to the memory addresses are shown in the simulation result. As shown in the figure let the address be 00010084 then the output results are row address is cannot covered is high because the row which is taken is not covered in the memory, c cannot covered is low, r address valid is low, c address valid be high, row address repaired is high impedance as row address cannot covered, column address valid is high impedance because the column address is within range and valid, restart row high, restart column be low, r insert high, c insert is zero, fault free row address low, fault free column address is high, out of row address range is high,

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out of column address range is low, address to mra is the same address will be sent to MRA circuitry. In this manner the output will be obtained for both row address and column address with respect to spare memory.

IV. CONCLUSION AND FUTURE WORK

The memory fault that occurs may be due to external environment disturbances or due to heat produced in the IC, the memory repairing technique is done with the help of solver and must repair analyser circuitry. This is implemented only with the help of memory address which contains both row and column address. This technique is implemented with online repairing. With respect to the row and column address the particular memory is within the specified memory location or not, row and column are covered, row and column address is valid, fault free row and column address these all conditions are checked. The particular proper signal and the fault memory address that is address to mra is given to must repair analyser. In must repair analyser the repairing of the faulty memory is performed. If the row address is pointing to the wrong memory location then the proper memory location pointing is done with the help of must repair analyser circuit. This helps to read or write the particular word of data to the proper memory location. This is the memory repairing with respect to the row address. Now with respect to the column address must repair analyser circuit checks for the column address whether the address is locating to the proper location or not and it lies within the specified range or not. With these signals MRA does the repairing of the memory with the help of spare memory. That is the faulty memory is replaced with the spare memory so the current operation will be performing as usual and no hazardous will happen with respect to the memory performance. In the future the implementation is done with the built in self test [4][7]. Here the memory repairing is done based on the address along with this based on the data stored in the memory location repairing is implemented in the future.

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