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Efficient Convolutional Adaptive Viterbi Encoder and Decoder Using Verilog

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Abstract: This Paper presents the design of efficient convolutional encoder and adaptive Viterbi decoder (AVD) with a constraint length, K of 3 and a code rate (k/n) of 1/2 using field programmable gate array (FPGA) technology. The adaptive viterbi decoder with convolutional encoder is a powerful forward error correction technique. This technique is particularly suited to a channel where the transmitted data is corrupted by additive white Gaussian noise. Instead of block codes, convolutional codes are used and these codes are applicable in communication. Viterbi algorithm is a maximum-likelihood algorithm for decoding of convolutional codes and these codes have good correcting capability and perform well on every noisy channel. In this paper viterbi decoder is designed for faster decoding speed and less are routing area. The proposed system is realized using verilog HDL and simulation is done by using modelsim SE 6.4c and Xilinx is used for RTL Design.

Keywords: Convolutional Encoder, Viterbi Decoder, Verilog HDL, FPGA.

I. INTRODUCTION

In today's digital communications, the reliability and efficiency of data transmission is the most concerning issue for communication channels. Error correction technique plays a very important role in communication systems. The error correction technique improves the capacity by adding redundant information for the source data transmission.Convolutional encoding is a Forward Error Correction (FEC) technique used in continuous one-way and real time communication links. Wireless devices such as hand phones and broadband modems rely heavily on forward error correction techniques for their proper functioning, thus sending and receiving information with minimal or no error.

All communication channels are subject to the additive white gaussian noise (AWGN) around the environment. Forward error correction (FEC) techniques are used in the transmitter to encode the data stream and receiver to detect and correct bits in errors, hence minimize the bit error rate (BER) to improve the performance. RS decoding algorithm complexity is relatively low and can be implemented in hardware at very high data rates. It seems to be an ideal code attributes for any application. However, RS codes perform very poorly in AWGN channel.

Most of the Viterbi decoders in the market are a parameterizable intelligent property (IP) core with an efficient algorithm for decoding of one convolutionally encoded sequence only. In addition, the cost for the Convolution Encoder and Viterbi decoder are expensive for a specified design because of the patent issue. Therefore, to realize an adaptive Convolution Encoder and Viterbi decoder on FPGA is very demanding. Complexity of Viterbi decoding algorithm increases in terms of trellis length. Increasing the trellis length causes the algorithm to take more time to decode. This will cause transmission speed lower but make the transmission more reliable. Reducing the trellis length will increase the transmission speed.

The overall block diagram of this paper is shown in the fig. 1. The message bits are generated and they are sent to the crypto system and then the decoded output is obtained. The Convolutional encoder encodes the message and then the encoded bits are generated. The bits which are encoded are again sent to the Viterbi Decoder and then the decoded output is obtained.

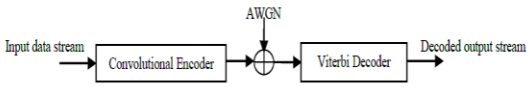

Fig 1.Block diagram

Source generates a message blocks at bits\sec,the channel with noise adds number of additional bits called check bits, which do not carry any information but helps the decoder to detects and correct the error. In digital communication errors are caused by the noise present in the communication channel, there are two types of noise channel that is Gaussian noise and

impulse noise. Also there are two types of codes which are block and convolutional codes. In digital communication errors are caused by noise present in communication.viterbi decoder is used for decoding convolutional codes and decoding algorithm is viterbi algorithm.

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II. LITERATURE SURVEY

Hema.S, Suresh Babu.V, Ramesh P [1], presented a field programmable gate array implementation of Viterbi Decoder with a constraint length of 11 and a code rate of 1/3. It shows that the larger the constraint length used in a Convolutional encoding process, the more powerful the code produced. A Viterbi algorithm based on the strongly connected trellis decoding of binary a convolutional code has been presented.

Viterbi decoders capable of achieving high decoding speed while satisfying a constraint on the structural complexity of the trellis in terms of the maximum number of states at any particular depth. Only uniform section alizations of the code trellis diagram are considered. An upper bound on the number of parallel and structurally identical (or isomorphic) sub trellises in a proper trellis for a code without exceeding the maximum state complexity of the minimal trellis of the code is first derived.

Convolutional encoding with Viterbi decoding is a good forward error correction technique suitable for channels affected by noise degradation. Fangled Viterbi decoders are variants of Viterbi decoder (VD) which decodes quicker and takes less memory with no error detection capability. Modified fangled takes it a step further by gaining one bit error correction and detection capability at the cost of doubling the computational complexity and processing time. A new efficient fangled Viterbi algorithm is proposed in this paper with less complexity and processing time along with 2 bit error correction capabilities. For 1 bit error correction for 14 bit input data, when compared with Modified fangled Viterbi decoder.

J.Tulasi, T.Venkata Lakshmi & M.Kamaraju [2], Presents designing and implementing a convolutional encoder and Viterbi decoder which are the essential block in digital communication systems using FPGA technology. Convolutional coding is a coding scheme used in communication systems including deep space communications and wireless communications. It provides an alternative approach to block codes for transmission over a noisy channel. The block codes can be applied only for the block of data. The convolutional coding has an advantage over the block codes in that it can be applied to a continuous data stream as well as to blocks of data.

Mahe Jabeen, Salma Khan [3], Presents a Convolution Encoder and Viterbi Decoder with a constraint length of 3 and code rate of 1/2. This is realized using Verilog HDL. It is simulated and synthesized using Modelsim Altera 10.0d and Xilinx 10.1 ISE. The main aim of this paper is to design FPGA based Convolution Encoder and Viterbi Decoder which encodes/decodes the data. This architecture has comparatively simpler code and flexible configuration when compared to other architectures and saves silicon area through efficient device utilization which makes it favorable for FPGA's.

Convolution coding is a popular error-correcting coding method used in digital communications. A message is convoluted, and then transmitted into a noisy channel. This convolution operation encodes some redundant information into the transmitted signal, thereby improving the data capacity of the channel. The Viterbi algorithm is a popular method used to decode convolutionally coded messages. The algorithm tracks down the most likely state sequences the encoder went through in encoding the message, and uses this information to determine the original message. Instead of estimating a message based on each individual sample in the signal, the convolution encoding and Viterbi decoding process packages and encodes a message as a sequence, providing a level of correlation between each sample in the signal. As the convolution codes are used mostly for the channel encoding of data to achieve low-error-rate in latest wireless communication standards like 3GPP, GSM and WLAN; the use of optimal decoding Viterbi algorithm will suffice. All communication channels are subject to the additive white Gaussian noise (AWGN) around the environment. The block codes can be applied only for the block of data whereas convolution coding has can be applied to a continuous data stream as well as to blocks of data. Convolution Encoding with Viterbi decoding is a powerful FEC technique that is particularly suited to a channel in which the transmitted signal is corrupted mainly by AWGN. It operates on data stream and has memory that uses previous bits to encode.

K. S. Arunlal1 and Dr. S. A. Hariprasad [4], Convolutional encoding with Viterbi decoding is a good forward error correction technique suitable for channels affected by noise degradation. Fangled Viterbi decoders are variants of Viterbi decoder (VD) which decodes quicker and takes less memory with no error detection capability. Modified fangled takes it a step further by gaining one bit error correction and detection capability at the cost of doubling the computational complexity and processing time. A new efficient fangled Viterbi algorithm is proposed in this paper with less complexity and processing time along with 2 bit error correction capabilities. For 1 bit error correction for 14 bit input data, when compared with Modified fangled Viterbi decoder, computational complexity has come down by 36-43% and processing delay was halved. For a 2 bit error correction, when compared with Modified fangled decoder computational complexity decreased by 22- 36%.Viterbi decoder is an important block in any CDMA modem. CDMA systems being interference based use forward error correction schemes like convolutional encoding to increase cell capacity. The Viterbi Algorithm may be viewed as a solution to the problem of maximum a posteriori probability estimation of the state sequence of a finite-state discrete-time Markov process observed in memory less noise. Viterbi decoder is one of the most important blocks in a CDMA modem. In this paper we have designed and implemented the Viterbi decoder targeting a FPGA implementation. Our aim was to develop

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an area efficient 19.2kbps, 256 states Viterbi decoder, but the design can cater to higher input data rates.

Rupali Dhobale,Kalyani Ghate, Nikhil Pimpalgaonkar ,R. B. Khule [5], Viterbi algorithm is employed in wireless communication to decode the Convolution codes; those codes are used in every robust digital communication systems. Such decoders are complex & dissipate large amount of power. Thus the paper presents the design of an Adaptive Viterbi Decoder (AVD) that uses survivor path with parameters for wireless communication in an attempt to reduce the power and cost and at the same time increase in speed. Most of the researches work to reduce power consumption, or work with high frequency for using the decoder in the modern applications such as 3 GPP, DVB, and wireless communications. Field Programmable Gate Array technology (FPGA) is considered a highly configurable option for implementing many sophisticated signal processing tasks.

III. CONVOLUTIONAL ENCODER

Convolutional codes are block of n code digits depends on previous as well present state values. Convolution encoder with viterbi decoder is a powerful method for forward error correction technique. The principle of viterbi algorithm is maximum likelihood decoding. Basic block diagram for convolution encoder followed by viterbi decoder with addition of Additive White Gaussian Noise (AWGN) is shown in the Figure1. Input data stream is fed to the convolution encoder, which produces encoded output stream according to designed encoder specification. The encoded data steam travels through channel having presence of noise, produces the new encoded stream with noise. Finally, this noisy data is given to the viterbi decoder that produces the corrected data which is applied to the encoder as input. A convolutional encoder is a Mealy machine, where the output is a function of the current state and the current input. It consists of one or more shift registers (DFF) and multiple XOR gates. XOR gates are connected to some stage of the shift registers as well as to the current input to generate the output polynomials.

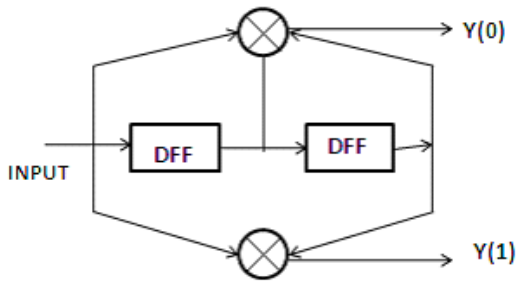

Fig 2. Convolutional encoder

The block diagram of convolution encoder is shown in Fig 2. To generate the output, the encoder uses three values of the input signal, one present and two past. The set of past values of input data is called a state. The number of input data values used to generate the code is called the constraint length. Each set of outputs is generated by EX-OR ing a pattern of current and shifted values of input data. The pattern used to generate the coded output value can be expressed as binary strings called "Generator Polynomials" (GP). The MSB of the GP corresponds to the input; the LSBs of the GP correspond to the state. The encoder that has been designed is a linear, non – systematic, convolution encoder.

IV. VITERBI DECODER

Viterbi decoding was developed by Andrew J. Viterbi, is an Italian-American electrical engineer and businessman who co-founded Qualcomm Inc. His seminar paper titled "Error Bounds for Convolutional Codes and an Asymptotically Optimum Decoding Algorithm", published in IEEE Transactions on Information Theory, in April, 1967. Since then, other researchers have expanded on his work by finding good convolutional codes, exploring the performance limits of the technique, and varying decoder design parameters to optimize the implementation of the technique in hardware and software. Design and Implementation of Viterbi Decoder with FPGAs by M. Kivoja and et.al [6] have analyzed suitability of FPGA device architectures for implementing complex algorithms.

The Viterbi algorithm works by forming trellis structure, which is eventually traced back for decoding the received information. It reduces the computational complexity by using simpler trellis structure. The Viterbi Decoder is used in many FEC applications and in systems where data are transmitted and subject to errors before reception. Viterbi decoders also have the property of compressing the number of bits of the data input to half. As a result redundancy in the codes is also reduced. Hence Viterbi decoding is more effective and efficient. The Viterbi decoder designed here is 8:4 decoder. The same logic and concept can also be extended to further number of bits also. Viterbi decoders are based on the basic algorithm which comprises of minimum path and minimum distance calculation and retracing the path.

The Viterbi algorithm is commonly used in a wide range of communications and data storage applications. It is used for decoding convolutional codes, in baseband detection for wireless systems, and also for detection of recorded data in magnetic disk drives. The requirements for the Viterbi decoder or Viterbi detector, which is a processor that implements the Viterbi algorithm, depend on the applications where they are used. This results in very wide range of required data throughputs and power or area requirements. Viterbi detectors are used in cellular telephones with low data rates, of the order below 1Mb/s but with very low energy dissipation requirement. They are used for trellis code demodulation in telephone line modems, where the throughput is in the range of tens of

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kb/s, with restrictive limits in power dissipation and the area/cost of the chip. On the opposite end, very high speed Viterbi detectors are used in magnetic disk drive read channels, with throughputs over 600Mb/s. But at these high speeds, area and power are still limited. Error correction is an integral part of any communication system and for this purpose, the convolution codes are widely used as forward error correction codes. The two decoding algorithms used for decoding the Convolutional codes are Viterbi algorithm and Sequential algorithm.

A Viterbi algorithm consists of the three major parts Branch metric unit, Path metric unit and trace back as shown in Fig. 3.

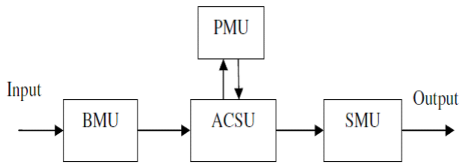

Fig 3. Block diagram of Viterbi decoder

Viterbi decoders also have the property of compressing the number of bits of the data input to half. As a result redundancy in the codes is also reduced. Hence Viterbi decoding is more effective and efficient. The Viterbi decoder designed here is 8:4 decoder. The same logic and concept can also be extended to further number of bits also. Viterbi decoders are based on the basic algorithm which comprises of minimum path and minimum distance calculation and retracing the path.

Sequential decoding has advantage that it can perform very well with long constraint length Convolutional codes, but it has a variable decoding time. Viterbi decoding is the best technique for decoding the Convolutional codes but it is limited to smaller constraint lengths (K<10) [5]. It has fixed decoding time compared to sequential decoding. With the Viterbi algorithm, storage and computational complexity are proportional to 2K. To achieve very low error probabilities, longer constraint lengths are required, and sequential decoding becomes attractive. The performance of a decoder is characterized by the number of decoded output bits which are in error, the Bit Error Rate or BER. The Viterbi algorithm [13], the most popular decoding approach for convolutional codes, determines a minimum distance path with regards to Hamming distances applied to each received symbol. A limiting factor in Viterbi decoder implementations is the need to preserve candidate paths at all $2K-1$ trellis states for each received symbol. This requirement leads to an exponential growth in the amount of computation performed and in the amount of path storage retained as constraint length K grows.

The basic units of viterbi decoder are branch metrics, Add compare select and Survivor management unit. Figure 1 shows the general structure of a Viterbi decoder. It consist of three blocks: the branch metric unit (BMU), which computes metrics, the add–compare–select unit (ACSU), which selects the survivor paths for each trellis state, also finds the minimum path metric of the survivor paths and the survivor management unit (SMU), that is responsible for selecting the output based on the minimum path metric.

1) Branch metric calculation

The first unit is called Branch metric unit. The Hamming distance (or other metric) values we compute at each time instant for the paths between the states at the previous time instant and the states at the current time instant are called branch metrics. Hamming distance or Euclidean distance is used for branch metric computation.

2) Path metric calculation

An accumulated Error metric called path metric (PM) contains the 2K-1 optimal paths. The current Branch Metric is added to previous PM and each the two distances are compared for all Add- compare select unit In terms of speed the performance of Viterbi Decoder is mainly determined by the number of ACS (2K-1) units and their computation time. As shown in figure each ACS unit comprises two adder blocks, a comparator and a selector block.

3) Trace back unit

The final unit is trace back unit where the survivor path and output data are identified. The Viterbi decoding flowchart is given in Fig.4.

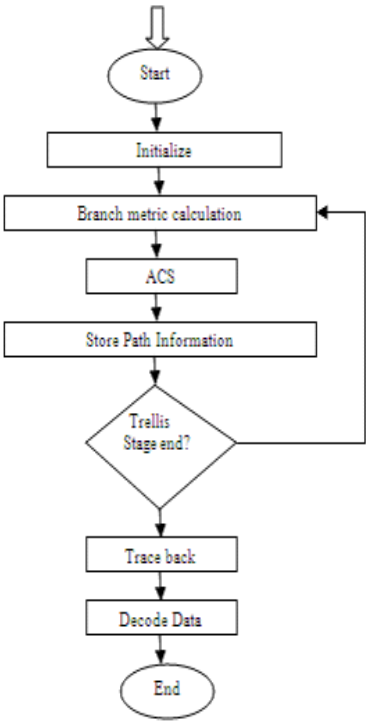

Fig 4: Viterbi decoding Flow Chart

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V. CONCLUSION

Viterbi decoder is one of the most important blocks in communication system. Viterbi algorithm allows safe data transmission via error correction and original message can recover accurately without any noise. Viterbi decoding is used for deep space communication, against impulsive noise with application to speech recognition, satellite communication and in many applications. Viterbi decoder and adaptive Viterbi decoder units will give simple elements in each unit and new algorithms. The survivor path algorithm used the address of the memory unit to select the correct path which specifies the output code.

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