ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING

National Conference on Advanced Innovation in Engineering and Technology (NCAIET-2015)

Alva's Institute of Engineering and Technology, Moodbidri

Vol. 3,Special Issue 1,April 2015

Hardware Implementation of Retinal Image Processing Algorithm on FPGA

Nazia Abdul Majeed[1], Satheesh Rao[2]

P.G Student, Department of E.C.E., N.M.A.M. Institute of Technology, Nitte, India[1]

Assistant Professor, Department of E.C.E. N.M.A.M. Institute of Technology, Nitte, India[2]

Abstract: A methodology for implementing real-time DSP applications on a field programmable gate arrays (FPGA) using Xilinx System Generator (XSG) is presented. This paper outlines efficient hardware architecture for detection of exudates in retinal images. The proposed design comprises architecture for Sobel edge detection and segmentation method. The egde map image obtained is enhanced for its perception using contrast stretching. Further the image is segmented to detect the exudates. This design has been implemented on Virtex-II Pro (xc2vp30-7ff896 platform). The code is synthesized within ISE 9.2 development suite. The results obtained via hardware software co-simulation use limited FPGA resources at higher maximum frequency.

Keywords: XSG, FPGA, Edge detection, Segmentation, Exudates

I. INTRODUCTION

Diabetic retinopathy is a disease commonly found in diabetic patients, which is a major cause of blindness and vision defects. It causes damage to the retinal vessels thus the protein and fat gets leaked out from the abnormal blood vessels, resulting in yellowish intraregional deposits termed as Exudates. Vision loss can occur if the exudates extend into the macular area [1]. Therefore it is essential to detect these exudates. But the detection of the exudates in early stage is difficult only by visual inspection. Therefore there is lot of ongoing research to detect this disease in an early stage by using different algorithms. Various edge detection based techniques are employed by researchers to detect blood vessels and exudates.

Edge detection is a fundamental tool in image processing, useful in the areas of feature detection and feature extraction. Edge detection highlights on sharp or gradual discontinuity in the pixel intensity. Thus amount of data to be processed is significantly reduced and irrelevant information is being filtered out. There are several types of operators available for edge detection based on first and second order derivatives. In First order derivative input image is convolved by an adapted mask to generate a gradient image. The major classical operators like Prewitt, Sobel, and Robert are the first order derivative operators also called gradient operators which spot edges by looking for maximum and minimum intensity values. Second order derivative include Laplace operator, which is often applied after smoothening the image to reduce noise.

FPGAs provide a better platform for real-time algorithms on application-specific hardware with substantially greater performance than programmable DSPs. The need to process the image in real time leads this implementation in hardware level, which offers parallelism and thus significantly reduces the processing time. FPGAs are increasingly used in medical imaging but the drawback is that high level language is used for coding. Xilinx System Generator is a DSP design tool from Xilinx that enables the use of the MathWorks model-based Simulink design environment which makes it very easy to handle with respect to other software for FPGA design. This objective leads to the use of Xilinx System Generator (XSG). It focuses in the processing pixel to pixel of an image and in the modification of pixel neighbourhoods owing to the transformation of the whole or partial image. The proposed hardware implementation method is architecturally based on the Xilinx system generator tool integrated with ISE 9.2 development suite and MATLAB 2007a. The design focuses on achieving overall high performance, short development time and low cost.

II. RELATED WORK

An extensive work is carried out in the field of feature extraction for real time image processing. Edge detection being fundamental step for any image processing operation, it provokes great concern in research fraternity. Pawar presented hardware implementation of canny edge detection algorithm [2] using XSG on Virtex-5 ML506 platform and developed VGA interfacing for displaying images on screen. Z. Shanshan and W. Xiaohong, proposed simplified hardware approach for vehicle edge detection in traffic analysis [3] using XSG. Yahia et al., presented design to estimate real time sobel edge detection for video processing [4]. The design utilized black blocks in Simulink to integrate the VHDL code for co-simulation. Architecture for Prewitt edge detection algorithm [5] is developed by Pham using system generator on Xilinx Spartan 6LX platform. The FPGA implementation of point processing algorithms [6] are described by Elamaran et al., which can be extended to both spatial and frequency domain applications. An efficient MRI image filtering and Tumour Characterization algorithm [7] is implemented on FPGA using XSG by Christe et al.

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING

National Conference on Advanced Innovation in Engineering and Technology (NCAIET-2015)

Alva's Institute of Engineering and Technology, Moodbidri

Vol. 3,Special Issue 1,April 2015

The remainder of the paper is organized as follows. Section 2 briefly presents the related work. Section 3 describes the features of XSG. Section 4 describes the architecture of the proposed system. Section 5 presents the architecture of hardware co-simulation and results. Section 6 draws the conclusion.

III. XILINX SYSTEM GENERATOR

The proposed architecture is developed by the integrated design tool XSG dedicated FPGA. XSG provides an interface based on the extensive set of xilinx optimized DSP building blocks. It includes slightly higher abstraction level. It uses the Mathworks Simulink with a list of specific Xilinx blockset, which can be used to create designs optimized for Xilinx FPGA's [8]. Some blocks such as the Black box and M-code allow for direct programming in Verilog, VHDL, MATLAB M-code and C code to simplify the integration with an existing design. Additionally it provides the usage of Matlab workspace during simulation. The Xilinx System Generator itself has the feature of generating User constraints file (UCF), Test bench and Test vectors for testing architecture.The integrated design flow of XSG allows simulink design to create the Bit Stream (*.bit) file and generate automatic VHDL or verilog code from Simulink and MATLAB. The bit file can then be downloaded on to the FPGA board.

Unlike software processing, XSG manipulates images as one-dimensional vectors in place of 2-d matrix. By this conversion, the (x, y) pixel in the (m, n) original image will have the [(y-1)*n + x] position in the output vector. Thus, the image is stored in an input ROM to be ready to handle. The image conversion is as shown in Fig. 1.

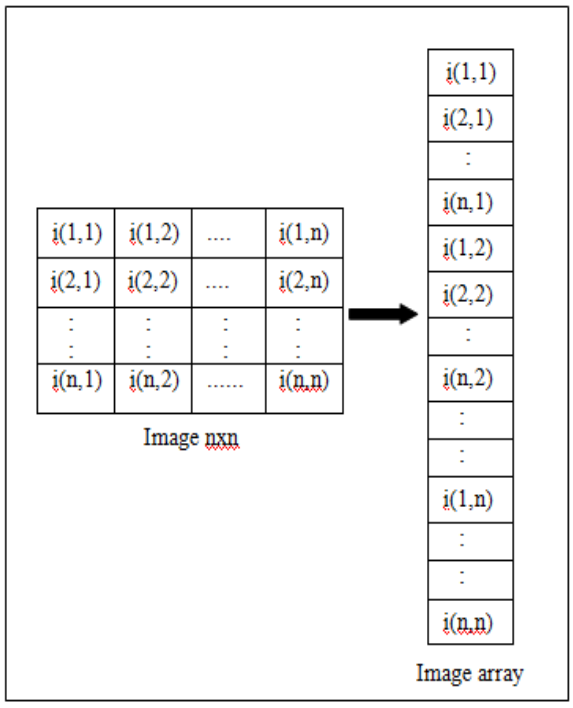

Fig. 1 Image Conversion

IV. THE PROPOSED SYSTEM

The architecture of the exudate detection using XSG is as shown in Fig. 2. The design flow describes about the basic idea of the proposed hardware implementation on FPGA platform. The powerful tools utilized for the design implementation are System Generator 9.2i, MATLAB 2007a, Xilinx ISE 9.2 and Virtex II-pro Development board for hardware-software co design.

The process of Xilinx System Generator in five stages:
1. Transform the 2D input image to 1D.
2. Design the proposed model in Simulink using XSG
3. Perform the co-simulation.
4. Generate and Synthesis HDL code.
5. Hardware/software co-simulation

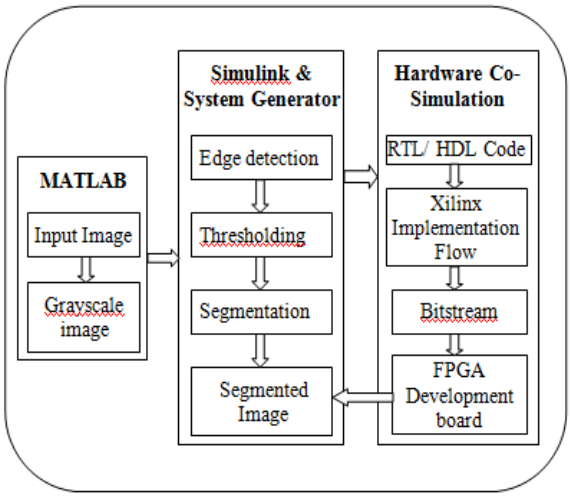

Fig. 2 Design Flow of the proposed model

Input Image Pre-processing: The images are converted from RGB to grayscale, resized and transformed to 1-dimensional vectors using MATLAB code. The pixels are serialized and temporarily stored in the workspace so as to make it in a format suitable for the hardware execution. Thus further processing of data is achieved by using 'From Workspace' block available in Simulink.

1) Sobel Edge Detection: Sobel is a gradient based edge detection filter. This operator has relatively small masks. Unlike laplace operator, Sobel operator is insensitive to noise. For edge detection, original image is convolved with coefficient of convolution kernel obtained along **x** and **y** direction. For a given image I, horizontal and vertical gradient of each pixel (x, y), are computed as shown in (1) and (2) where G_x and G_y represent horizontal and vertical gradients.

$$G_x(x,y) = \begin{bmatrix} +1 & 0 & -1 \\ +2 & 0 & -2 \\ +1 & 0 & -1 \end{bmatrix} * I(x,y) \quad (1)$$

$$G_y(x,y) = \begin{bmatrix} +1 & +2 & +1 \\ 0 & 0 & 0 \\ -1 & -2 & -1 \end{bmatrix} * I(x,y) \quad (2)$$

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING

National Conference on Advanced Innovation in Engineering and Technology (NCAIET-2015)

Alva's Institute of Engineering and Technology, Moodbidri

Vol. 3,Special Issue 1,April 2015

XSG provides a simple solution for edge detection on images. The 2-D convolution operation, in (1) and (2), can be functionally implemented as an n-tap MAC FIR filter with nine programmable coefficient sets. Further high abstracted implementation can be achieved using a 5x5 filter image block.

The architecture of the proposed model is as shown in Fig.3 consists of three stages: Edge detection, contrast stretching and segmentation. In the first stage, the retinal pixels are sequentially streamed into virtex2 5 line buffers via a gateway in block to construct 5 lines of output. Each line is delayed by N samples where N is the length of the line. Line 1 is delayed by 4*N samples, each of the following lines are delayed by N fewer samples, and line 5 is a copy of the input.

This follows 5x5 filter which consists of parallel five n-tap MAC FIR filters and four adder blocks structure, to filter the 256x256 grayscale retinal image. 5x5 filter block provides nine different 2-D FIR filters and offers compile time parameter. The nine filters are Edge, Smooth, Sharpen, SobelX, SobelY, SobelXY, Blur, Gaussian and Identity. The 2-D filters types can be selected by varying the mask parameter on the 5x5 Filter block. SobelXY filter is selected for Sobel edge detetion which performs convolution operation with input pixel values in the horizontal and vertical direction. The filter coefficients are stored in a block RAM .Hence, these coefficients can be modified by changing the mask of the 5x5 FIR filter. The architecture needs 5 clock cycles to process per pixel. The MAC processes the pixels at one pixel per clock cycle, since they are clocked five times faster than the input rate. They have to be down-sampled by 5 to match the output rate. Here the Simulink system period is set to 1/5s.

The Xilinx Register block in the model is a D flip-flop-based register, having latency of one sample period.

2) Contrast Stretching: In the second stage the edge map image thus obtained is enhanced for its perception using contrast stretching algorithm. The contrast of an image is its distribution of light and dark pixels. It is a point process which involves application (addition, subtraction, division or multiplication) of an identical constant value to every pixel in the image. Contrast stretching in XSG is achieved by using Addsub, Constant, and CMult blocks

3) Image Segmentation: Segmentation is a significant method in many imaging applications. The third stage depicts Image segmentation using threshold, essentially employed to locate the exudates. Segmentation on a simple pixel-by-pixel basis using threshold decisions can be achieved using Mcode block.

Constant block used in the model, sets the threshold level. The results thus obtained are reconverted to two dimensional matrix using MATLAB Workspace in order to represent it as an image. Finally, the exudates seen as yellow patches on the retina are segmented.

The Xilinx Resource Estimator block estimates the FPGA resources required to implement XSG model or subsystem. Additionally Xilinx System Generator token is utilized for FPGA compatibility. Using both Simulink and Xilinx blocks in the model helps for XSG simulation, HDL code generation, and synthesis. The proposed model is simulated in Simulink environment with suitable simulation time and simulation mode. The resultant segmented image is observed. Once the expected results are obtained System Generator is configured for suitable FPGA board.

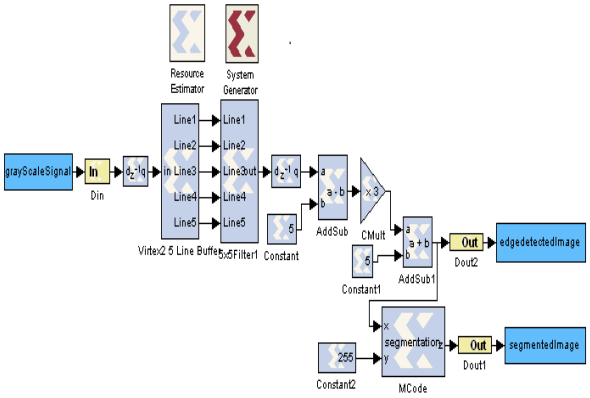

Fig. 3 Architecture of Proposed Model

V. HARDWARE CO-SIMULATION AND RESULTS

Hardware board is installed using System Generator Board Description Builder to implement the design in Virtex-II Pro development Platform. The clock is set to frequency of 100 MHz. Clocking mode is set to single step clock, which keeps the hardware in the lock step with the software simulation.

The automatic code is invoked by pressing Generate button in system generator block dialog box. The code generator produces a FPGA configuration bitstream for the design that is suitable for hardware co-simulation and also comprises of additional interfacing logic that allows Sysgen to communicate with the design using a physical interface between the FPGA platform and the PC. Completion of compiling design creates a new JTAG co-simulation block as shown in Fig.4.

This JTAG Co-simulation block contains all Xilinx blocks within the Gateway blocks of the original system. Gateway In and Gateway Out blocks define the FPGA boundary. During simulation, a hardware co-simulation block interacts with the underlying FPGA platform, automating tasks such as device configuration, data transfers

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING

National Conference on Advanced Innovation in Engineering and Technology (NCAIET-2015)

Alva's Institute of Engineering and Technology, Moodbidri

Vol. 3,Special Issue 1,April 2015

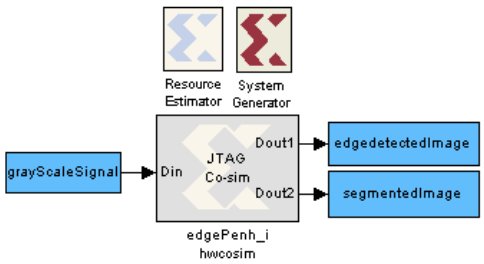

Fig. 4 Architecture for Hardware Co-simulation

and clocking. Co-simulation process displays the output signal produced by the FPGA hardware. The data received from the FPGA is then acquired by the MATLAB Workspace. The Fig.5 and Fig.6 shows the Edge detection and Segmentation results obtained using an efficient algorithm for 2 different retinal images. Edge detected Image highlights the optic disc, blood vessels and exudates of the input image. Further, Segmented Image locate only the exudates from the edge detected image and thus identifying the abnormalities present in retina.

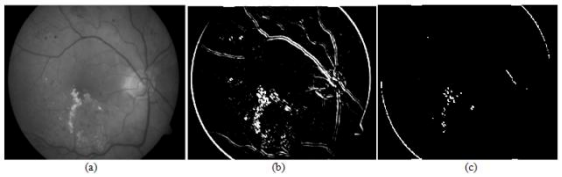

Fig.5 (a) Input Image (b) Edge Detected Image (c) Segmented Image

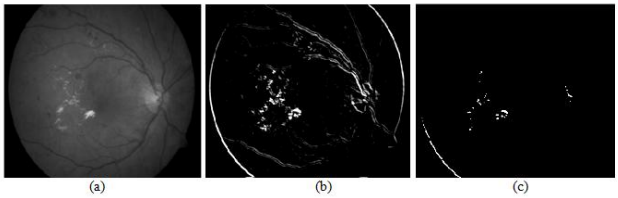

Fig.6 (a) Input Image (b) Edge Detected Image (c) Segmented Image

The generated HDL files are synthesized using Xilinx. The synthesis of the code will give the information about the errors, warnings, RTL schematic of that code, device utilization summary etc. The Top-level RTL schematic of the proposed architecture is as shown in Fig. 6.

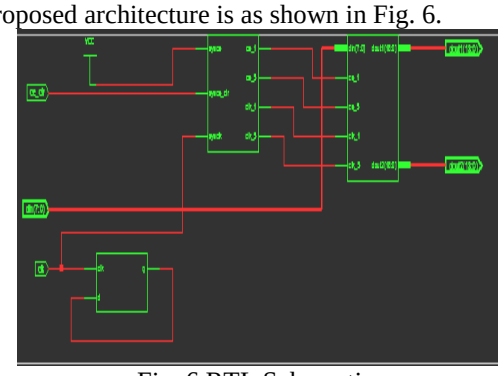

Fig. 6 RTL Schematic

Device utilization summary depicts the information pertaining to device utilization analysis. Detailed reports provide access to reports that are generated as the design is processed. Table 1 indicates the device utilization summary after the design is mapped to a Xilinx Virtex-II Pro xc2vp20 FPGA..Slice registers available are 13696, out of which 350 are used for implementation which is equal to 2% of available resources. Number of slice Flip-flops used is 2% which gives 579 usages out of 27392. Usage of 4 input LUTs are 390 out of 27392 which is equal to 1%.

TABLE 1: DEVICE UTILIZATION SUMMARY

Logic Utilization	Used	Available	Utilization
Number of Slices	350	13696	2%
Number of Slice Flip Flops	579	27392	2%
Number of 4 input LUTs	390	27392	1%
Number of bonded IOBs	47	556	8%
Number of BRAMs	9	136	6%
Number of MULT18X18s	6	136	4%
Number of GCLKs	1	16	6%

Utilization of Bonded IOBs is 47 out of 556 which 8% of available IOBs. Numbers of BRAMs used are 9 out of 136 which is 6% of available. Number of multipliers used is 4% which gives 6 usages out of 136 and 1 GCLK is used out of 16 available resources. These summaries tell that the use of the device or hardware for system is very less at low power consumption of 210.23mW and higher maximum frequency of 323.23 MHz.

VI. CONCLUSION

Xilinx system generator has a unique FPGA in the loop co-simulation feature, which greatly simplifies the complicated programming and allows the designers to accelerate simulation while simultaneously testing the design in hardware. The aim of this paper is to prove the role of System Generator in designing a hardware system for the recognition of Retinal exudates and thus identify the abnormalities present in retina. The hardware architecture of edge detection and segmentation is successfully implemented in the device Virtex-II Pro (xc2vp30-7ff896 platform). The results obtained via hardware software co-simulation use limited FPGA resources at higher maximum frequency and low power consumption.

REFERENCES

[1]. Singer DE, Nathan DM, Fogel HA, Schachat AP. Screening for diabetic retinopathy. Ann Intern Med 1992; 116(8):660–71.

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING

National Conference on Advanced Innovation in Engineering and Technology (NCAIET-2015)

Alva's Institute of Engineering and Technology, Moodbidri

Vol. 3,Special Issue 1,April 2015

[2]. P.H. Pawar and R.P. Patil, "FPGA implementation of Canny edge detection algorithm," International Journal of Engineering and Computer Science, vol. 3, pp. 8704–8709, 2014.
[3]. Z. Shanshan and W. Xiaohong, "Vehicle Image Edge Detection Algorithm Hardware Implementation on FPGA," in Proc. ICCASM, Vol.14, p.184-188, 2010.
[4]. Yahia Said, Taoufik Saidani, Fethi Smach and Mohamed Atri, "Real Time Hardware Co-simulation of Edge Detection for Video Processing Time", in Proc. of Electrotechnical Conference (MELECON),Vol.25, p.852-855, 2012.
[5]. P. Nguyen, J. Cho, and S. B. Cho, "An architecture of real time hardware co-simulation of edge detection in image processing using prewitt edge operator," in Proc. ICEIC'00, paper 11.3.4, p.1-2, 2014.
[6]. V. Elamaran and G. Rajkumar, "FPGA implementation of point processes using Xilinx system generator", Journal of Theoretical and Applied Information Technology, Vol. 41, pp.201-206, 2012.
[7]. S.A. Christe, M. Vignesh and A. Kandaswamy, "An efficient FPGA implementation of MRI image filtering and tumour Characterization using Xilinx system generator" International Journal of VLSI design and Communication Systems, Vol. 2 No. 4, pp.95-109, 2011.
[8]. System Generator for DSP user guides, (2010) [Online]. Available: http://www.xilinx.com/support/sw_manuals/sysgen_bklist.pdf
[9]. Xilinx, Inc., XUP Virtex-II Pro Development System Hardware Reference Manual, 2005.