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Design and Analysis of an Efficient Counter Using Pulse Enhancement Flip-Flop

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Abstract: In this paper, a high performance pulse Triggered flip- flop design is presented. The proposed design reduces the number of transistors stacked in the discharging path and also reduces the overall switching delay. This enhanced pulse triggered low-power flip flop (EPTLFF) avoids unnecessary internal node transitions to improve the power consumption as compared to previously designed circuits. A 4-bit counter is also designed using proposed EPTL. This design features the reduced power consumption and power-delay-product performance as compared to the other two types of flip flops which are implemented. These designs are simulated using mentor graphics schematic editor tool.

Keywords: Flip-flop, low power, pulse-triggered.

I. INTRODUCTION

Flip-Flops (FFs) or latch is the basic storage elements used extensively in all kinds of digital designs. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. One latch or Flip-Flop can be store one bit information. Some of these flip-flops are quite good at being low power and high performance. Pulse triggered flip flop (PFF) is considered as a popular alternative to the conventional master slave based FF in the application of high speed operations. Conventional master slave flip-flops have two separate clocks for the master and slave and hence consume more power. A delay is introduced between the input and the output which provides the expected results but comparatively slower. Edge-Triggered flip-flops consume more power. Performance of the system is a major concern and the need for high speed circuits have increased. High speed in the sense it needs high clock frequency for its operation which in turn consumes more power [1].

Traditional master-slave flip-flops are characterized by their hard-edge property. Alternatively, pulse-triggered flip-flops reduce the two stages into one stage and are characterized by the soft edge property. The logic complexity and number of stages inside these pulse-triggered flip-flops are reduced, leading to small D-to- Q delays. Pulse triggered flip-flops can be used for low power operation. The term pulse-triggered means that data are entered into the flip-flop on the rising edge of the clock pulse, but the output does not reflect the input state until the falling edge of the clock pulse. Pulse triggered flip-flops are sensitive to any change of the input levels during the clock pulse is still HIGH, the inputs must be set up prior to the clock pulse's rising edge and must not be changed before the falling edge. There is a need of only one latch, so circuit complexity is reduced. Pulse triggered flip-flops are less sensitive to clock skew and jitter. They reduce the two stages in the master slave flip-flop into one stage and are characterized by the soft edge property. The logic complexity and number of stages inside these pulse-triggered flip-flops are reduced, leading to small D -to- Q delays. One of the main advantages of pulse-triggered flip-flop is that they allow time borrowing across cycle boundaries as a result of the zero or even negative setup time. Due to these timing issues, pulse- triggered flip-flops provide higher performance than their master-slave counterparts. It needs pulse generation logic for generating the control pulse. In this paper an Enhanced Pulse Triggered Flip Flop (EPTLFF) is proposed that has reduced the number of transistors and avoids unnecessary internal node transitions, as well as low power consumption and smaller delay compared to conventional P-FF and using this flip flop an efficient counter is designed and compared with conventional designs [4].

II. CONVENTIONAL FLIP FLOP DESIGNS

Some of the conventional flip flop circuits used in later performance comparison are shown below.

A. Single- Ended Conditional Capture Energy Recovery flip flop(SCCER)

A refined low power P-FF design SCCER using conditional discharged technique is shown in Fig. 1. In this design, a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node X. The discharge path contains NMOS transistors N2 and N1 connected in series.

In order to eliminate superfluous switching at node X, an extra NMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high. The worst case timing of this design occurs when input data is "1" and node X is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull up transistor P1. A powerful pull-down circuitry is thus needed to ensure node X can be properly discharged [2].

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B. Enhanced Pulse Triggered Flip Flop (EPTLFF)

The Enhanced Pulse Triggered Low-power Flip Flop (EPTLFF), for high-speed operation of data storage and a popular alternative to Master slave flip-flop is shown in Fig. 2. The enhanced pulse triggered low-power flip flop (EPTLFF) with pulse control scheme consists of pulse generator for generating Strobe signals and a latch for data storage. The upper part latch design and lower part enhanced pulse generation. This particular clock pulse is used to a two-input pass transistor logic, N2, N3 a two input pass transistor logic based AND gate to control the discharge of transistor N1. Author design reduced the discharging path X, avoids unnecessary internal node transitions to reduce power consumption and delay [2].

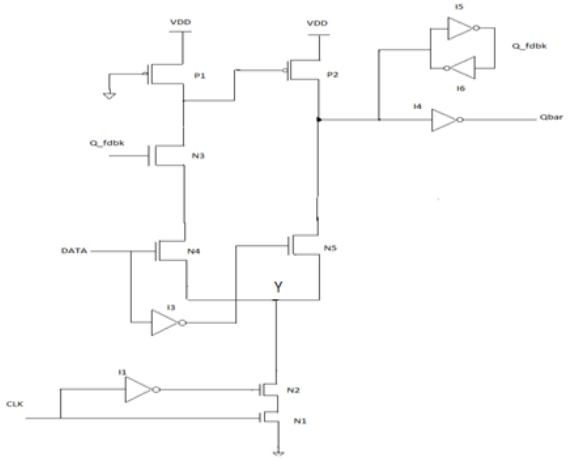

Fig. 1. Conventional pulse-triggered FF design. SCCER

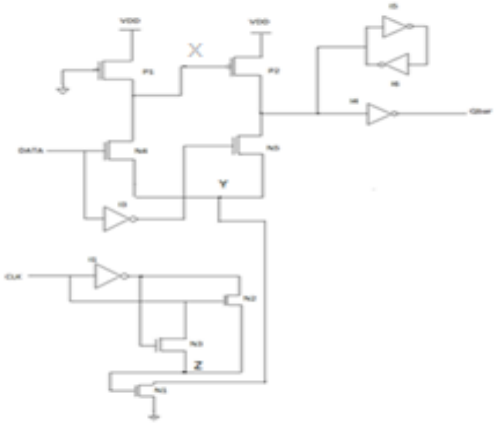

Fig. 2. Conventional pulse-triggered FF design. EPTL

III. PROPOSED ENHANCED PULSE TRIGGERED FLIP FLOP (EPTLFF)

The proposed design Enhanced Pulse Triggered Flip Flop (EPTFF), for high speed operation of data storage and popular alternative to Master Slave flip-flop is shown in Fig. 3. The enhanced pulse triggered low-power flip flop (EPTLFF) with pulse control scheme consists of pulse generator for generating Strobe signals and a latch for data storage. It reduces the number of transistors stacked in the discharging path and also reduces the overall switching delay.

Refer to Fig. 2, the upper part latch design and lower part enhanced pulse generation. This particular clock pulse is used to input pass transistor logic, N2 input pass transistor logic to control the discharge of transistor N1. The output node Z is kept at zero most of the time. At the rising edges of the clock, transistors N2 is turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1 by a time span defined by the delay inverter I1. The switching power at node Z can be reduced due to a diminished voltage swing. Where the discharge control signal is driven by a single transistor, conduction of one NMOS transistors (N2) speeds up the operations of pulse generation. In this design reduced the discharging path X, avoids unnecessary internal node transitions to reduce power consumption and power delay product [1].

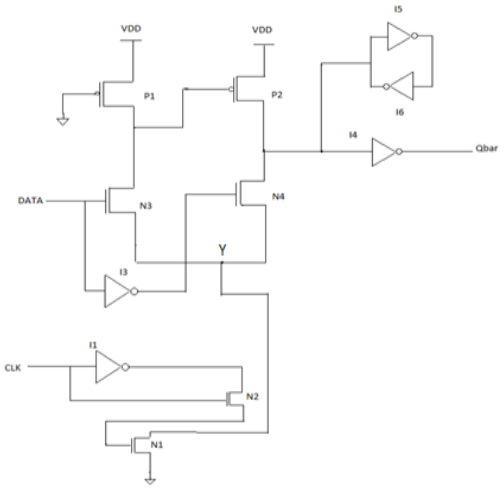

Fig. 3. Proposed Enhanced Pulse Triggered Flip Flop

IV. SYNCHRONOUS COUNTERS

Flip-flops are the basic storage elements and can be used to design registers, counters and memory elements. By designing a synchronous counter using such designs, we can prove that the counter designed with pulse enhancement scheme provides low power consumption in the counters [4].

A 4-bit synchronous counter designed using these flip flops is shown in Fig. 4.

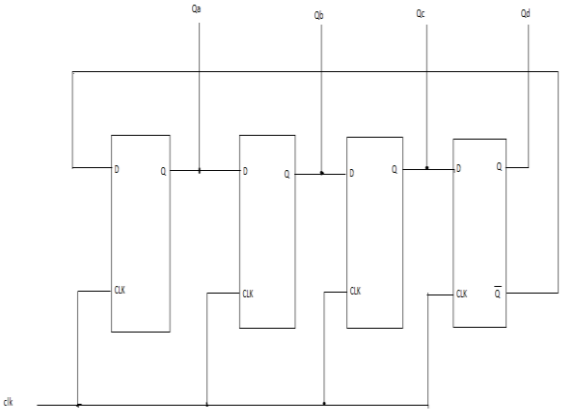

Fig 4. 4-bit synchronous counter

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V. RESULT AND ANALYSIS

The design is simulated using mentor graphics schematic editor tool. The simulation waveform obtained for various flip flop circuit is shown below. Schematic diagram of proposed flip flop and the simulation result which is obtained by simulating this design in mentor graphics schematic editor tool is shown in Fig. 5 and Fig. 6 respectively and is same as expected.

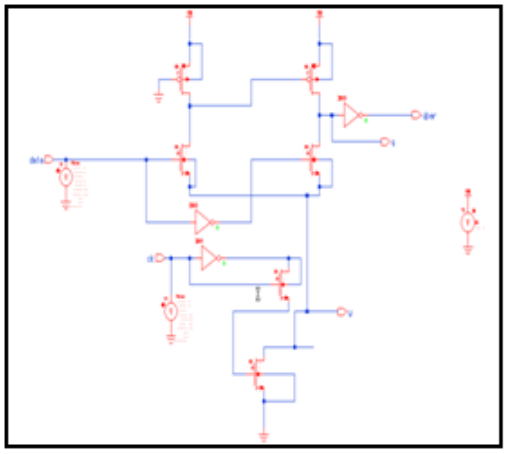

Fig. 5. Schematic of Proposed Enhanced Pulse Triggered Flip Flop

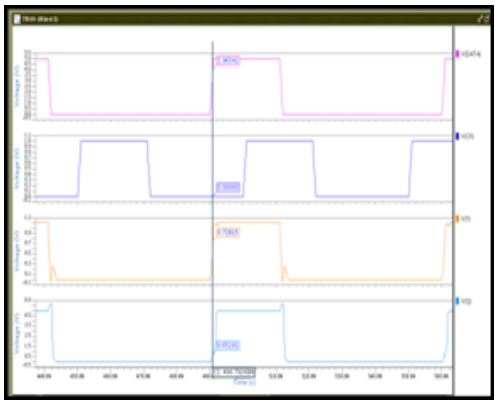

Fig. 6. Simulation Result for Proposed Pulse Triggered Flip Flop

The schematic diagram of conventional flip flop and the simulation result which is obtained by simulating this design in mentor graphics schematic editor tool is shown in Fig. 7 and Fig. 8 respectively and is same as expected.

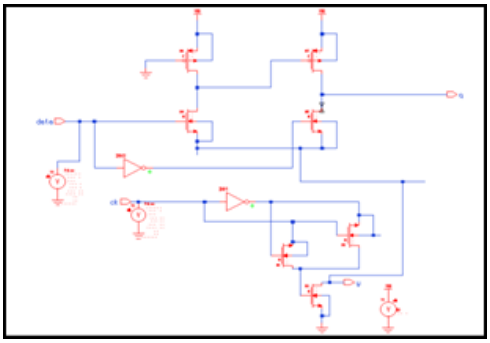

Fig. 7. Schematic of Conventional Enhanced Pulse Triggered Flip Flop

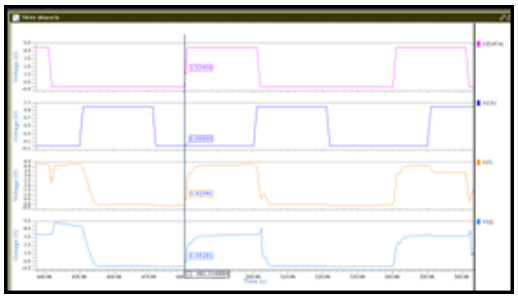

Fig. 8. Simulation Result for Conventional Pulse Triggered Flip Flop

The schematic diagram of Single Ended Conditional Capture Energy Recovery flip flop and the simulation result which is obtained by simulating this design in mentor graphics schematic editor tool is shown in Fig. 9 and Fig. 10 respectively and is same as expected.

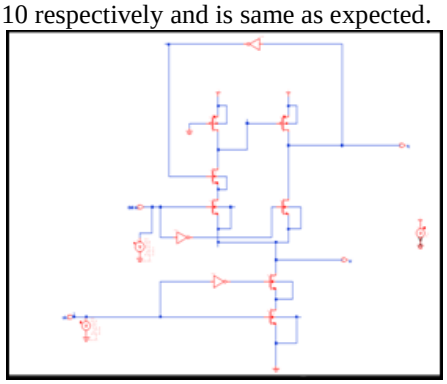

Fig. 9. Schematic of Single Ended Conditional Capture Energy Recovery

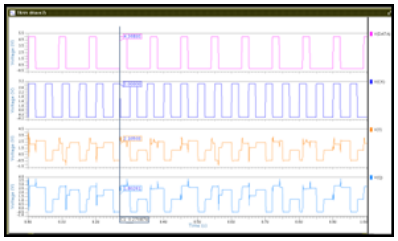

Fig. 10. Simulation Result for Single Ended Conditional Capture Energy Recovery Flip Flop

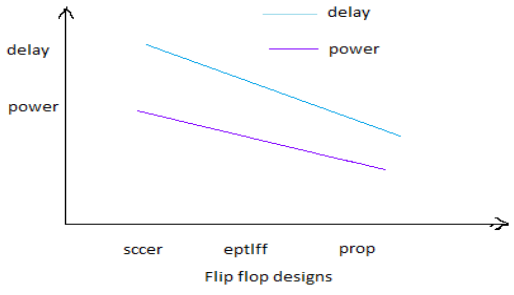

Fig. 11. Expected graph of the proposed and conventional designs

The expected graph for the proposed and conventional design is shown in Fig. 11. It shows that proposed design is much more efficient in terms of power and delay as compared to the conventional circuits.

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VI. CONCLUSION

A synchronous counter using these flip flops has to be designed and performance is analyzed and comparison is carried out in terms of power, area and delay. It is expected to have low power consumption for the proposed flip flop and counter than other conventional designs.

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