

Fractional N-Phase Locked Loop using VLSI Technology

Chaitali P.Charjan¹, Asso.Prof.Atul S.Joshi²

PG student, Department of Electronics & Telecommunication, Sipna's college of Engineering & Technology, Amravati, Maharashtra, India ¹

Associate Professor, Department of Electronics & Telecommunication, Sipna's college of Engineering & Technology, Amravati, Maharashtra, India ²

Abstract: Literature survey of Phase Locked Loop reflects that many researchers have applied different techniques like digital and analog simulation by applying mathematical/logical relations to design the Phase Locked Loop (PLL) . Researchers have undertaken different systems, processes or phenomena with regard to design and attempted to find the unknown parameters and analyzed PLL. Since in the real world today VLSI/CMOS is in very much in demand, it is observed that very few researchers have undertaken the work for designing PLL using CMOS/VLSI technology, after the careful study of reported work. In the proposed work, low power PLL with multiple outputs is designed with stability of system and there are no fractional spurs in the output spectrum of the fractional-N phase locked loop.

Keywords-Phase Locked Loop; Sigma-Delta modulation; Frequency Synthesizer; Fractional-N; Phase Noise

I. INTRODUCTION

The Phase locked loop is a feedback system as can be seen in the figure. It is a basic building block which is widely used in communications system such as mobile phones, which may contain up to 5 PLL's. Another important application are in motor speed control and for optical disk drive (ODD's) as found in DVD's and CD players. The basic PLL can be analog or digital. A phase locked loop (PLL) is used for different purposes in various sectors such as communication and instrumentation. In the microwave range they are used in frequency synthesis and phase recovering among others. To maintain a well-defined phase and hence frequency relation between two independent signal sources, phase-locked loop can be used. Basic PLL consists of three elements: a phase detector, a loop filter and a voltage controlled oscillator (VCO) as shown in figure.

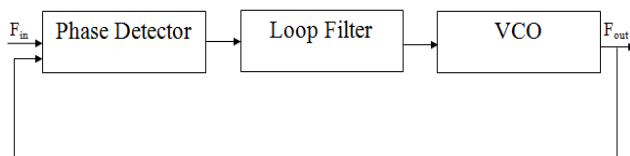


Figure 1. : Block diagram of PLL

The output voltage of phase detector is proportional to the phase difference between the VCO's output signal and the reference. The phase detector's output produces a regular square oscillation when the clock input and signal input have one quarter of period shift or 90° ($\pi/2$). For angles other than 90° , the output is not regular. The phase error voltage controls the VCO's frequency after being filtered by the loop filter.

The filter used in PLL transforms the phase difference into an analog control voltage which is same as the average

output of phase detector. The filter converts rapid variations of the phase detector output into a slow varying signal, which later controls the voltage controlled oscillator.

The most vital part of PLL is VCO which is used to produce clock in phase locked loop circuits. This unit ingests most of the power in the system in addition to operating at highest frequency i.e. the VCO reduces power consumption.

Design and analysis of a low power fractional-N phased-locked loop is basically implemented by modifying conventional Phased-locked loop circuit. The proposed work is aimed at achieving the low power consumption and high stability for phase locked loop. Power is the most significant parameter for communication systems such as optical data links, wireless products, microprocessor designs. Hence, to achieve very low power consumption, this work is implemented using VLSI technology.

Due to the benefits and current demand in communication technology, the effort has been taken to design proposed phase-locked loop or phase lock loop (PLL) using VLSI technology. A phase locked loop (PLL) is divided into two architectures, an integer-N PLL and a fractional-N PLL, of which, the main problem with the integer-N PLL is the trade-off between the channel spacing (frequency resolution) and the loop bandwidth. A small channel spacing or high frequency resolution needs a small reference frequency (Fref), but using a small reference frequency leads to two main issues. First, for stability requirement the loop bandwidth must be smaller than the reference frequency ($f_B.W \ll 0.1 \text{ Fref}$), hence a low reference frequency means a small loop bandwidth, and this will result in slow switching time and the second one is , reducing the reference frequency causes an increase in

the phase noise because of the high division ratio. The fractional-N PLL solves the trade-off issue set up in the integer-N PLL, offering a higher frequency resolution, lower phase noise, and a larger loop bandwidth. A larger loop bandwidth means faster switching time. The output frequency of the fractional-N PLL is $f_{out} = (N.\alpha) * F_{ref}$, where N is an integer, and α is any fraction. We know that, Phase locked loops (PLLs) have been extensively used in the electronic systems as frequency synthesizers. The performance of a frequency synthesizer is measured according to its frequency range, frequency resolution, settling time, and spectral purity. As compared with the classical integer frequency synthesizer, fractional-N frequency synthesizer provides with some additional advantages, such as fast settling time and better phase noise suppression that comes with a larger loop bandwidth. Despite of all its advantages, the fractional-N frequency synthesizer suffers from the fractional spurs.

The limitation of this method is that the periodic operation of the dual modulus divider generates a spurious tone which is called fractional spurs. If these spurs occur inside the loop bandwidth, this problem can be solved by reducing the loop bandwidth to remove these spurs, which in turn will increase the switching time. The best method to remove the fractional spurs without affecting the loop bandwidth is by breaking the periodicity of the dual modulus operation, which is accomplished by using a Sigma-Delta Modulation technique.

The Sigma-Delta modulator changes the division ratio between more than two values, so the spurs will spread over the spectrum. The Sigma-Delta modulator generates a random integer number with an average equal to the desired fractional ratio and pushes the spurious contents to the higher frequencies. Then the spurious contents are removed by the loop filter action.

II. LITERATURE REVIEW

In 2006, Erkan Bilhan, Feng Ying, Jason M. Meiners, Liming Xiu[6], proposed architecture for spur-free fractional-N PLL making use of precision frequency and phase selection to provide better resolution for the fraction and to avoid any compensation that is required for the correction of the instantaneous jitter. The proposed architecture does not produce any spurs due to fractional frequency synthesis. As a result it provides better resolution for the fraction and avoids any compensation required for correction of the instantaneous jitter. In this paper a new method to obtain fractional frequencies has been described. For this purpose, to avoid the fractional spurs and any circuitry related with the compensation or suppression of these spurs, use of the phases available from a ring oscillator is made.

In 2007, Richard Gu and Sridhar Ramaswamy [5] discussed the architecture of a sigma-delta PLL and the relation between the PLL bandwidth and the order of the sigma-delta modulator. This paper presents the design and applications of fractional-N sigma-delta phase locked loop (PLL). The applications focus mainly on wireless communication and clock synthesizers. Here, the

comparison of performance of multi-stage noise shaping (MASH) and single-loop sigma-delta modulators is done. The causes of fractional spurs and spur reduction techniques are discussed here.

The phase locked loop (PLL) is a rudimentary part of consumer electronics, crystal oscillator frequency, wireless and Radio, telecommunication, multiplication and clock synthesizer. The PLL is used to accomplish frequency or phase modulation and demodulation, clock recovery, jitter suppression in communication systems, frequency synthesis, skew suppression and edge detection. The PLL's work is to multiply the reference frequency by either an integer or a fractional number. A PLL with an integer multiplication is called an integer-N PLL, while a PLL with a fractional multiplication is called a fractional-N PLL. An integer-N PLL finds it difficult to meet various specifications due to the basic tradeoff between frequency spacing and loop bandwidth. A high frequency resolution requires a very large feed-back divider and a very low PLL bandwidth which results into a long settling time and increased in-band phase noise. A large loop-filter capacitor is required by a low loop bandwidth PLL. The integrated loop filter occupies large silicon area and therefore an external loop filter is required. A fractional-N PLL offers benefits over an integer-N PLL by decoupling frequency resolution from the PLL bandwidth. Therefore, a fractional-N PLL can achieve high bandwidth, fast lock and narrow frequency spacing to meet communication system needs.

In 2008, Xiao Pu, Axel Thomsen, Jacob Abraham [4], compared several techniques for increasing bandwidth including an improved version of one recently proposed by the authors. Circuits that suppress fractional spurs along the signal path are discussed. The loop bandwidth of fractional-N PLL is an appropriate parameter for many wireless communication applications. To improve bandwidth design tradeoffs must be made among different circuit blocks. The key to successful implementation of a wideband fractional-N synthesizer is in managing jitter and spurious performance. In this paper several techniques for bandwidth enhancement including an improved version of one recently proposed by the authors are compared. Circuits that suppress fractional spurs along the signal path are discussed.

Fractional-N PLL (FNPLL) is a well known technique to synthesize a clean, stable and programmable frequency source from a fixed reference, with fine resolution.

The reference frequency F_{ref} is no longer limited by the resolution requirement as is the case for integer-N synthesizers. Since loop bandwidth (BW) is generally kept within 5% of the reference frequency, a higher reference frequency means a higher bandwidth. For wireless communication applications, a wider bandwidth is mostly desirable. Wider bandwidth allows expedient digital in-loop modulation and has a faster settling response to frequency or phase steps, and also causes large attenuation of the phase noise in the VCO. In addition, a wideband

PLL uses smaller R and C components to implement the loop filter; this makes possible a single chip solution of RF system in standard CMOS technologies. In $\Delta\Sigma$ fractional-N PLL, a $\Delta\Sigma$ modulator is used to modulate the desired fractional number into a sequence of integers so that the divided clock approximates the desired fractional ratio over time. As a byproduct of this process, and for fractional-N PLLs in general, the instantaneous clock edges are never truly locked, except only momentarily. Even though the loop achieves steady state by aligning the time average of the divide-down clock to the reference clock. This creates significant noise on the feedback clock. If this noise is removed through additional loop filter poles then Fractional N-PLL does not provide with the bandwidth advantage over integer-N PLL with same reference frequencies. The tradeoff between loop bandwidth and phase noise shows the primary limitation in fractional-N PLLs.

In 2010, Fatah and H. Nabovati [1] designed and simulated fractional-N phase locked loop frequency synthesizer using sigma-delta modulation technique for bluetooth systems. A fractional-N PLL is proved to be advantageous over an integer-N PLL by decoupling frequency resolution from the PLL bandwidth. Hence, high bandwidth, fast lock and narrow frequency spacing to meet communication system requirement, can be achieved by the fractional-N PLL.

The fractional-N frequency synthesis technique provides supple switching in narrow channel spacing systems and improves phase-locked loop (PLL) design constraints for phase noise and reference spur. A sigma-delta modulator is represented in this work which reduces spur in output frequency spectrum of the fractional-N frequency synthesizers (FS). This technique also alleviates the performance of the frequency synthesizer. A fractional-N frequency synthesizer is designed by employing a third-order MASH modulator. A fourth order type II PLL with two out of band poles is used to suppress quantization noise of the modulator. The in-band phase noise of -95 dB/Hz at 10-kHz offset with a spur of less than -96 dB is achieved with a reference frequency of 8 MHz and a loop bandwidth of 40 kHz. The traditional integer-N frequency synthesizers based on a phase locked loop (PLL) are suffering from limitations in meeting desired specifications due to the fundamental trade-off between the loop bandwidth and the channel spacing. Regarding their high division ratio, meeting the noise requirement using the integer-N synthesizers is also challenging when implemented with CMOS Technology. A fractional-N PLL has advantages compared with the traditional integer-N implementations, namely: better phase noise performance, faster lock, and better spur levels. The benefits of fractional-N PLLs come from both a larger loop bandwidth and higher phase-frequency detector (PFD) frequencies. A larger loop bandwidth infers better voltage controlled oscillator (VCO) phase noise suppression and faster locks time. On the other hand, fractional-N techniques provide wide bandwidth with narrow channel spacing and improve PLL design

constraints for phase noise and reference spur. The intrinsic problem of the fractional-N frequency synthesizer is that the periodic operation of the dual-modulus divider produces spurious tones. Several spur reduction techniques have been proposed in the literature; among them the sigma-delta modulation technique is considered in this work to boost the overall synthesizer performance. The main aim of this work is to develop a practical frequency synthesis technique for high spectral purity using the sigma-delta modulation method, which is applicable to low-cost wireless transceivers. In this work, the oversampling modulator performance has been analyzed by considering practical design aspects in fractional-N frequency synthesis, and a high-order MASH sigma-delta modulator is proposed to improve the overall performance, and curb the phase noise and spur.

From the careful study of reported work, it is observed that researchers have proposed various techniques to design the chip and to improve its characteristics and various parameters. But up to the result of my survey regarding PLL design; very few researchers had suggested the High performance VCO which includes delay cell with linear delay dependence on the control voltage. It is also well known to that; VLSI technology is the fastest growing field today. And according to Moore's law which state that, the number of transistors on an integrated circuit will double every 18 months. By scaling down the technology, we can optimize the parameters like power consumption. The current technology up to 2008 was 90 nm technology. Hence considering the advancement of future technology and the advantage of 45 nm technology over 65 and 90 nm technology, the proposed project has been decided to do with the selection of 45nm technology. Again from review of various researches under taken on PLL, it is observed that the proposed research to design low power PLL with multiple outputs is totally a new concept and superior to all the conventional techniques. Since multiple output of PLL generates multiple clocks at a time, it can be useful for multi channeling wireless communication system. Considering all this constraint regarding the demand of today's fast communication world, the research has been taken to design low power multiple output PLL using 45nm VLSI technology.

III. CONCLUSION

The proposed work provides with a low power PLL with multiple outputs. Since multiple output of PLL generates multiple clocks at a time, it can be used for multichanneling wireless communication system. Taking into account all these constraints regarding the demand of today's fast speed communication, the research has been taken to design low power multiple output PLL using 45nm VLSI technology.

IV. REFERENCES

- [1] N.Fatahi, and H.Nabovati, "Design of low noise fractional-N frequency synthesizer using Sigma-Delta Modulation technique," 27th International Conference of Microelectronics, IEEE, 2010.
- [2] N. Fatahi, and H. Nabovati, "Sigma-Delta Modulation technique for low noise fractional-N frequency synthesizer," Proceedings of the

- 4th International Symposium on Communications, Control and Signal Processing, ISCCSP 2010, Limassol, cyprus, 3-5 March 2010.
- [3] Shiwei Cheng, Ke Zhang, Shengguo Cao, Xiao fang Zhou, and Dian Zhou, "2.4 GHz ISM band Delta-Sigma fractional-N frequency synthesizer with automatic calibration," WSEAS Transactions on Circuits and Systems, Volume 7 Issue 10, October 2008, pp. 859-868.
- [4] Xiao Pu, Axel Thomsen, Jacob Abraham, "Improving Bandwidth while Managing Phase Noise and Spurs in Fractional-N PLL", IEEE Computer Society Annual Symposium on VLSI, 2008.
- [5] Richard Gu, and Sridhar Ramaswamy, "Fractional-N phase locked loop design and application," 7th International Conference on ASIC Proc. October 26-29, 2007, pp. 327-332.
- [6] Erkan Bilhan, Feng Ying, Jason M. Meiners, and Liming Xiu, "Spur free fractional-N PLL utilizing precision frequency and phase selection," IEEE Dallas/CAS Workshop on Design, Applications, Integration and Software, 2006.
- [7] T.Bourdi, A.Borjak, and I.Kale, "A Delta-Sigma frequency synthesizer with enhanced phase noise performance," Instrumentation and Measurement Technology Conference, Proceedings of 19th IEEE, 2002, pp.247-250
- [8] Kaveh Hosseini and Michael Petter Kennedy, " Minimizing spurious tones in digital Delta Sigma modulators," Analog Circuits And Signal Processing, pp30-31
- [9] Sangil Park, "Principles of Sigma-Delta Modulation for analog-to-digital converters," Chapter 6, pp.8
- [10] Behzad Razavi, "Rf Microelectronics," University of California, Los Angeles, Second Edition. Pp.742-746.
- [11] Dean Banerjee, "PLL performance, simulation, and design," 4th Edition, pp.186-197.
- [12] Paul C. A. Roberts, "Understanding phase noise in RF and microwave calibration applications," NCSL International Workshop and Symposium, 2008
- [13] Kevin J.Wang, Ashok Swaminathan, Ian Galton, "Spurious tones suppression techniques applied to a wide-bandwidth 2.4 GHz fractional-N PLL," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 43, NO. 12, DECEMBER 2008, pp.2787-2797.
- [14] Wong Man Chun, "A 1.8-V 2.4-GHz Monolithic CMOS Inductorless frequency synthesizer for bluetooth application," thesis master, Hong Kong University of Science and Technology, August, 2002.
- [15] Yi-Da Wu, Chang-Ming Lai, Chao-Cheng Lee, and Po-Chiun Huang "Error minimization method using DDS-DAC for wideband fractional-N frequency synthesizer," IEEE Journal of Solid-State Circuits, 2010, pp.2283-2291

BIOGRAPHIES



Chaitali P.Charjan received the bachelor's degree in Electronics and Telecommunication Engineering from Prof. Ram Meghe College of Technology & Research, Amravati, Maharashtra, India and currently pursuing M.E in Electronics &Telecommunication from Sipna College of Engineering & Technology, Amravati, Maharashtra, India.



Asso.Prof. Atul S.Joshi is currently working as an Associate Professor in Electronics and Telecommunication Engineering Department, Sipna College of Engineering & Technology, Amravati, Maharashtra, India.