

# Design of area efficient chip layout of fractional N-phase locked loop using VLSI technology. A review

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**Abstract:** In communication system power is one of the most important parameter. Power is the amount to function or generating out energy. This means that it is a way of measuring how fast a function can be carried out. So power has become one of the most important parameter in various communication systems such as optical data links, wireless products, microprocessor. This topic presents the design of an area efficient chip layout of fractional-N phase locked loop for Bluetooth application using VLSI technology. Phase locked loop is a control system that generates an output signal whose phase is related to the phase of an input signal. This phase locked loop is designed using VLSI technology, which offers high speed performance at low power. Loop filter and Sigma-Delta modulator are the most important factors in improving the performance of fractional-N phase locked loop. The digital Sigma-Delta modulator provides a useful noise shaping for the phase noise introduced by the fractional division operation, while the loop filter bandwidth limits the speed of switching time between the synthesized frequencies.

**Keywords:** Phase locked loop, sigma delta modulator, Divide by N- counter Voltage controlled oscillator.

## I. INTRODUCTION

Phase locked loop is a control system that generates an output signal whose phase is related to the phase of an input reference signal. Phase locked loop is widely employed in radio communication computer and other electronic applications. Power has become one of the most important parameter in various communication systems such as wireless products, optical data links, microprocessor. For maintaining a well-defined phase and hence frequency relation between two independent signal sources, phase-locked loop can be used.

Monolithic phase locked loops have been used for clock & data recovery in communication system, clock generation & distribution in microprocessor and frequency synthesis in wireless application PLL is used in wireless communications where the oscillator is usually at the receiver and the input signal is extracted from the signal received from the remote transmitter.

Phase locked loop, an electronic circuit that controls an oscillator so that it maintains a constant phase angle (i.e. lock) on the frequency of an input or reference signal. Basic PLL is a feedback system consist of three elements: a phase detector, a loop filter and a voltage controlled oscillator (VCO).

The phase detector compares the phase of the input signal with the phase of the signal derived from its output oscillator and adjust the frequency of oscillator to keep the phase matched. The phase detector output produces a regular square oscillation when the clock input and signal input have one quarter of period shift or  $90^\circ$  ( $\pi/2$ ).

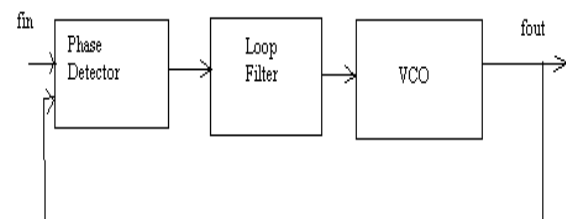


Figure. Block Diagram of phase locked loop

The low pass filter is used in PLL which is used to remove high frequency components from the output of phase detector. The filter converts rapid variations of the phase detector output into a slow varying signal, which will later control the voltage controlled oscillator. The most important part of PLL is VCO which is used to generate clock in phase locked loop circuits. This unit consumes the most of the power in the system in addition to operating at highest frequency means the VCO is for reducing power consumption

## II. LITERATURE REVIEW

The electronics industry is the fastest growing field mainly due to the rapid advances in integration technologies. VLSI Technology is the advance technology. Many researchers design the Phase locked loop by applying various mathematical & Logical expressions using different phenomenon or processes for finding various parameters.

From the review of related work and published literature, it is observed that many researchers have designed Phase Locked Loop (PLL) by applying different techniques.

Today VLSI/CMOS is very much in demand, from the careful study of reported work it is observed that very few researchers have taken a work for designing PLL with CMOS/VLSI technology.

One of the important design of low power phase locked loop (PLL) using 45nm VLSI technology is given by U. Belokar et.al [1]. They designed and analyzed the low power PLL using 45 nm CMOS/VLSI technology with micro wind 3.1 with four multiple outputs which provides high efficient, optimum area chip with low power of 0.211 mw and four multiple outputs with high stability.

Another important implementation of phase lock loop is describe by H. Nabovati et.al. [2]. They implement the fractional-N frequency synthesizer using Sigma-Delta modulation technique which offers a short switching time and a good noise reduction performance. A loop filter offers the best suppression to the quantization noise at high frequencies. The simulation results showed that chosen bandwidth and phase margin yield fast switching time.

Another important application of PLL is given by H. Perrott[3]. He will focus on the design of a Sigma-Delta frequency synthesizer intended for a direct conversion GSM cell phone transmitter. In this, he used the PLL Design Assistant and CppSim programs to design a frequency synthesizer at the system level that is intended for a GSM transmitter application. Using the PLL Design Assistant, he examine the noise performance of the synthesizer under different configurations and thereby select a candidate approach that met the GSM noise specifications and also met the settling time requirements under nominal conditions.

Another important application of Phase locked loop as frequency synthesizer and its model is described by Yang [9] in 1997. Author proposed a model of a phase-locked loop (PLL) frequency synthesizer. The voltage-controlled oscillator (VCO) utilizing a ring of single-ended current-steering amplifiers (CSA) provides low noise, wide operating frequencies and operation over a wide range of power supply voltage. A programmable charge pump circuit automatically configures the loop gain and optimizes it over the whole frequency range. The PLL frequency ranges are 0.3–165 MHz and 0.3–100 MHz measured at 5 V and 3 V supplies, respectively. The peak-to-peak jitter is 81 ps (13 ps rms) at 100 MHz. The chip is fabricated with a standard 0.8m n-well CMOS process PLL (phase locked loop) is designed for high-frequency, low-voltage, and low-power applications by Moon[6]. This paper proposes a new PLL architecture to improve the voltage to frequency linearity of a VCO (voltage controlled oscillator) with a new delay cell. The proposed VCO operates in a wide frequency range of 30 MHz\_1 GHz with good linearity. The DC-DC voltage up/down converter is newly designed to regulate the control voltage of the two-stage VCO. The designed PLL architecture is implemented on a 0.6m n-well CMOS process. The simulation results show a locking time of 2.6 sec at 1 GHz,

a lock in range of 100 MHz\_1 GHz, and a power dissipation of 112 mW. Simulations of the proposed PLL circuit were performed in a standard 0.6-m CMOS technology.

From review of various researches under taken on PLL, it is observed that the proposed work to design area efficient low power fractional - N PLL Frequency synthesizer using VLSI technology is a new concept and superior to all the conventional techniques. By using the VLSI technology we can reduce the power consumption and area required. VLSI technology is the fastest growing field today. Hence considering the advancement of VLSI technology and the advantage of 32 nm technology over 45 and 65 nm technology, the proposed work is implemented with 32 nm technology.

Due to the current demand in communication technology, the proposed Fractional-N phase-locked loop is decided to design using 32 nanometre (nm) VLSI technology to achieve less area, low power consumption and high stability.

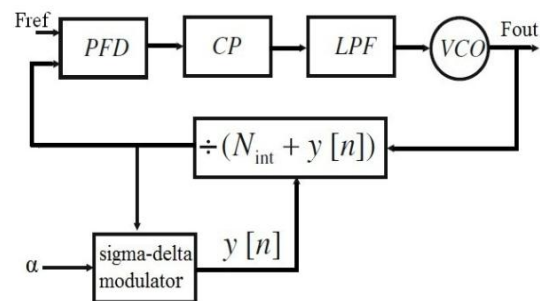


Figure Proposed Block Diagram of PLL using Sigma-delta fractional -N frequency synthesizer

The proposed PLL is designed using 32 nm CMOS/VLSI technology in microwind 3.1. The main novelties related to the 32 nm technology are very low-k interconnect dielectric, the high-k gate oxide and metal gate. The effective gate length required for 32 nm technology is 18nm.

Compared to 45-nm technology, 32 nm technology must offer:

- 30% increases in switching performance
- 30 % reduction in Power consumption
- 2 times higher density
- 2 times reduction of the leakage between source and drain and through the gate oxide.

## CONCLUSION

The current technology up to 2008-2009 was 90 nm technology. Considering the advantages of 32 nm over 45 and 65 nm technology, the selection of 32 nm technology for the proposed work is the proper choice of technology. To design area efficient chip layout of fractional N-PLL using VLSI technology, first phase lock loop circuit and sigma delta modulator will have to design using 32 nm VLSI technology. So that after cascading all these blocks we will get short switching time, good noise reduction and less power consumption.

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