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Solar PV Fed Interleaved Boost Sepic Converter

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Abstract: Increased threat of environmental contamination, global warming and other environmental factors significantly contributes to the development of renewable energy sources (RES). Among the RES, solar photovoltaic (PV) has become the most promising technology. PV has several advantages that it is free, abundant, noise free and pollution free. This paper presents an interleaved boost sepic converter which utilizes the benefits of interleaved topology. The interleaving effect of source inductors ensures low ripple current drawn from PV source. The power stage has been split into smaller ones and hence the cost and ratings of components has been reduced. This converter can operate in either voltage control mode or current control mode. Due to low ripple current from the PV source, the maximum power point tracking (MPPT) efficiency is increased. Incremental conductance(IC) based MPPT control algorithm, along with a PI controller is used to track maximum power. Under rapidly varying irradiation conditions, IC method tracks maximum power point (MPP) with minimum error. The simulation of interleaved boost sepic converter has been done in MATLAB software. It has been observed that input inductor current ripple has been reduced. The interleaved boost sepic converter can be used for low voltage dc micro grid applications. The increased component count of the interleaved boost sepic converter can be justified by the reduced cost.

Keywords: Renewable Energy Source (RES), Photo Voltaic (PV), Maximum Power Point Tracking (MPPT), Incremental Conductance (IC).

I. INTRODUCTION

The wide spread usage of fossil fuels in recent decades has caused resource reduction and a dramatic increase in environmental pollution. Severe pollution caused by the consumption of fossil fuels endangers human health and natural life. These reasons cause people to prefer renewable energy sources. Renewable energy sources like solar, wind, fuel cell etc., are gaining an increasing share of the global electricity generation. Among the renewable energy sources, photovoltaic (PV) source is one of the significant players in the world's energy scenario. Reduction of carbon dioxide emissions is the greatest advantage of PV. According to experts, the energy obtained from PV cells will become the most important alternative renewable energy source until 2040 [1]. The number of home appliances operating on dc is also growing rapidly. These RES, storage units, and dc loads are efficiently interfaced to a dc micro grid environment compared to the ac microgrid. In dc microgrid, converters for multiple power conversion are eliminated. Hence, low voltage dc micro grid is gaining popularity and would be the technology for the future [2].

Many non isolated dc-dc converters suitable for PV applications are available in the literature. Conventional boost converter is the simplest one. However, parasitic effects are caused due to high duty ratio operation of boost converter [3]. Three level boost converter offers high voltage gain with increased voltage and current stress of power devices. The output diode reverse recovery problem of three level boost converter has been avoided by the active zero voltage transition (ZVT) three level boost converter [4]. However, the ringing induced by the parasitic capacitor of the active clamp switch and the resonance inductor increases the switch voltage stress in ZVT three level boost converter. The coupled inductor based converter topologies caused severe electromagnetic interference problems, switching losses, voltage and current stress. Many interleaved converter topologies has been proposed in the literature. The advantage of these converters is that they draw very low ripple current from the source. Also, they have reduced current stress and filter size. The disadvantage is that they are single output converters [5]-[9]. Hence, these interleaved converters are not suitable for dc micro grid requiring dual output for various applications.

This paper discusses about an interleaved boost plus sepic converter which is a single input dual output converter. The converter has PV as input and can be used for low voltage dc micro grid application.Low ripple in source current is an advantage especially in case of PV source since the efficiency of the MPPT would be high.The current stress, effective filter size and current rating of the switches are also reduced due to interleaving [10].

The power of PV modules is unstable and strongly dependent on solar irradiation and load. The efficiency of energy conversion is currently low, and the initial cost for its implementation is considered high. Thus, it becomes necessary to

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use techniques to extract the maximum power from these panels, in order to achieve maximum efficiency in operation. Hence, the maximum power point tracking (MPPT) controller is introduced to ensure the PV system always provide high efficiency despite the variation in solar irradiation and load resistance [11], [12].
Many MPPT algorithms can be used to improve the efficiency of the PV system, including fractional open circuit voltage, fractional short circuit current, fuzzy logic, neural network, hill climbing or perturbation and observation (P&O) and incremental conductance(IC) [13]-[19]. Among those algorithms, P&O and incremental conductance are the most popular algorithms. Under rapidly changing illuminations, incremental conductance method provides better transient response and MPP is tracked with minimum error [20]. In this paper, an incremental conductance MPPT algorithm is used.

II. PV FED INTERLEAVED BOOST SEPIC CONVERTER

The output voltage of PV panel is very low and PV panel has nonlinear characteristics. In order to step up the low PV output voltage we require a dc-dc converter at the panel end. Interleaved boost sepic converter has been used at the panel end which has benefits of reduced input current ripple, reduction in current stress and filter size.

A. Interleaved boost sepic converter

The interleaved boost sepic converter can be obtained by paralleling conventional boost and sepic converter with a phase shift of 180°. The PV panel output current is shared among the input inductors. Fig.1 shows the circuit diagram of interleaved boost sepic converter.

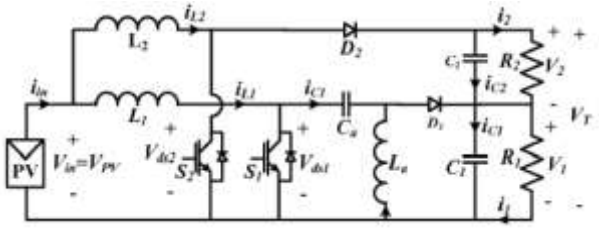

Fig.1. Circuit diagram of interleaved boost sepic converter

The converter operates under following assumptions.
1) The switches of the converter are assumed to be ideal, i.e., forward voltage drop and on-state resistances of the switches are neglected.
2) Passive components of the converter (R, L, and C) are assumed to be linear.
3) Continuous inductor current mode is assumed.

The converter can be operated in current control (CC) mode and voltage control (VC) mode.The mode of operation depends upon the input source connected to the converter. In case of solar PV source, the converteris operated in CC mode, where the PV current is controlled bycontrolling the currents through inductor $L_1$and L_2. In this case switches are controlled to control the inductor currents, i_{L1} and i_{L2}.The converter can be operated in VC mode, when a dispatch able dc source like battery or ultra-capacitor is connected to the input terminals. In case of VC mode, switches are controlled to control the output voltages V_1 and V_T.
The source inductors are designed such that $L_1 = L_2 = L$ and in such a way that the converter operates in CCM. In this, single-input-dual-output converter, there can befour possible switching states depending upon the status ofswitches S_1 and S_2.The operation of the circuit under four different switching states are summarized in Table I:

TABLE I Switching States

S1	S2	L1	L2	C1	C2
0	0	Discharge	Discharge	Charge	Charge
0	1	Discharge	Charge	Charge	Discharge
1	0	Charge	Discharge	Charge	Charge
1	1	Charge	Charge	Discharge	Discharge

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A. Steady state equations of the converter

For the interleaved boost sepic converter, D_1 and D_2 are the duty ratios of the switch S_1 and S_2 respectively. V_T is the total output voltage of the converter. The steady state waveforms of the converter are shown in Fig.2. Under steady-state and during CCM operation, the relationships between the output voltages V_1 and V_T with the input voltage are given by the following equations:

$$V_1 = V_{in} * \frac{D_1}{1-D_1} \quad (1)$$

$$V_T = V_1 + V_2 = V_{in} * \frac{1}{1-D_2} \quad (2)$$

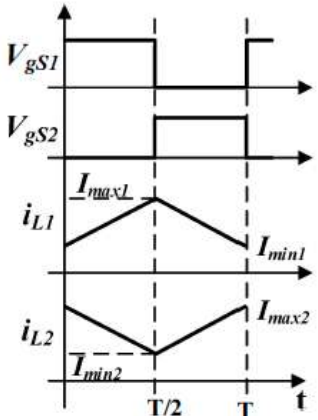

Fig.2. Steady state waveforms of the converter

To analyse the performance of the converter and to prove that the ripple in the current drawn from the source is minimum, the input voltage is considered to be equal to V_1 for simplicity

$$V_{in} = V_1 = \frac{V_T}{2} \quad (3)$$

The duty ratio of the converter at steady state is given by:

$$D_1 = D_2 = 0.5 * T_s \quad (4)$$

The current ripple in the inductors L_1 and L_2 is given by:

$$\Delta i_{L1} = \Delta i_{L2} = \frac{V_{in}}{L} * DT_s \quad (5)$$

The inductor currents and source current for the switching states, S_1=1, S_2=0 and for conditions (3) and (4) are given by:

$$i_{L1}(t) = \frac{V_{in}}{L} * t + I_{min\,1} \quad (6)$$

$$i_{L2}(t) = -\frac{V_{in}}{L} * t + I_{max\,2} \quad (7)$$

$$i_{in}(t) = i_{L1}(t) + i_{L2}(t) = I_{min\,1} + I_{max\,2} \quad (8)$$

The inductor currents and source current for the switching states, S_1= 0, S_2=1and conditions (3) and (4) are given by:

$$i_{L1}(t) = -\frac{V_{in}}{L} * t + I_{max\,1} \quad (9)$$

$$i_{L2}(t) = \frac{V_{in}}{L} * t + I_{min\,2} \quad (10)$$

$$i_{in}(t) = i_{L1}(t) + i_{L2}(t) = I_{max\,1} + I_{min\,2} \quad (11)$$

B. Incremental conductance MPPT control

Incremental conductance method uses two sensors, that is voltage and current sensors to sense the output voltage and current of the PV array. In this method, the array terminal voltage is always adjusted according to the MPP voltage. It is based on the incremental and instantaneous conductance of PV module. Algorithm works by comparing the ratio of derivative of conductance with the instantaneous conductance. Incremental conductance method offers good performance under quick changing circumstances; it is also simple and can be implemented using low cost microcontroller. The basic equations are as follows [20]:

At maximum power point (MPP),

$$\frac{dp}{dv} = 0 \quad (12)$$

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The condition on the left of MPP,

$$\frac{dI_p}{dV_p} > -\frac{I_p}{V_p} \quad (13)$$

The condition on the right of MPP,

$$\frac{dI_p}{dV_p} < -\frac{I_p}{V_p} \quad (14)$$

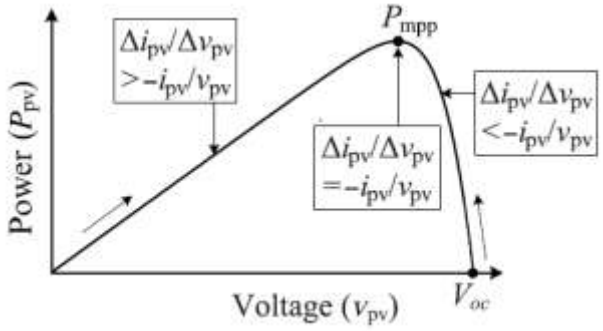

Fig.3.Illustration of IC method with PV array PV characteristics

In theory, the steady-state oscillations would be eliminated once the derivative of power with respect to voltage is null at MPP. However, a null value of this slope hardly everoccurs due to digital implementation resolution. Hence there will always be an offset value of dP_p/dV_p at the steady state. Improvement in IC method by reducing this offset is achieved by adding a simple PI controller in the control loop. The IC method along with PI controller minimizes the error between the actual conductance and the incremental conductance. The implementation of IC method using PI controller is shown in Fig.4.

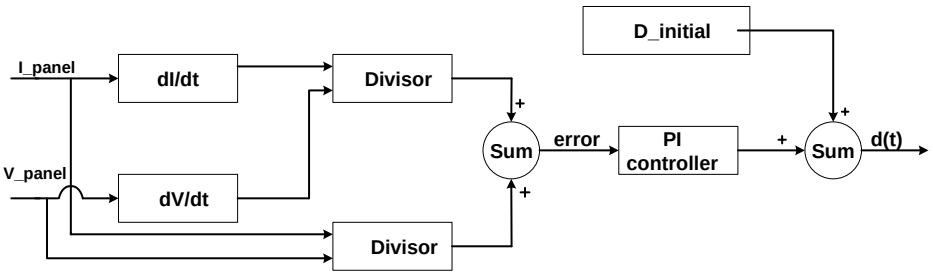

Fig.4. Implementation of IC method with PI controller

III.SIMULATION RESULTS

The interleaved boost sepic converter performance for incremental conductance MPPT algorithm with PI control has been studied. The design parameters are given in Table II. The values of proportional and integral control are: k_p=0.05 and k_i=1. The irradiation has been varied from 500W/m^2 to 1000W/m^2 at 0.3s. Initial dutycycle has been set to 0.5.

TABLE II Design Parameters

Symbol	Values
L_1,L_2,L_a	250µH
C_1,C_2,C_3	1000µF
f_s	30kHz
V_{in}	22V
P_o	200W
R_1	3.84Ω
R_2	11.52Ω
V_T	48V
V_1	24V

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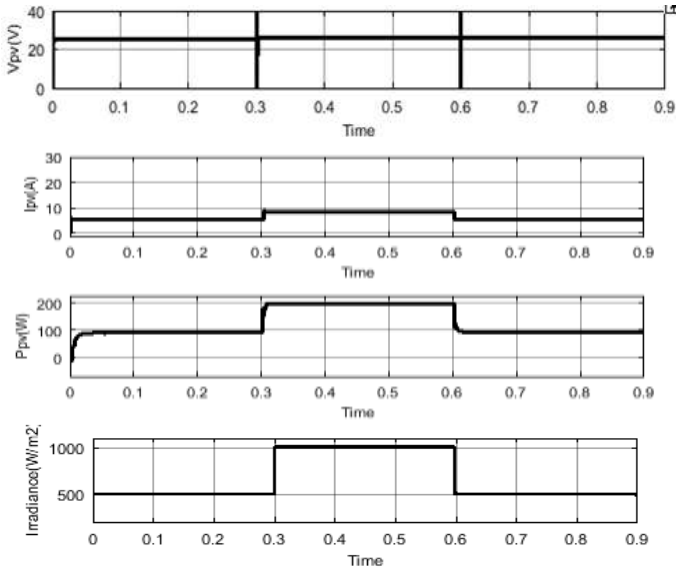

Fig.5. PV panel output voltage, output current, PV power and irradiation of interleaved boost sepic converter with IC algorithm

The PV panel output voltage, output current and PV power waveforms for two irradiation levels has been shown in Fig.5. The PV panel output power for an irradiation of 500W/m^{2}has been found to 95 W. For an irradiation of 1000W/m^2, PV panel output power was about 195W. Fig.6. shows the output voltage forinterleaved boost sepic converter for different irradiation conditions.

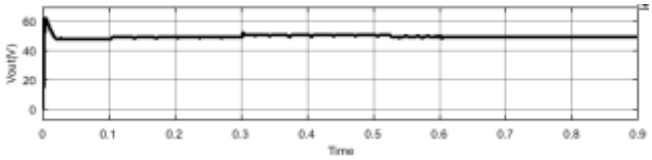

Fig.6. Output voltage of the interleaved boost sepic converter

The output power for the interleaved boost sepic converter for an irradiance of 1000W/m^2 is shown in Fig.7.

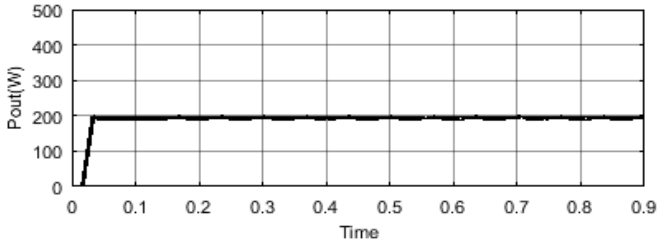

Fig.7. Output power of the interleaved boost sepic converter for irradiance 1000 W/m^2

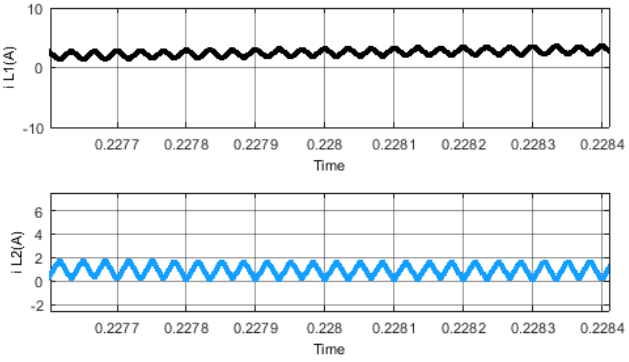

Fig.8. Input inductor current waveform

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Fig.8. shows the inductor current wave forms for interleaved boost sepic converter. The ripple in inductor currents was found to be very low due to interleaving. Input inductor current ripple for boost part and sepic part of the interleaved boost sepic converter has been obtained as 0.33A.

IV. CONCLUSION

An interleaved boost sepic converter has been designed. Simulation of PV fed interleaved boost sepic converter with an incremental conductance algorithm has been done in MATLAB.The MPPT algorithm extracts the maximum power under different irradiation conditions. The input inductor current ripple was found to be very low due to interleaving. Ratings of the power electronic components were reduced due to current sharing in the interleaved topology. The performance of the converter could further be improved by fast tracking MPPT algorithm. Highcomponent count associated with the interleaved circuit is justified by the lower ratings of the components. The interleaved boost sepic converter finds its application in dc micro grid.

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BIOGRAPHIES

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