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Implementation of an Efficient Adaptive Feedback Equalization for Ladner Fischer Adder

S. Ayesha

P.G Scholar, VLSI Design, Department of ECE, Srinivasan Engineering College, Perambalur, India

Abstract: An Efficient tunable subthreshold logic circuit designed by using adaptive feedback equalization circuit. This circuit used in Ladner Fischer adder. This circuit used in a sequential digital logic circuit to mitigate the process variation effects and reduce the dominant leakage energy component in the subthreshold region. Feedback equalizer circuit adjusts the switching threshold of its inverter. It is based on the output of the flip-flop in the previous cycle to reduce the charging and discharging time of the flip-flop's input capacitance. Moreover, the smaller input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic block. Also present detailed energy-performance models of the adaptive feedback equalizer circuit. Proposed approach can reduce the normalized variation of the critical path delay while reducing the energy product at minimum energy supply voltage. This design will be implemented in the 8 bit Ladner Fischer adder and provide the efficient power reduction. The adaptive equalization circuits are design by Verilog HDL and simulated by Modelsim. Area and power will synthesized by Xilinx tool.

Index Terms: Feedback equalizer, leakage energy component, subthreshold, parallel prefix adder, Ladner Fischer adder.

I. INTRODUCTION

The use of sub threshold digital CMOS logic circuits is becoming increasingly popular in energy-constrained applications where high performance is not required. The main idea here is that scaling down the supply voltage can significantly reduces the dynamic energy consumed by digital circuits. Scaling the supply voltage also lowers down the leakage current due to reduction in the drain-induced barrier lowering (DIBL) effect. However, as the supply voltage is scaled below the threshold voltage of the transistors, the propagation delay of the logic gates increases, which in turn increases the leakage energy of the transistors. These two opposite trends in the leakage and the dynamic energy components lead to a minimum energy supply voltage that occurs below the threshold voltage of the transistors for digital logic circuits. However, digital logic circuits operating in the sub threshold region suffer from process variations that directly affect the threshold voltage. This in turn has a significant impact on the drive current due to the exponential relationship between the drive current and the threshold voltage of the transistors in the sub threshold regime.

Moreover, sub threshold digital circuits suffer from the degraded ION/IOFF ratios resulting in a failure in providing rail-to-rail output swings when restricted by aggressive timing constraints. These degraded ION/IOFF ratios and process-related variations make sub threshold circuits highly susceptible to timing errors that can further lead to complete system failures. Since the standard deviation of VT varies inversely with the square root of the channel area one approach to overcome the process variation is to upsize the transistors alternately, one can increase the logic path depth to leverage the statistical averaging of the delay across gates to overcome process variations. These approaches, however, increase the transistor parasitic, which in turn increases the energy consumption.

In this paper, we first propose the use of a feedback equalizer circuit for lowering the energy consumption of digital logic operating in the sub threshold region while achieving robustness equivalent to that provided Here, the feedback equalizer circuit (placed just before the flip-flop) adjusts the switching threshold of its inverter based on the output of the flip-flop in the previous cycle to reduce the charging/discharging time of the flip-flop's input capacitance. Moreover, the smaller input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic block. Overall, this reduces the total delay of the sequential logic, which makes it more robust to timing errors and allows aggressive clocking to reduce the dominant leakage energy.

In addition to reducing energy consumption, we also demonstrate how the tuning capability of the equalizer can be used to enable extra charging/ discharging paths for the flip-flop input capacitance after fabrication to mitigate timing errors resulting from worse than expected process variations in the sub threshold digital logic. In general, our approach of

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using feedback equalizer to lower energy consumption and improve robustness is independent of the methodology used for designing a combinational logic block operating in the sub threshold regime. We propose using an adaptive feedback equalizer circuit in the design of tunable sub threshold digital logic circuits. This adaptive feedback equalizer circuit can reduce energy consumption and improve performance of the sub threshold digital logic circuits. At the same time, feedback equalizer circuit enables post fabrication tuning of the digital logic block to overcome worse than expected process variations as well as lower energy and improve performance. Expected process variations, we show that the tuning capability of the equalizer circuit can be used post fabrication to reduce the normalized variation ($3\sigma/\mu$) of the critical path delay with minimal increase in energy.

II.CONSIDEEDR SCENERIO

A.ADAPTIVE EQUALIZER CIRCUIT OF ADAPTIVE EQUALIZATIO WITH MULTIPLE FEEDBACKS (AEMF)

Several techniques have been used to design robust ultralow power sub threshold circuits. Transistor upsizing and increasing the logic path depth can be used to overcome process variations. The use of gates of different drive strengths has also been proposed to overcome process variations. This method based on the two feedback path used to reduce the power and area of the circuits. In Existing system propose using joint equalization and coding to improve on-chip communication speeds by signaling at rates beyond the rate governed by resistance–capacitance (RC) delay in interconnects.

Operating beyond the RC limit introduces inter-symbol interference (ISI). We mitigate the effects of ISI by employing equalization. The existing equalizer employs a variable threshold inverter whose switching threshold is modified as a function of past output of the bus. In fig.1 the Adaptive feedback equalizer circuit has the two different feedback path in sub threshold regime shows the adaptive feedback equalizer with variable threshold invertors. The use of variable threshold inverter using adaptive feedback equalizer along with the classic master–slave positive edge-triggered flip-flop to design an adaptive E-flip-flop. This adaptive feedback equalizer circuit consists of two feed forward transistors (M1 and M2)and four control transistors (M3 and M4 for feedback path 1 that is always ON and M5 and M6 for feedback path 2 that can be conditionally switched ON post fabrication that provide extra pull-up/pull-down paths in addition to the pull-up/pull-down path in the static inverter for the Data Flip- Flop input capacitance. The extra pull-up/pull-down paths are enabled whenever the output of the critical path in the combinational logic changes. The control transistors M5 and M6 are enable /disable through transistor switches (M7 and M8) that are controlled by an asynchronous control latch. The value of the static control latch is initially reset to 0 during chip boot up.

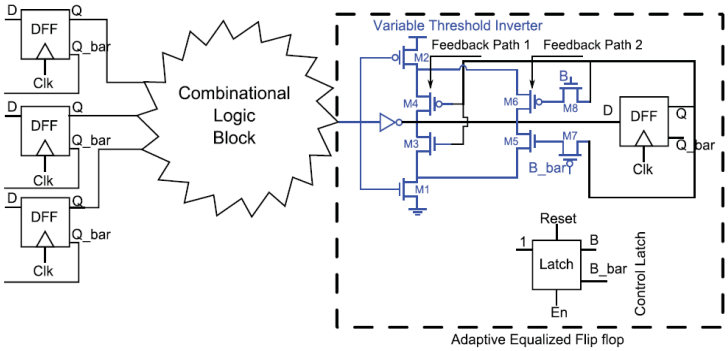

Figure: 1Adaptive feedback equalizer circuit with multiple feedback paths (designed using variable threshold invertors)

After boot up, if required a square pulse is sent tithe En terminal to set the output of the latch to 1 to switch ONM7 and M8, which enables feedback path 2.The adaptive E-flip-flop effectively modifies the switching threshold of the static inverter in the feedback equalizer based on the output of flip-flop in the previous cycle. The previous output of the flip-flop is a 0; the switching threshold of the static inverter is lowered, which speeds up the transition of the flip-flop input from 0 to 1. Similarly if the previous output is 1, the switching threshold is increased, which speeds up the transition to 0.Effectively, the circuit adjusts the switching threshold and facilitates faster high-to-low and low-to-high transitions of the flip-flop input. Moreover, the smaller input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic block.

III.PROPOSED METHOD

A.EQUALIZED DESIGN WITH SINGLE FEEDBACK PATH ON

Single fee back path equalized design provide the better performance and more efficient to power consumption. It consists of two PMOS and 2 NMOS. Using a minimum sized inverter instead of an upsized inverter would further

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lower down the delay but has lower reliability with respect to the dominant process variation effects in subthreshold regime. Figure:2 shows the proposed Equalized design with single feedback path on it use a combination of minimum

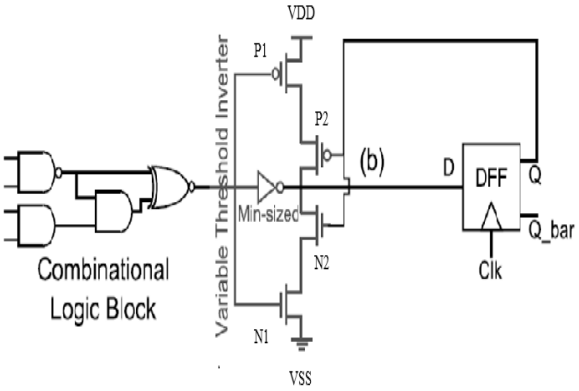

Figure: 2. Equalized design with single feedback path on sized inverter and feedback equalizer circuit along the critical path of the subthreshold logic. Minimum-sized inverter reduces the total delay and the feedback equalizer mitigates the effect of process variation.

B.OPERATION OF VARIABLE THRESHOLD INVERTER

1) First condition--Threshold voltage is vth^0. It is nominal threshold voltage of inverter.
2) Second condition--Pull down path is off and threshold voltage is increased to vth^+
3) Third condition-- Pull up path is off and threshold voltage is decreased to vth^-

C. PROPOSED ADDERS

Adaptive feedback equalization of single path has been implemented in 8 bit Ladner fisher adder It is one type of Parallel Prefix Adder

D.PARALLEL PREFIX ADDER

Parallel Prefix Adder (PPA) is very useful in today's world of technology because of its implementation in Very Large Scale Integration (VLSI) chips. The VLSI chips rely heavily on fast and reliable arithmetic computation. These contributions can be provided by PPA. There are many types of PPA such as Brent Kung, Kogge Stone, Ladner Fisher, Hans Carlson and Knowles. For the purpose of this research, Ladner Fisher Fig. 8 shows the structured diagram of a PPA. PPA can be divided into three main parts, namely the pre-processing, carry graph and post-processing. The pre-processing part will generate the propagate (p) and generate (g) bits. The acquirement of the PPA carry bit is differentiates PPA from other type of adders. It is a parallel form of obtaining the carry bit that makes it performs addition arithmetic faster.

The parallel prefix adders are more flexible and are used to speed up the binary additions. Parallel prefix adders are obtained from Carry Look Ahead (CLA) structure. The production of the carriers the prefix adders can be designed in many different ways based on the different requirements. We use tree structure form to increase the speed of arithmetic operation. Parallel prefix adders are fastest adders and these are used for high performance arithmetic circuits in industries. The construction of parallel prefix adder involves three stages

1. Pre- processing stage
2. Carry generation network
3. Post processing

1. PREPROCESSING UNIT

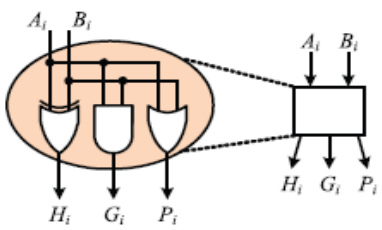

Figure: 3. Preprocessing unit

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The preprocessing stage computes the carry-generate bits Gi, the carry-propagate bits Pi, and the half-sum bits Hi, for every i,0 ≤ i ≤ n-1. Where . , +, and ⊕ denote logical AND, OR, and exclusive-OR, respectively.

Carry generation bits => Gi = Ai. Bi

Carry propagate bits => Pi = Ai + Bi

Half sum bits => Hi = Ai ⊕ Bi

2. CARRY GENERATION NETWORK

In this stage we compute carries corresponding to each bit .Execution of these operations is carried out in parallel .After the computation of carries in parallel they are segmented into smaller pieces. It uses carry propagate and generate as intermediate signals which are given by the logic equation:

CP

i:j=Pi:k+1 and Pk:j

CG

i:j=Gi:k+1 or (Pi:k+1 and Gk:j)

CP0=Pi and Pj

CG0= (Pi and Gj) or Gi

3. POST PROCESSING UNIT

This is the final step to compute the summation of input bits. It is common for all adders and the sum bits are computed by logic equation.

Ci-1=(Pi and Cin) or Gi

Si=Pi xor Ci-1

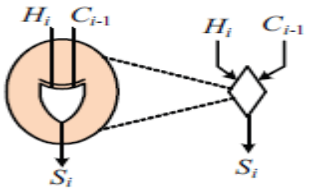

Figure: 4.Post processing unit

E. AESF IMPLEMENTED IN 8BIT LADNER-FISCHER ADDER

Proposed method of adaptive feedback equalization with single feedback is implemented in 8bit ladner- fischer adder. It is a parallel prefix form carry look-ahead adder. A parallel prefix adder can be represented as a parallel prefix graph consisting of carry operator nodes. The time required to generate carry signals in this prefix adder is o(log n). It is a fastest adder design and common design for high performance adders in industry. The Ladner-Fischer adder concept was developed by R. Ladner and M. Fischer, which they published in 1980. The better performances of Ladner-Fischer adder are minimum logic depth and bounded fan-out. But it has large area. Thus the adaptive equalization with single feedback has inserted into the buffer. It reduces the total delay and power consumption compare to the normal Ladner-Fischer adder and it provide more efficient output. Figure 5 shows the 8 bit ladner Fischer adder

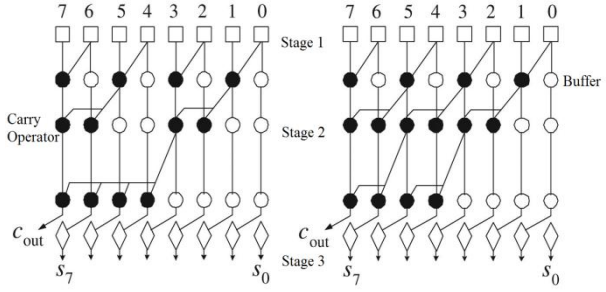

Figure: 5. Proposed AESF implemented in Lander Fischer Adder

IV.SIMULATION RESULTS

A.OUTPUTWAVEFORM OF AESF

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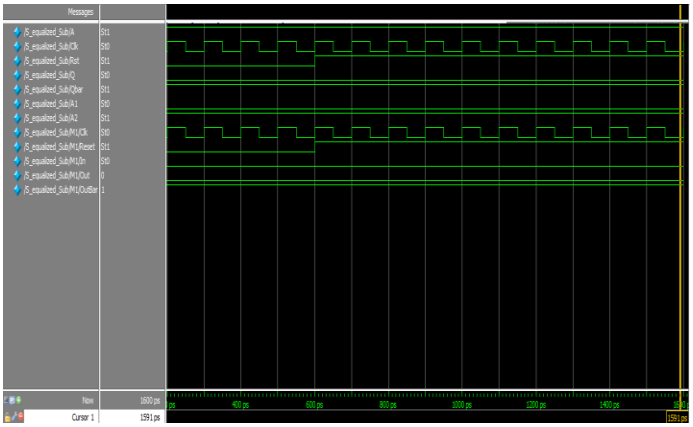

Figure: 6.Proposed AESF

B.OUTPUT WAVEFORM OF AESF IMPLEMENTATION IN 8 BIT LADNER FISCHER ADDER

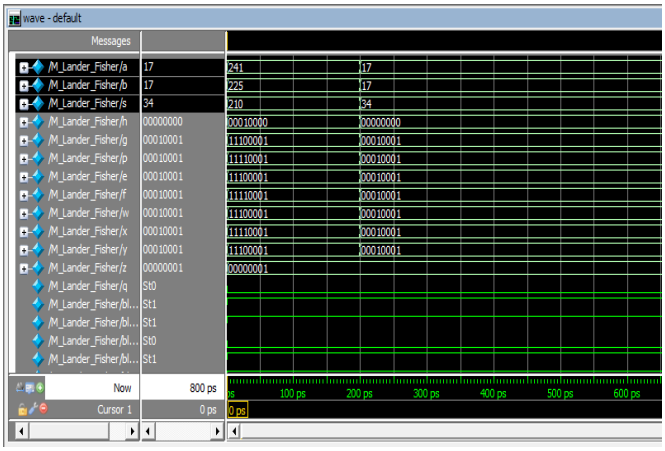

Figure: 7.AESF in 8 bit Ladner Fischer adder

V. COMPARISION RESULTS

A.POWER CALCULATION OF AEMF AND AESF

Table: 1. Power calculations of AEMF and AESF

Method name	Power		
	Voltage	Current	Total Power
Existing method of AEMF	475mW	190.00mA	729mW
Proposed method of AESF		59.38mA	391mW

B.POWER AND AREA CALCULATION OF IMPLEMENTATION OF 8 BIT LADNER FISCHER ADDERS

Table: 2.Power and Area comparisons of FIR filter

Method Name		LF adder based on Existing Equalized Flip Flop	LF adder based on Proposed Equalized Flip Flop
Area	LUT	22	14
	Slices	18	9
	Gate	1,248	1,152
Power	Voltage	4512.50mW	3800.00mW
	Current	1805.00mA	1520.00mA
	Total Power	6269.35mW	4608.17mW

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VI.CONCLUSION

The proposed application of tunable adaptive feedback equalizer circuit used to reduce the normalized variation of total delay along the critical path and the dominant leakage energy of the digital CMOS logic operating in the sub threshold regime. Adjusting the switching thresholds of the flip-flop based on the gate output in the previous cycle, the adaptive feedback equalizer circuit enables a faster switching of the gate outputs and provides the opportunity to reduce the leakage energy of digital logic in weak inversion region. Tuning capability of the equalizer circuit with single path can be used the power of 391mW and multiple paths used the power of 729mW. This design will be Implemented in 8 bit Ladner Fischer adde to provide the minimum logical depth..

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