IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 5, May 2017

Designing Low Dropout Regulator for Power Efficiency

C. Saranya[1], B.S. Aswathy[2]

PG Scholar, Dr. Sivanthi Aditanar College of Engineering, Tiruchendur, India[1]

Assistant Professor, Dr. Sivanthi Aditanar College of Engineering, Tiruchendur, India[2]

Abstract: Power efficient can empower an abiding operation in Very Large Scale Integration digital circuits. This design recommends a small potential loss and output voltage drop is competent by using Low Dropout Voltage Regulator (LDO). Low Dropout Voltage Regulator can act with a very poor Input–Output Differential Voltage. In battery regulated weightless device like Lithium Ion which need high rigor consistent tension mode and fast constant current process among absence of memory effect action in depressed quitter Regulators. This LDO consists of a floating-gate nMOS pass transistor, an attentively based error amplifier, and capacitive course for voltage reference generation along with feedback sensing. The power is the major parameter to be compared to various circuits between LDO and Li-Ion battery LDO based charger design. The LDO architecture results obtained from Tanner 16.3 software. The paper shows the completion inquiry of expected Li-Ion battery in LDO design are decisive in terms of cost function when compared to actual LDO arrangement of above perimeter.

Keywords: Low Dropout Voltage Regulator (LDO), Floating Gate Pass Transistor, Lithium-Ion Battery Charger, Band gap Reference circuit.

I. INTRODUCTION

Nowadays, LDO plays an expanding number of low voltage utilization, i.e., cellular phones, pagers, laptops, remote sensing appliances, etc. The low truant nature of the regulator makes it appropriate for use in many applications namely, automotive, portable, and industrial functions. This movable electronics market requires lowering voltage and below quiescent current flow as long as heightened array efficiency and longevity in drastic small capacity grasp front-end circuits. Conventionally multistage blunder amplifying gadget hold resorted to remarkable line and load regulation. Being fluctuating the influence quantity along with inferior pass filtering, a cascade NMOS transistor has the gate source service. It spends class-AB error amplifier, also preferencing effective reservoir ignition. To meet the effective mentioned requirements, several advanced techniques are volunteered as well as presented to design a high performance LDO with fast load transient response, high potential number rejection ratio, short inrush swinging, excellent payload arrangement together with precise over present preservation.

Bandwidth is another important specification in DC regulator pattern. Tremendous radio band again improves the power supply rejection ratio (PSRR) of the regulator, which is a measure of how well the regulator attenuates noise on the power supply. The better the power supply rejection, the less the yield electron changes in retort to inconstancy in the accumulation [3]. Therefore, articulate LDO have been determined toward flat product voltage stream with compressing sudden influence damage service in Lithium ion body charger.

This paper focuses on the design of proposed power efficient LDO based on that proposed Lithium array disk. Those PTAT and current alternator route code are constructed in Li-Ion occupying LDO technology and their specifications are compared to prove the productivity.

II. BACKGROUND

One of the upcoming and promising technologies that have many advantages over LDO is handy aligned Li-Ion chain charging. Advantages are high efficiency, high accuracy, low size area, and high importance. The sequence create including LDO is being researched and shows that they allow scaling up to nanometre dimensions.

A. Low Dropout Voltage Regulator

The A low-dropout switch (LDO) is suited of managing its specified profit service over a broad length of amount present also input ignition, down to a very cramped change among proposal and crop utility. This contrast is well-known as the nonconformist electron. A little truant voltage thermostat is given in Fig. 1. It consists of disparate factor like,

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 5, May 2017

1. Series Pass Transistor
2. Error Amplifier
3. Voltage Divider

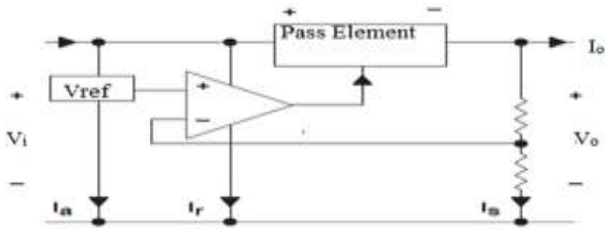

Fig 1 Low Dropout Voltage Regulator

The ongoing leakage is concluded in either NMOS or PMOS pass transistor. The switch is associated in series across gate to drain contact, where the gate is electrically isolated. The error amplifier working the gain signal and brings the unidirectional salient outflow in the inured differential input signal. The voltage divider undertaking the load resistor and lift the payload production in the appropriate profit current.

B. Conventional LDO Using Floating Gate NMOS Pass Transistor

The inflated gate obtaining yield capacitor limited LDO DC thermostat is recommended. The LDO recognize a below nonconformist electron of one V_{DSsat} as regular LDOs with NMOS pass transistors, but displayed good line regulation. An attentively biased class-AB error amplifier is approved to appreciate transient response with lesser quiescent current utilization.

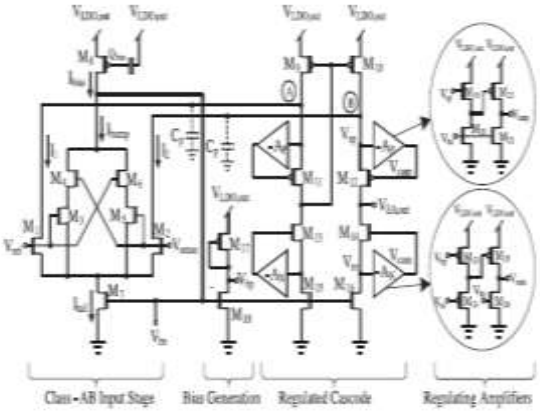

Fig. 2 Proposed Low Dropout Voltage Regulator

The transmission of the error amplifying device can be adjusted by programming charges on a floating-gate transistor without degrading route strength. To further boost power energy, the voltage source generation and gain voltage observation sensing are attained by capacity line beyond extra power expenditure. The LDO output voltage equivalent can hence be adjusted in continuum with low temperature variation to attain in saturation region.

C. Floating Gate

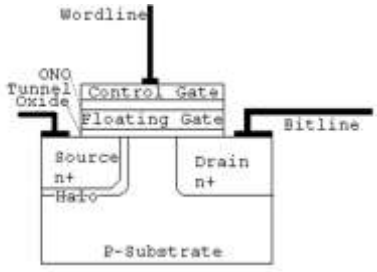

Fig. 3 Floating Gate

DOI 10.17148/IJIREEICE.2017.5525

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 5, May 2017

The floating gate is an electrically confined gate. It stores current from source to drain and the control signal is carried in the control line. The floating gate is effectively surrounded by a confinement layer. This implements the floating gate transistor to be used as non-volatile memory, but also imposes the need to find ways to charge or discharge it.

This assembled in the channel region between drain and sinks hot (fast) charge carriers that have abundant energy to pass the isolation region between the substrate and the floating gate. This compiles a charge on the floating gate. They have sufficiently high energy to escape through the surrounding layer.

D. Error Amplifier

An **error amplifier** is most generally encountered in feedback unidirectional voltage force circuits, where the sampled output voltage of the circuit under supervision, is fed back and correlated to a steady reference voltage.

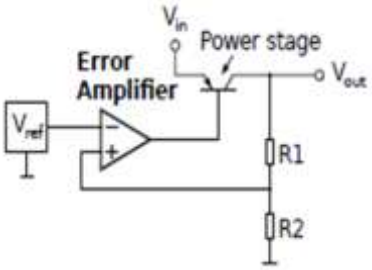

Fig. 4 Error Amplifier

Any distinction enclosed by the two generates a compensating error voltage which tends to move the output voltage towards the layout specification.

E. Class AB Input Stage

Class AB sacrifices some expertise over class B in favour of quantity, that is fewer productive (below 78.5% for full amplitude sine waves in transistor amplifiers, typically, much deficient is common in class-AB vacuum-tube amplifiers).

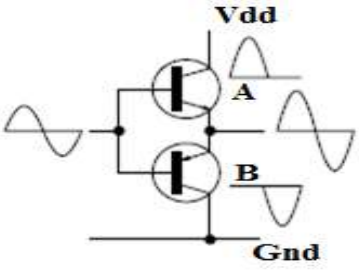

Fig. 5 Error Amplifier

F. Regulated Cascode Topology

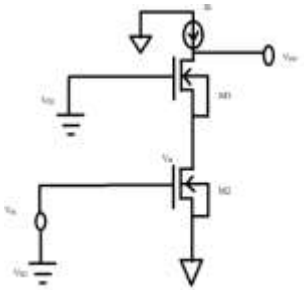

Fig. 6 Regulated Cascode Topology

The cascode is a two-stage amplifier that reposes of a common emitter stage feeding into a common base stage. Here, Cascoding is used for getting the signal intensifies in gate topography. It provides the information to the previous gain as third input.

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 5, May 2017

G. LDO Working Procedure

Table 1. LDO Working Procedure

CONDITION	SATURATION	LINEAR	CUTOFF
All transistor in sub threshold	M4 & M6 'ON'	M3 & M5 for amplifying	____
If reducing the class-AB input	M4,M6,M7 'ON'	Input voltage only engage in linear region	____
Explicit casting	Either M15,M16 'ON' or M9,M10 'ON'	_____	____
PMOS Cascoding	_____	_____	M11 & M12 'OFF'
NMOS Cascoding	M13 & M14 'ON'	_____	_____
When error amplifier are in ground contact	All transistors are 'ON' and get the voltage drop.	_____	_____

The table II shows the functioning action for Low Dropout Voltage Regulator.

H. Simulation

The Low Dropout Voltage Regulator (LDO) employing floating gate NMOS pass transistor can display preferencing in the voltage anticipating and obtain the low voltage drop. Hence, they produces decreasing power disappearance in the given input voltage unit. The implementation of Low Dropout Voltage Regulator (LDO) is simulated by using TANNER software.

III. EXISTING WORK

A. Schematic of Existing LDO Circuits

The actual Circuits are performed by LDO applying NMOS pass transistor. Some revaluation of power loss and low output voltage drop are managed. The LDO circuits are work out by testing tanner software.

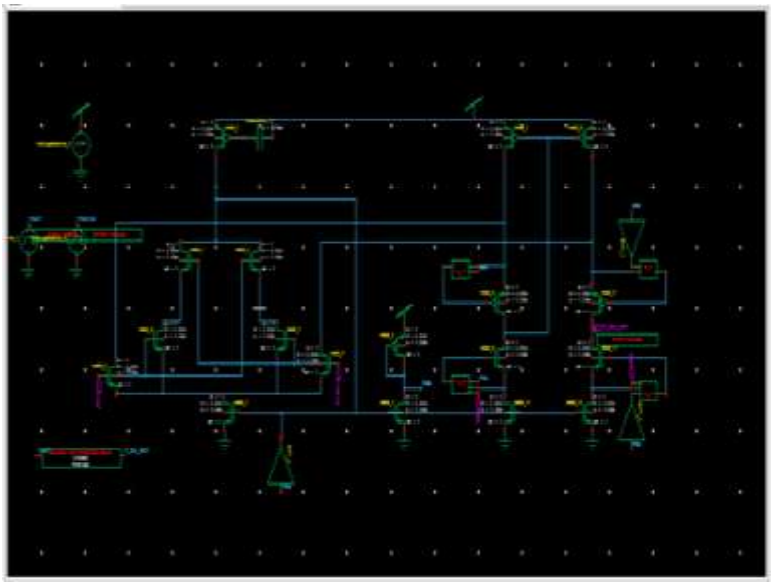

Fig 7.a) Schematic of LDO Using NMOS Pass Transistor

The above figure 7(a) display the schematic diagram for LDO proving floating gate pass transistor. It subsist of floating gate, NMOS pass transistor, class AB input stage, and regulated cascading for CMOS amplifier is done in the TANNER circuit. Now let's analyse the parameter setting for the required power loss.

B. Output For Existing LDO Using NMOS Pass Transistor

It arranged the input DC voltage as 2.7v and amplifier voltage as 2.5v. We earn the output voltage drop as 2.25v.

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 5, May 2017

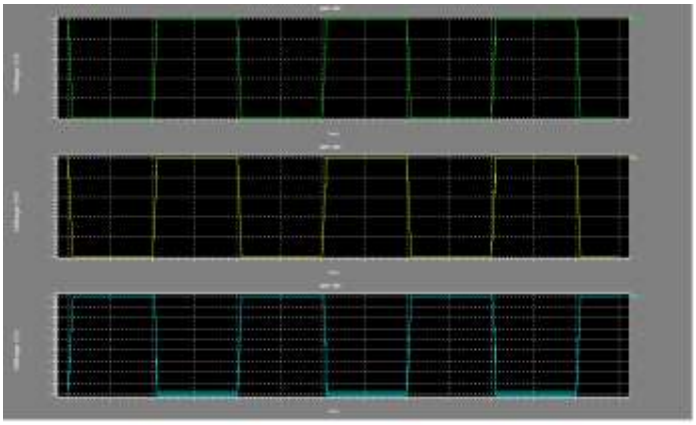

Fig 7.b) Output of LDO Using NMOS Pass Transistor

IV. PROPOSED WORK

A. Lithium Ion Battery Charger Circuit

In this planned work, efficient Li-Ion battery LDO positioned charger has been suggested with diminished voltage discharge and power fall although correlated to current scheme receive from some quotation [1], [7], [11], [12]. Li-Ion battery is strong fitted to compact voltaic builder such as cell phones, and PDAs [1]. It take up three mode domination like leak continual current, rapid stable current and regular voltage condition. It is the elemental as well as crucial element in overcharging conservation.

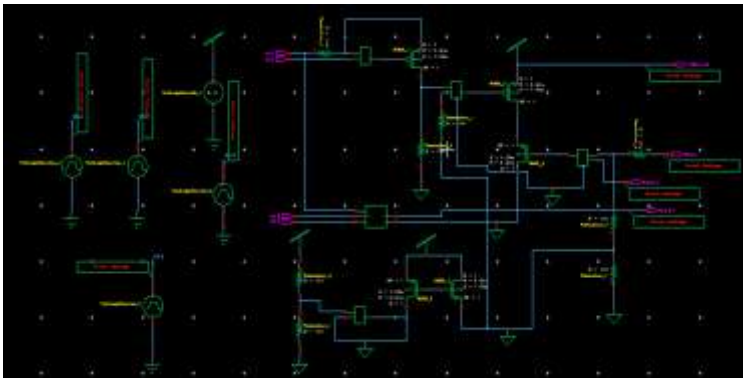

Fig 8 Schematic of Li-Ion Battery Charger

The array enables three aspects like, reconditioning, regulating current and consistent voltage. If the sequence voltage is down the inherent low-voltage threshold, the body is preconditioned with an evaluation current. The preconditioning point preserves the lithium-ion unit and underestimates heat distraction. The charge current is raise ascend, established on the cell DC, from the fall back current to the peak charge current settled by the sense resistor. This time is sustained as far as the batch grasps the charge-regulation voltage.

B. PTAT Circuit

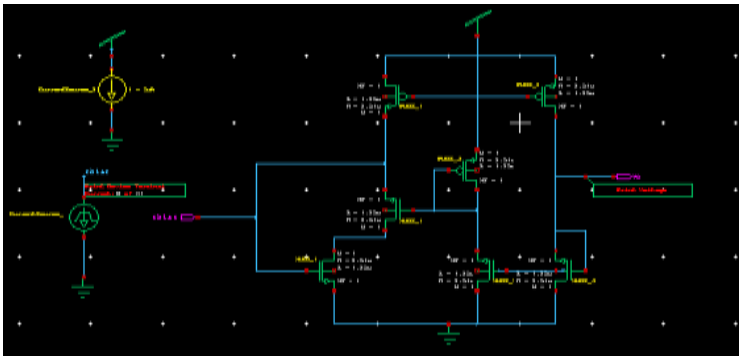

Fig 9 Schematic of PTAT Circuit

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 5, May 2017

The PTAT service generator is stationed on the MOS tension category, even reversal parallel and leaning prevailing alternator.

C. Current Generator Circuit

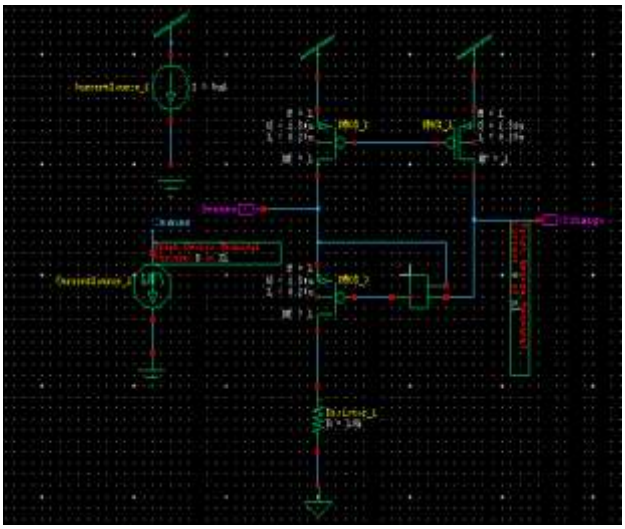

Fig 10 Schematic of Current Generator Circuit

To restraint the dribble in the quick current approach, the current dynamo limit is pre-owned.

D. Architecture Of Li-Ion Battery LDO Based Charger Circuit

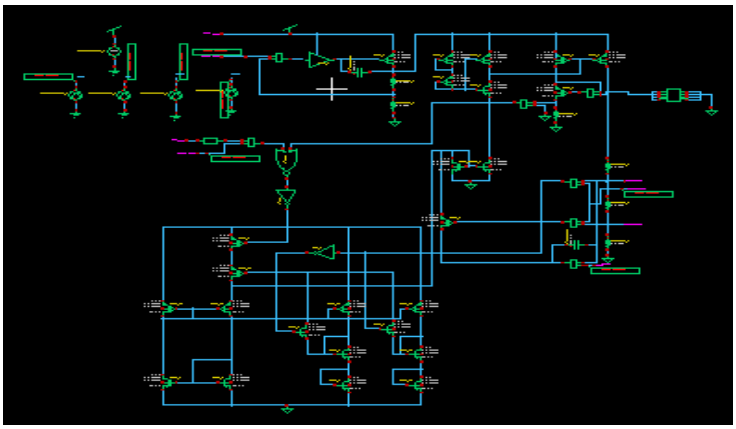

Fig 11 Schematic of Li-Ion Battery LDO Based Charger Circuit

In prior method, a transfer pressure is supported alongside LDO switch. The power transistor is recycled to shift in peculiar system. The current alternator fix up the plug current and they restrict the dribble charge. For developing the resource ignition stable, we use PTAT generator. The image is converted in op-amp for measuring the constriction in mentioned voltage levelled.

V. RESULTS AND DISCUSSIONS

A. Simulation Of Li-Ion Battery Charger Circuit

The simulation event received saved from the Tanner tool as specified prior. The suggested charger is performing not over creep regular current, rapid unbroken current and stabile spark mechanism. Thus, they resolve huge power energy. The output waveform for the Li-Ion battery charger is abated as exhibited in Fig 12.

The Fig. 12 shows the waveform for Li-Ion battery charger. Due to this they cut down the mortal issue of current and voltage charging.

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 5, May 2017

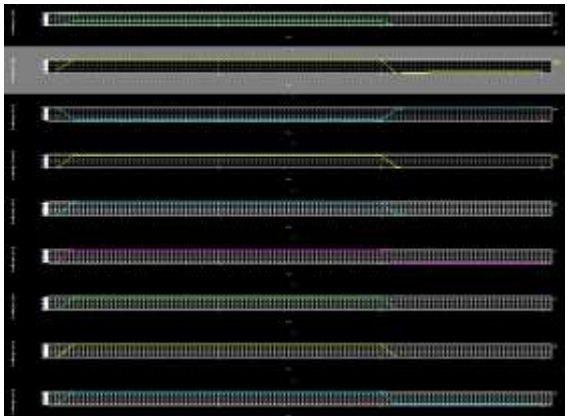

Fig. 12 Simulation Result for Li-Ion Battery Charger

B. Simulation For PTAT Circuit

Consider developing the voltage relating equivalent, the output waveform for the PTAT circuit is given in Fig. 13.

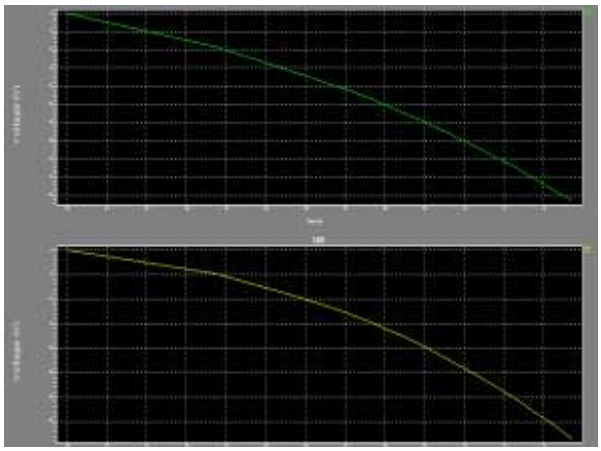

Fig. 13 Simulation Result for PTAT Circuit

The Fig. 13 shows the output waveform for the PTAT circuit. Here, the temperature amount weaken to 0ns. It bring the complete time period as 120ns.

C. Simulation Of Current Generator Circuit

To escape streaming in the rapid current technique, the output waveform for the current generator route is given in Fig.14.

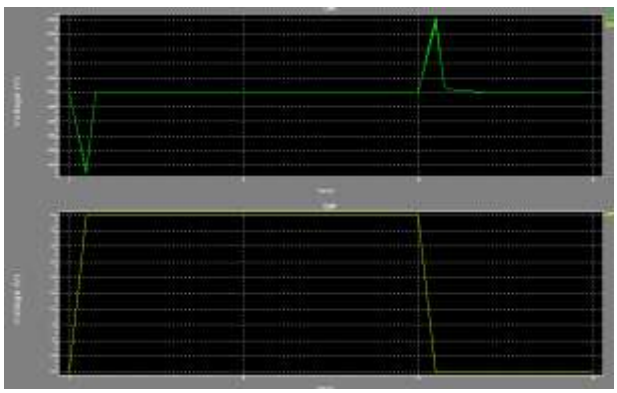

Fig. 14 Simulation Result for Current Generator Circuit

The Fig. 14 shows the waveform for current generator circuit. At the initial stage, it promotes some misinterpretation. Afterwards, it yields boosting of charging at 5V.

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 5, May 2017

D. Simulation of Proposed Architecture Of Li-Ion Battery LDO Based Charger Circuits

To charge the sequence in input supply, the LDO regulator can outgrowth power to battery charger as shown in Fig. 15.

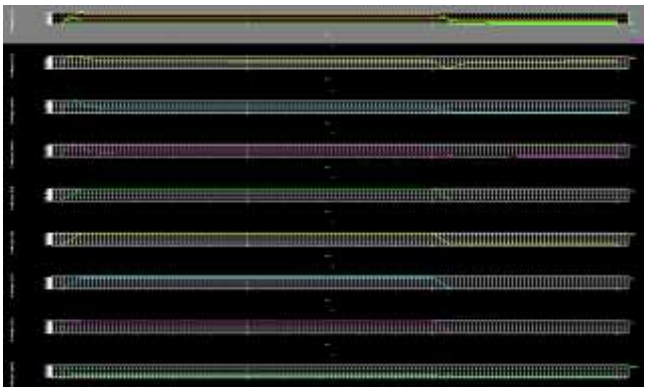

Fig. 15 Simulation Result for Proposed Architecture In LDO Based Li-Ion Battery Charger Circuit

The Fig. 15 shows the output waveform for the suggested architecture in LDO based Li-Ion battery charger circuit. Here, the supply input should be below 4.2V. Consequently, the output outturn as under 2.7V, although correlate to past process. Accordingly, it outcomes maximal potential productivity.

VI. COMPARISON

The expected LDO based Li-Ion battery charger have related with actual circuits in premise of output voltage drop including power.

Table 2. Comparison Of Existing And Proposed Method Of LDO

Circuit	Output voltage drop	Power consumption
LDO Using Floating Gate NMOS Pass Transistor	2.25V	0.4443W
Proposed LDO Based Li-Ion Battery Charger	200mV	0.0647W

The Table 2 programs similarity table for conventional LDO, expected LDO based Li-Ion battery charging capability.

VII. CONCLUSION

The constructed effort placed on LDO has large scope of employment in Li-Ion battery charging. The Tanner tool is used for utilization and reproduction of LDO occupying Li-Ion battery charging circuits. In this paper, advanced construction for LDO with Li-Ion charging is recommended. The prospective circuits are exceedingly powerful in charge of output voltage drop, and weaken power loss. These prospective circuits are correlated with actual circuits and their observation is tabled. The comparison shows that proposed circuits are efficient and the power can be reduced more than 75% in LDO based Li-Ion charging.

REFERENCES

[1] J. Buxton, "Li-ion battery charging requires accurate voltage Sensing," Analog Dialogue: Analog Devices, vol. 31, no. 2, pp. 3-4, 1997.
[2] D. Linden and T. B. Reddy, Handbook of Batteries, chapter 35, McGraw-Hill, New York, NY, USA, 2002.
[3] S. Dearborn, "Charging Li-ion batteries for maximum run times," Power Electronics Technology, vol. 31, no. 4, pp. 40–49, 2005.
[4] M. Chen and G. A. Rinc´on-Mora, "Accurate, compact, and Power-efficient li-ion battery charger circuit," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 53, no. 11, pp. 1180– 1184, 2006.
[5] P. Li and R. Bashirullah, "A wireless power interface for rechargeable battery operated medical implants," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 54, no. 10, pp. 912–916, 2007.
[6] J.-J. Chen, F.-C. Yang, C.-C. Lai, Y.-S. Hwang, and R.-G. Lee, "A High efficiency multimode Li-Ion battery charger with variable current source and controlling previous-stage supply voltage," IEEE Transactions on Industrial Electronics, vol. 56, no. 7, pp. 2469–2478, 2009.
[7] A. Dey and T. K. Bhattacharyya, "Design of a CMOS band gap reference with low temperature coefficient and high power supply rejection performance," International Journal of VLSI Design & Communication Systems, vol. 2, no. 3, pp. 139–150, 2011.
[8] S.-H. Yang, J.-W. Liu, and C.-C.Wang, "A single-chip 60-V bulk charger for series Li-ion batteries with smooth charge-mode transition," IEEE Transactions on Circuits and Systems. I. Regular Papers, vol. 59, no. 7, pp. 1588–1597, 2012.
[9] S. S. Bethi, K.-S. Lee, R. Veillette, J. Carletta, and M.Willett, "A Temperature and process insensitive CMOS reference current generator," in Proceedings of the IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS '13), pp. 301–304, 2013.
[10] P. H. V. Quang, T. T. Ha, and J.-W. Lee, "A fully integrated multimode wireless power charger IC with adaptive supply control and built-in resistance compensation," IEEE Transactions on Industrial Electronics, vol. 62, no. 2, pp. 1251–1261, 2015.