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Design of Efficient Novel XOR and a Code Converter using QCA with Minimum Number of Cells

P. Vijayalakshmi[1], V. Monisha[2]

PG Scholar, Dr. Sivanthi Aditanar College of Engineering, Tiruchendur, India[1]

Assistant Professor, Dr. Sivanthi Aditanar College of Engineering, Tiruchendur, India[2]

Abstract: Quantum-dot Cellular Automata (QCA) is a developing implementation technology for the development of low power, low area, and highly efficient digital circuits. QCA is an alternative technology to Complementary Metal Oxide Semiconductor (CMOS) because CMOS has scaling limitations which leads to high leakage power. QCA is a transistor less implementation model. To date, the cost function is a more important parameter to be compared to various circuits within QCA design. Such cost function includes delay, the number of QCA majority gates and types of crossovers used. The area is the major parameter to be compared to various circuits between CMOS and QCA design. In this paper, new XOR and Binary to Gray code converter are proposed. The proposed circuits are designed in both CMOS and QCA technologies. The CMOS technology results obtained from Tanner 16.3 software and QCA results obtained from QCA Designer tool. The paper shows the performance analysis of proposed XOR and Binary to Gray code converter are efficient in terms of cost function when compared to existing QCA designs of above circuits. Also the analysis shows that above QCA designed circuits are efficient in terms of the area when compared to CMOS technology.

Keywords: Quantum-Dot Cellular Automata (QCA), Majority Voter, XOR, Code Converter, Cost Function.

I. INTRODUCTION

Integrated Circuits are mainly based on Complementary Metal Oxide Semiconductor (CMOS) technology. Nowadays integrated circuit technology has been improving so that the dimensions of the devices are varying which results in the reduction in size. Due to this improvement, the dimensions of the devices are reducing continuously which leads to scaling limitations. Scaling limitations includes second order effects like short channel effects, impact ionization, hot carrier effects, Velocity Saturation effect etc.., so new technology which is Quantum-Dot Cellular Automata (QCA) has been arrived to overcome above scaling limitations. QCA is an alternative technology to CMOS which is a transistor less implementation model.

QCA deals with only electrons and their positions which lead to easy implementation. The basic element of QCA is a QCA cell that consists of four electrons. The position of electrons represents the bit either binary 0 or 1. The key process is the interaction between the cells by means columbic force.

This paper focuses on the design of proposed efficient QCA based XOR and binary to gray code converter based on that proposed XOR. Those XOR and code converter are designed QCA technology and their parameters are compared to prove the efficiency.

II. BACKGROUND

One of the upcoming and promising technologies that have many advantages over CMOS is Quantum Dot Cellular Automata (QCA). Advantages are low power dissipation, less area, and high speed. Logic design with QCA is being researched and shows that they allow scaling up to nanometre dimensions.

A. QCA Cell

The basic element of QCA is QCA cell which consists of two electrons. Each electron is located at the diagonal corners of the cell as shown in Fig 1. Those electrons are tunnel through barrier to occupy various diagonal positions. The tunnelling is due to the electrostatic force of repulsion. The position of cells determine the polarization of cells as P= -1 and P= +1 where -1 indicates logic 0 and +1 indicates logic 1. The working principle of QCA Cell and their polarizations are obtained from [17], [18]. Figure 2 shows the QCA cells of various arrangements includes Null cells, binary logic ‘0’ and binary logic ‘1’.

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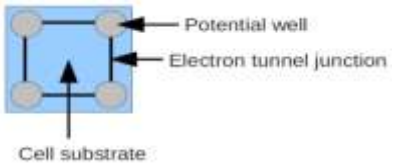
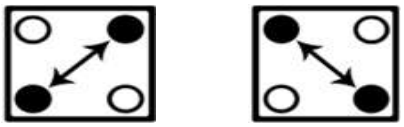


Fig 1. QCA Cell



Polarity P=+1 Polarity P=-1

Fig 2. QCA Cell arrangements

B. QCA Wire

QCA wire is to propagate the binary signal from input to output cell by means of electrostatic interactions between the cells. The propagation may through both 90^o and 45^o wires as shown in Fig 3 and Fig 4.

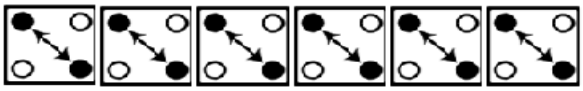


Fig 3. Binary Wire

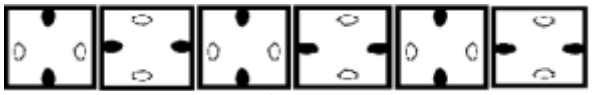


Fig 4. 45^o Binary Wire

Assume that the cell at left side is input cell and cell at right side is output cell. The columbic interaction which is the electronic repulsion from neighbouring cell determines the position of electrons in normal cell [2].

C. QCA Inverter

QCA cells can be arranged to form various logic gates. One of the basic logic gates of QCA technology is inverter which is formed by connecting the corners of two QCA cells as shown in Fig 5(a) and Fig 5(b).

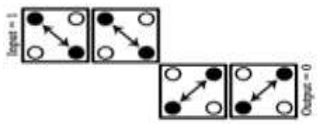


Fig 5. a) QCA Inverter

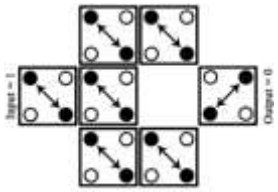


Fig 5. b) QCA Robust Inverter

QCA inverter can use either one clock cycle or more than one clock cycle. Fig 5(a) inverter use one clock cycle. Fig 5(b) inverter use one clock cycle for input wire and another clock cycle for output wire [10].

D. QCA Majority Gate

Another major logic gate of QCA is Majority gate. It performs three input logic function. Consider the inputs of majority gate as A, B and C, then its logic function is

M (A, B, C) = AB+BC+CA

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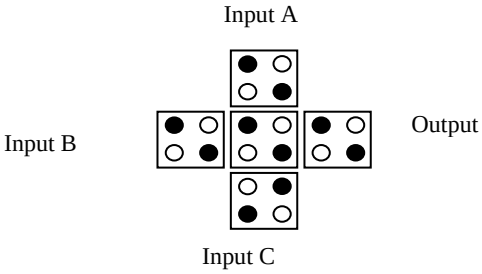

Fig 6. Majority Gate

By setting any one of the input of majority gate as either logic '1' or logic '0' we can obtain logic gate OR and AND gate as shown in Fig 7(a) and Fig 7(b).

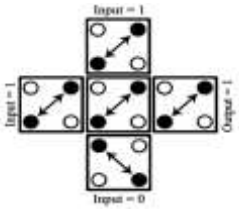

Fig 7. a) AND Gate

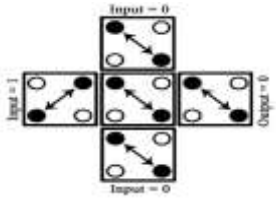

Fig 7. b) OR Gate

E. QCA Clock

In general power is the need to change the state of the cell. In QCA, clock acts as the power to make tunnelling of electrons to obtain logic '0' and logic '1'. QCA consists of four clock zones and each clock zone has four phases as Switch, Hold, Relax and Release as shown in Fig 8. Each clock phase has 90^{o} phase shift from previous phase. In the Switch phase, the tunnelling barriers in a zone are raised. While this occurs, the electrons within the cell can be influenced by the Columbic charges of neighbouring zones. Zones in the Hold phase have a high tunnelling barrier and will not change state, but an influence other adjacent zones. Lastly, the Release and Relax decrease the tunnelling barrier so that the zone will not influence other zones [4].

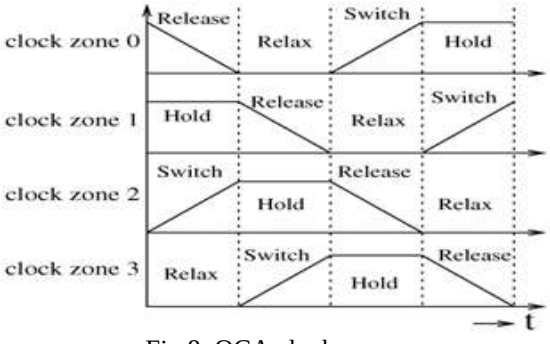

Fig 8. QCA clock zones

F. Wire Crossover

The collection of two intersecting QCA wires is known as a crossover. There are several types that include Multilayer approach, coplanar approach, Multiphase Clocking scheme, Ternary cell approach. Based on the type of crossover used, cost function of the design may vary [18].

G. Simulation

Simulation of QCA design is done using QCA Designer tool. This tool used to do user defined or custom layout and

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also to verify the functionality or logic of the design by simulation. It consists of two simulation engines as the bistable approximation and a coherence vector [5], [16].

III. EXISTING WORK

A. Schematic of Existing CMOS Circuits

The Existing Circuits are designed using CMOS technology which consists of large number of transistors. By reducing the channel length to improve the efficiency, it leads to scaling effects which includes second order effects. CMOS circuits such as EX-OR and Binary to gray code converter circuits are designed using tanner software.

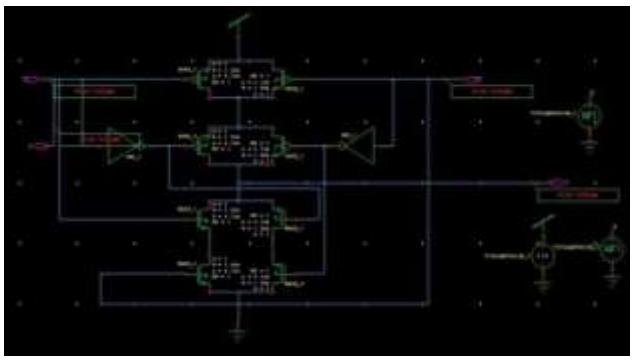

Fig 9.a) Schematic of CMOS EX-OR

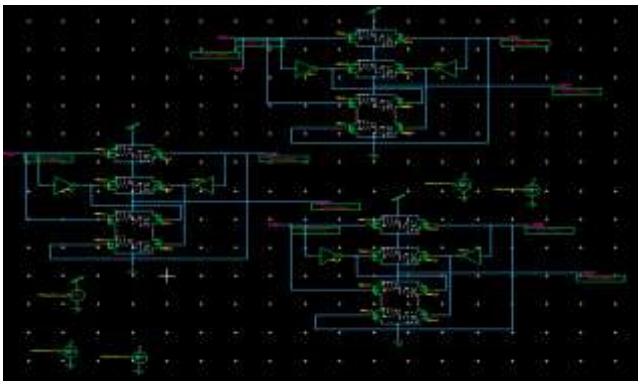

Fig.9 b) Schematic of CMOS Binary to Gray Code Converter

Fig 9 Shows the schematic of CMOS circuit that occupies more area.

B. Layout of Existing QCA Circuits

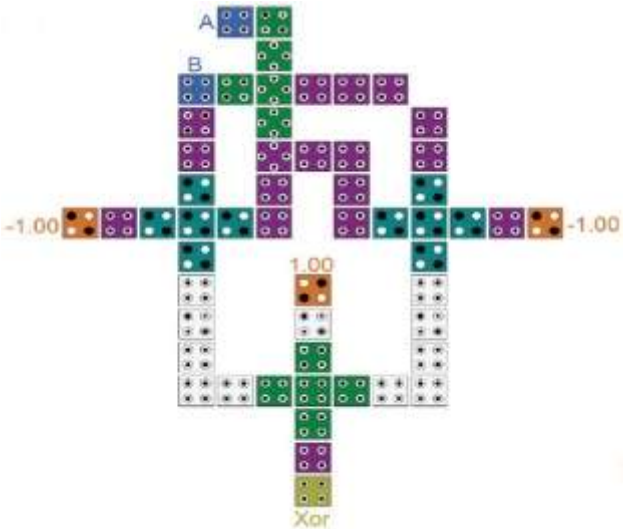

Fig 10. a)Existing EX-OR

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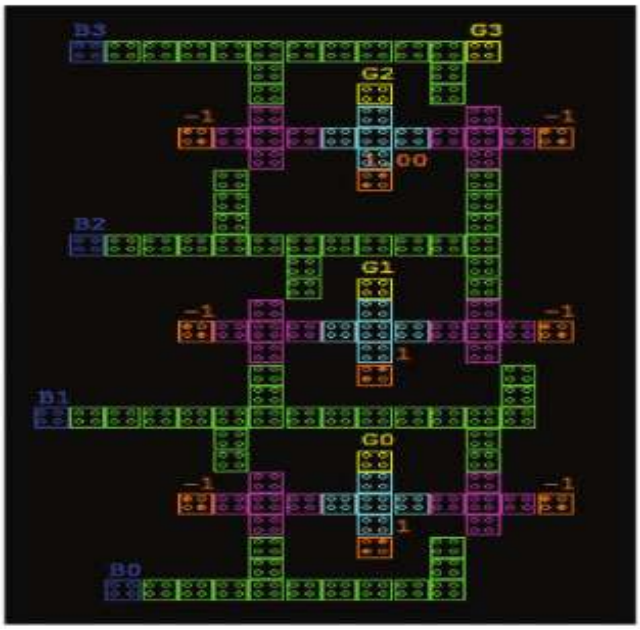

Fig 10. b)Existing Binary to Gray code converter

IV. PROPOSED WORK

A. Layout of Proposed Circuits

In this proposed work, efficient XOR and binary to gray code converter has been proposed with reduced number of cells when compared to conventional designs obtained from some references [1], [7], [11], [12]. XOR is the basic and essential element in most of the digital logic designs. So, many designs of XOR are proposed so far.

In former designs, XOR logic is designed with 3-input majority gate, but in the proposed they are not based on majority gates. Figure 9(a) shows the layout of proposed XOR.

Y=A XOR B

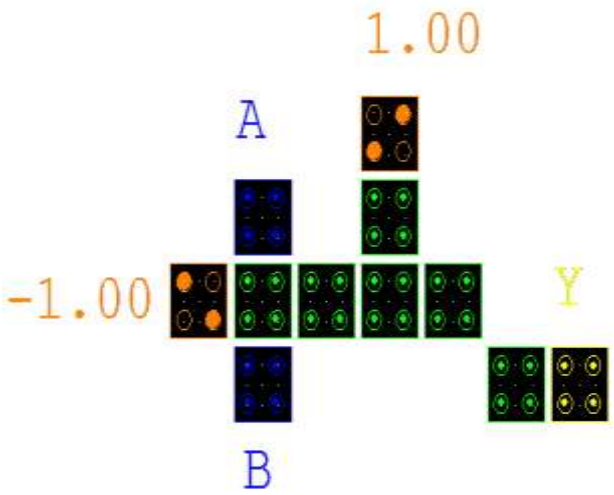

Fig .11 a) Layout of Proposed XOR

The proposed XOR consists of only one majority gate which results in reduced number of cells. Similarly with the help of proposed XOR, code converters can be designed because XOR is the basic element of all code converters. Code converters are to convert one form of code to another form to make the implementation easy. In this paper, binary to gray code converter is designed in QCA with reduced number of cells. The layout of Proposed Binary to gray code converter is shown in Fig 11 (b).

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Z = A
Y= A XOR B
X= B XOR C
W= C XOR D

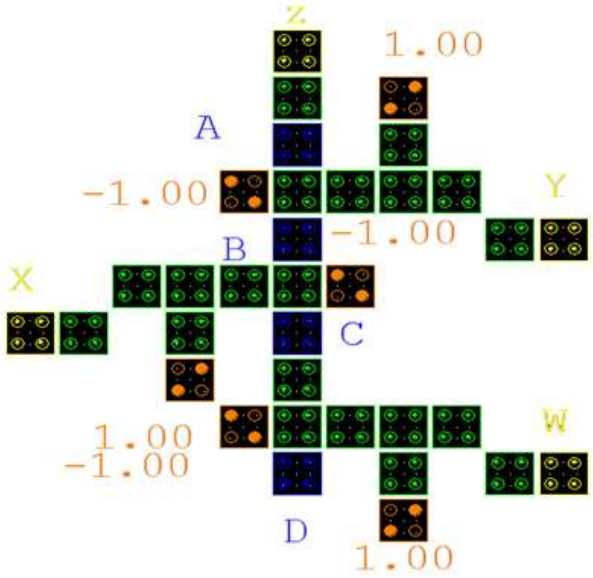

Fig.11 b) Layout of Proposed Binary to Gray code converters

V. RESULTS AND DISCUSSIONS

A. Simulation of Proposed Circuits

The simulation result obtained from the QCADesigner tool as mentioned earlier. The simulation result is similar to the result obtained from truth table which shows the logic function of the logic gate. The output for proposed XOR gate is obtained at ¼ th clock cycle. The input is given at clock 0 and the output is obtained at same clock 0 which results in low delay value. The output waveform is obtained as shown in Fig 12(a).

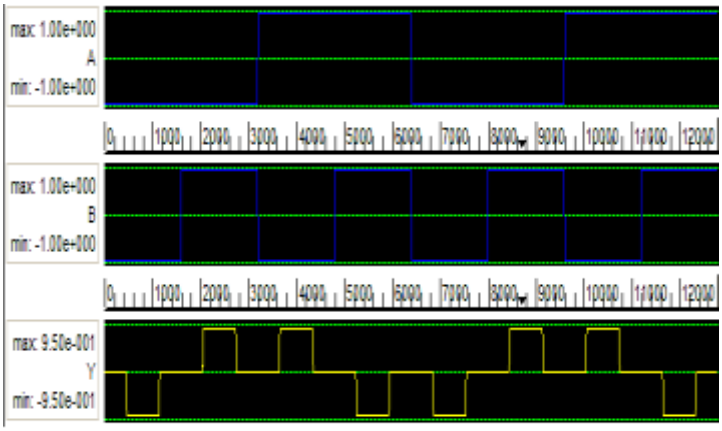

Fig.12 a) Simulation Result for XOR gate

Fig 12(a) shows the waveform for proposed XOR gate which produce logic 1 when two inputs A and B are different, produce logic 0 when both inputs are same.

Similarly Binary to Gray code converter output is obtained at 1/4th clock cycle. The input is applied at clock 0 and output is obtained at same clock 0 phase. The output waveform is obtained as shown in Fig 12(b).

Fig 12(b) shows the waveform for proposed Binary to gray code converter which produce gray code for given binary values. The basic logic element used in this converter is XOR gate.

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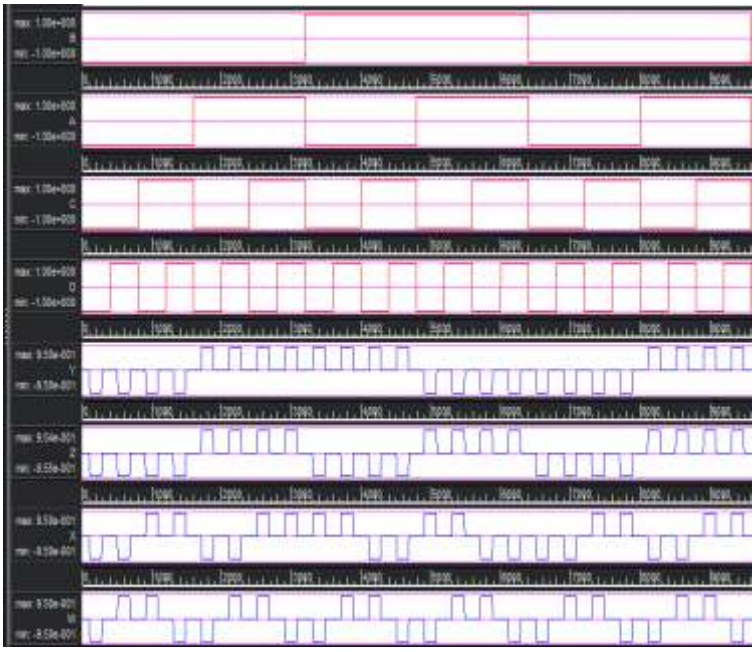

Fig.12 b)Simulation Result for Binary to Gray code converter

VI. COMPARISON

The proposed XOR and Binary to Gray code converter layout have compared with conventional circuits in terms of cell area, number of cells, number of majority voters and delay. Table 1 shows the comparison table for XOR designs that shows the comparison of conventional and proposed XOR design's efficiency. Table 2 shows the comparison table for Binary to Gray code converters that shows comparison result among various binary to gray code converters obtained from references [1],[7],[11],[12],[13].

Table 1. Comparison of XOR Designs

CIRCUIT	AREA (μm^2)	CELL COUNT	CLOCK)	CROSS-OVER
XOR [6]	0.09	60	1.5	Coplanar
XOR [10]	0.08	54	1.5	Coplanar
XOR [11]	0.06	67	1.25	Coplanar
XOR [8]	0.08	87	1	-
XOR [7]	0.03	36	0.75	-
XOR [1]	0.03	29	0.75	Not Required
PROPOSED XOR	0.01	11	0.25	Not Required

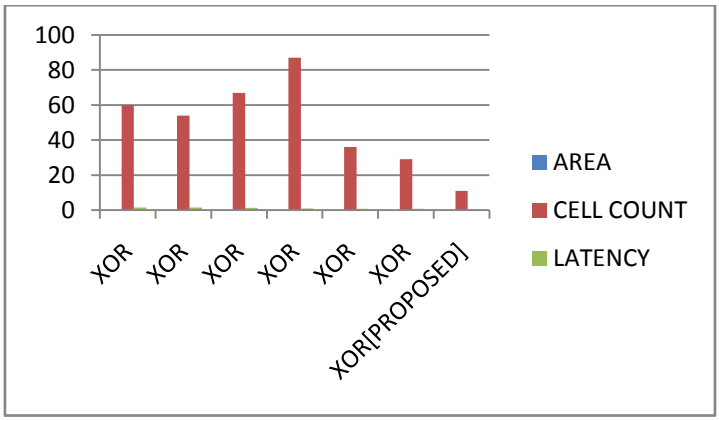

Fig.13 a) Comparison Chart for XOR

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Table 2. Comparison of 4-bit binary to gray code converter

CIRCUIT	AREA (μm^2)	CELL COUNT	LATENCY (CLOCK)
BINARY TO GRAY CODE [13]	0.18	131	0.75
BINARY TO GRAY CODE [3]	0.63	389	8
BINARY TO GRAY CODE [7]	0.14	133	0.75
PROPOSED BINARY TO GRAY CODE	0.06	34	0.25

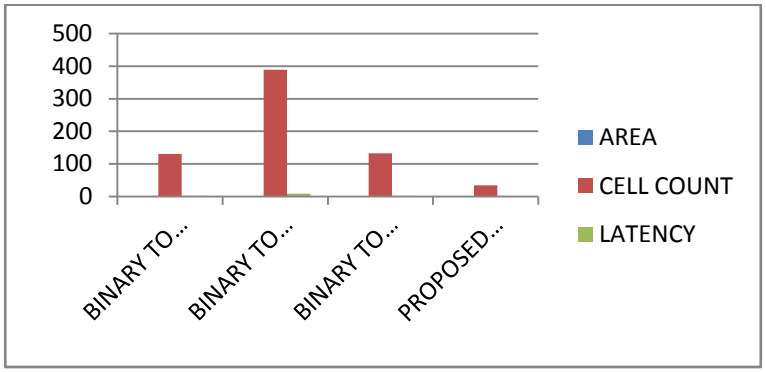

Fig. 13 b) Comparison chart for code converter

VII. CONCLUSION

The designed work based on QCA has wide range of applications in digital circuits. QCADesigner tool is used for implementation and simulation of QCA circuits. In this paper, new XOR circuit and Binary to Gray code converter circuit with XOR are proposed. The proposed circuits are highly efficient in terms of cell area, cell count, majority voter and latency. These proposed circuits are compared with conventional circuits and their comparisons are tabled. The comparison shows that proposed circuits are efficient and the area can be reduced more than 85% in QCA when compared to CMOS technology.

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