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Design and Analysis of Low Power Track and Hold Circuit using 32 nm Technology

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Abstract: This Paper introduces module of conventional track and hold circuit, differential track and hold circuit and two stage track and hold circuit using Microwind 3.1 VLSI Backnend Software. A very fast and linear T & H circuit is the key element in any modern wideband data acquisition system. Applications like a cable-TV or a broad variety of different radio standards require high processing speeds with high resolution. The results came from the proposed module shows the circuit made in 32nm technology consumed less power which is 9.083 uW for conventional track and hold circuit. 5.107 uW for Differential track and hold circuit and 76.30 uW .

Keywords: Track and Hold circuit, low power consumption, low chip area, sampling switch.

I. INTRODUCTION

Track and hold circuit is the fundamental block for anolog-to-digital converters(A/D). Its use allows most dynamic errors of A/D converters to be reduced, especially those showing up when using high frequency input signals. Track and hold circuit is inserted in front of a comparator array of a flash A/D converter to keep comparator's input voltages constant while the comparators are settling their output voltage levels. This Project includes different approaches for track and hold circuit.

II. LITERATURE REVIEW

From the rigorous review of related work and published literature it is observed that many researchers have designed different techniques for high speed communication in different techonologies.
Since the real world today VLSI/CMOS very much in demand, from the careful study of reported work it is observed that track and hold circuit is the fundamental block for block for A to D converters. Its used for most dynamic errors of A to D converters to be reduced especially high frequency input signal.

A.N. Karanicolas, "A 2.7-V 300-MS/s track-and-hold amplifier," IEEE J. Solid-State Circuits, Dec,1997. In this Paper A.N. Karanicolas invented a fully differential bipolar track and hold amplifier(THA) employed an open-loop linearization technique compatible with low supply voltage. A feed through reduction method utilized the junction capacitance of a replica switch to provide a close match to the junction capacitance of the main switch.[1]

W. Yu, S. Sen and B. H. Leung, "Distortion Analysis of MOS Track-and-Hold Sampling Mixers Using Time-Varying Volterra Series",IEEE Transactions on circuits and systems-II: Analog and Digital Signal Processing, vol. 46, No. 2, Feb.1999. In this paper time-varying theory of Volterra series is developed and applied in the sampled-data domain to solve for harmonic and intermodulation distortion of a MOS-based track-and-hold sampling mixer with a nonzero fall-time LO waveform. Distortion due to sampling error is also calculated.

These results, when combined with the continuous-time solution, quantify harmonic and intermodulation distortion of a track-and-hold type mixer completely. Closed form solutions are obtained. As a practical consequence, it is shown that for certain fall-time, the distortion of track-and-hold mixers can be better than what would be predicted by a simple application of time-invariant Volterra series theory.[2]

A. Boni, A. Pierazzi, and C. Morandi, "A 10-b 185-MS/s track-and-hold in 0.35-µm CMOS,"IEEE J. Solid-State Circuits,,Feb. 2001. This master paper described the design of a track-and-hold (T&H) circuit with 10bit resolution, 185MS/s. It is designed in a 0.35µm CMOS process. The circuit is supposed to work together with a 10bit pipelined analog to digital converter.[3]

Mohammad Hekmat and Vikram Garg, "Design and Analysis of a Source-Follower Track-and-Hold Circuit" , EE315 (VLSI data conversion circuits), June 2006, this paper investigates effect of various design schemes and

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circuit topology for track and-hold circuit to achieve acceptable linearly, high slew rate, low power consumption and low noise.[4]

Takahide SATO†a), Member, Isamu MATSUMOTO, Nonmember,Shigetaka TAKAGI, Member, and Nobuo FUJII, Fellow, "Design of Low Power Track and Hold Circuit Based on Two Stage Structure",june 2008. In this paper, two track and hold circuits are designed and implemented using 65 nm CMOS technology. The first circuit is based on a dummy switch topology to decrease the charge injection error. The second circuit used a clock linearization technique to reduce the sampling instant inaccuracy. Simulation results showed that the track and hold circuit based on dummy transistor technique presented the best performances in terms of rapidity and accuracy.[5]

III. PROBLEM DEFINITION

Track and hold circuit is an important block used in Analog to Digital converter infront of array comparators to keep comparators input voltage constant.

Hence to design stable track and hold circuit is main task of our project proposal. Various design schemes and circuit topology will be investigated for track and hold circuit. Track and hold circuit will be design using 32 nm CMOS technology to acheive acceptable linearity and low noise.

Today, for high speed communication circuit power consumption is important parameter. Hence the problem definition of proposed project work is to design and analyse low power, low chip area track and hold circuit applicable for high speed communication.

IV. PROPOSED WORK

The circuit diagram of Track and Hold circuit is

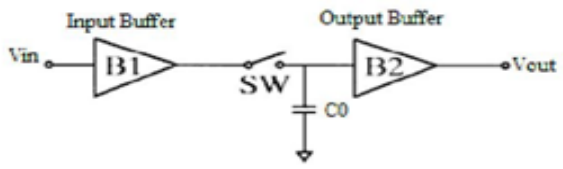

Figure: Circuit of Track and Hold circuit

The above circuit consist input and output buffer is simply connected by sampling switch Track and hold circuit is a newly found fundamental circuit, whose behaviour is predicted by various design schemes and investigations of circuit topologies. Every step of design follows the design flow of Microwind 3.1 software. The design methodology will be according to VLSI design flow.

To achieve the proposed target following steps are included in the design and analysis of track and hold circuit.

1) Design of single MOS switch using 32 nm CMOS technology.
2) Design of Transmission gate using 32 nm CMOS technology.
3) Design of conventional track and hold circuit using source follower.
5) Design and analysis of fully differential track and hold circuit
6)Design and analysis of two stage track and hold circuit using conventional circuit.
7) Comparison of all track and hold circuit and their analysis.

V. DESIGN METHODOLOGY

Conventional T/H circuit:

A conventional source follower T/H circuit basically consists of input, output buffers, a switch and a sampling capacitor. An output buffer is usually used to charge and discharge the input capacitances of following comparators.

A T/H circuit has two operation phases named "track phase" and "hold phase". During a track phase the switch is shorted and V_{out} becomes equal to V_{in}. On the other hand, during a hold phase the switch is opened and the T/H circuit keeps its output voltage equal to the value at end of track phase. A required hold time of a T/H circuit is usually decided by a settling time of the following comparators since the comparators must settle their output voltage during a hold time.

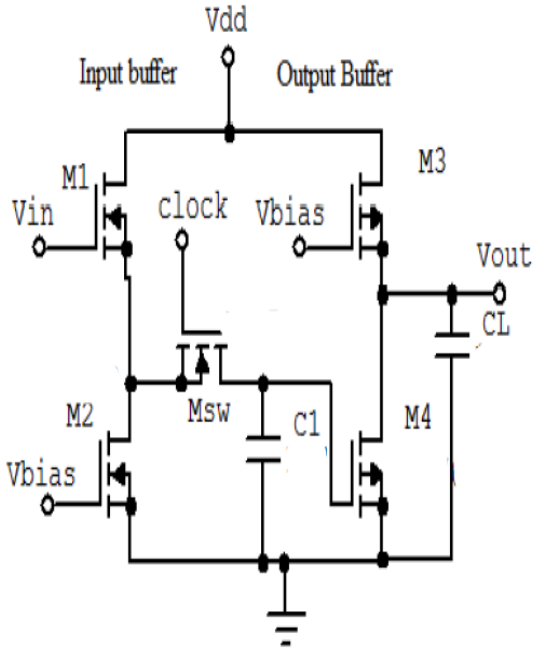

Figure. CMOS Design conventional T/H

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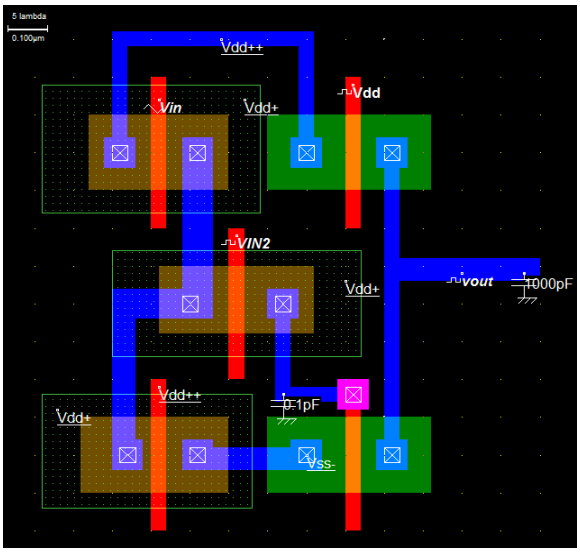
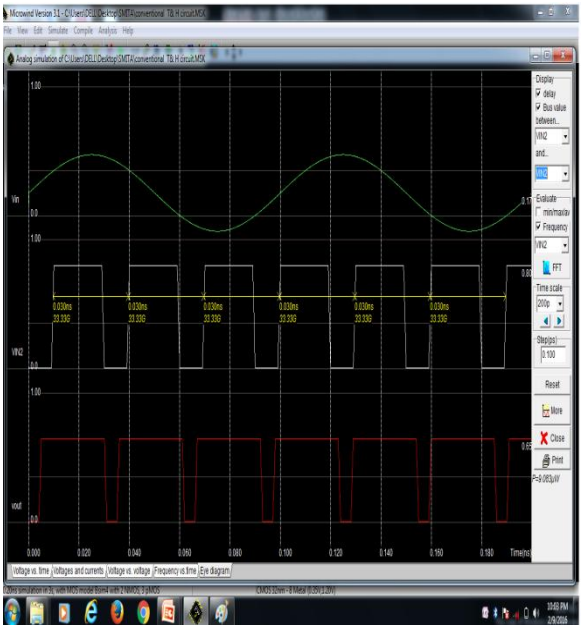
VLSI Design of Conventional T/H circuit:



Design specification of T/H circuit:

Cmos technology	32nm
Chip Area	Width: 5.1µm Height: 3.3 µm Surf: 16.8 µm
3 PMOS	P1 : 0.180×0.40 µm P2 : 0.200×0.040 µm P3 : 0.200×0.040 µm
2 NMOS	N1 : 0.200×0.40 µm N2 : 0.200×0.40 µm
Load Capacitance	1000 pf
Holding Capacitance	0.1 pf

Output Waveform of conventional T/H circuit:



Hspice simulation of conventional T/H circuit:

Power consumption	9.083 uW
Amplitude of Vin	0.4 v
Amplitude of VIN	0.80 v
Track time	0.020 ns
Hold time	0.04 ns

Differential T/H circuit

Following figure shows that input and output buffers of conventional Track-and-Hold circuit are modified in differential manner so that common mode noise could be suppressed. This architecture suppress the noise upto 60-70% as compared to conventional one but at the cost of power consumption and area overhead.

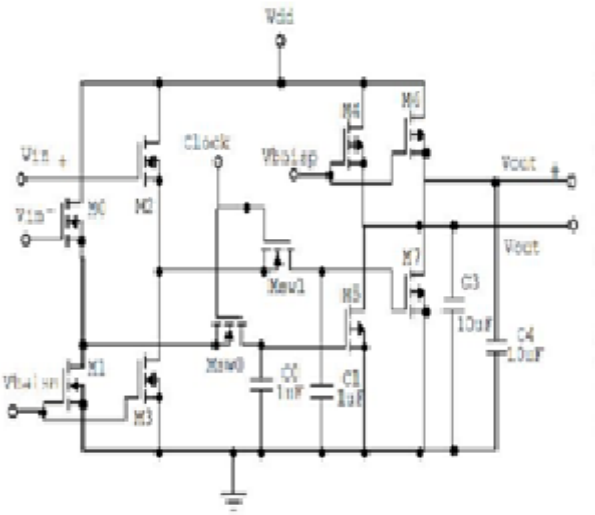
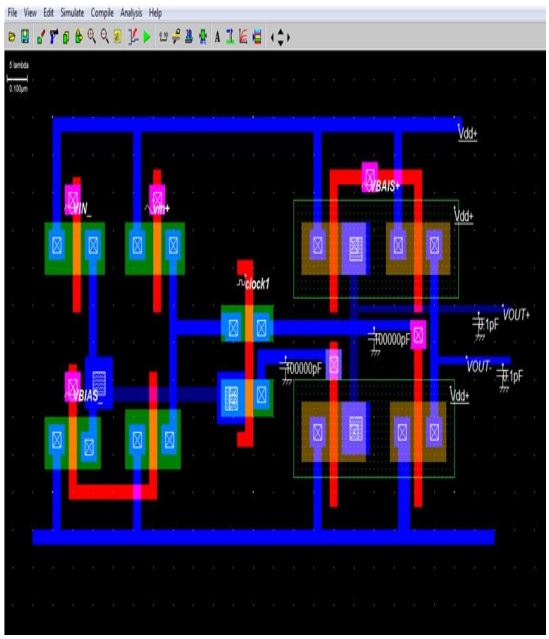


Figure: CMOS design of Differntial track and hold circuit

VLSI Design of Differential T/H circuit:



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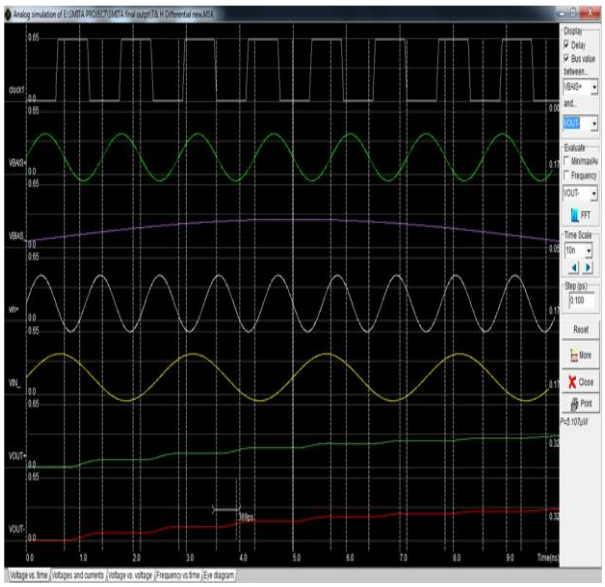
Design specification of Differential T/H circuit:



Output waveform of Differential T/H circuit:

CMOS technology	32nm
Chip area	Width:-3.1um Height:-1.1 um Surf:-3.6 um2
4 PMOS	P1:-0.140×0.040 um P2:-0.160×0.040 um P3:-0.140×0.040 um P4:-0.160×0.040 um
6 NMOS	N1:-0.100×0.040 um N2:-0.100×0.040 um N3:-0.140×0.040 um N4:-0.160×0.040 um N5:-0.140×0.040 um N6:-0.140×0.040 um
Load Capacitance	0.1 pf
Holding capacitance	100000 pf

Hspice simulation of Differntial T/H circuit:

Power consumption	5.107 uW
Amplitude of clock1	0.65 v
Amplitude of V_{BIAS+}	0.27 v
Amplitude of V_{BIAS-}	0.21 v
Amplitude of V_{in}	0.27 v
Amplitude of V_{IN}	0.21 v
Amplitude of V_{OUT+}	0.32 v
Amplitude of V_{OUT-}	0.32 v
Track time	0.4 ns
Hold time	0.6 ns

Two-Stage T/H using Conventional T/H Circuit:

In two-stage T/H circuit, two conventional T/H circuits are connected in cascade. The output of the first T/H serves as the input to the next T/H. If the input voltage of a T/H circuit is kept constant during its track phase, only one of charging or discharging is occurred in a track phase. In this case the output voltage of the T/H circuit settles monotonously into the constant voltage from the beginning of the track phase and its hold time must be as long as possible. This reduction of the tracking time results in a low power consumption. In order to apply such a constant voltage to the T/H circuit an additional small T/H circuit is inserted in front of the original T/H circuit as shown in Figure. Inverting and non-inverting clocks are applied to the two switches, Msw0 and Msw1, respectively so that the two T/H circuits act reciprocally.

When the second T/H circuit is in a track phase the first T/H circuit is always in a hold phase whose output voltage is constant. The first T/H circuit also charges and discharges its load capacitance during a track phase, however, it can operate very fast because its load capacitance is much smaller than that of the conventional T/H circuit.

The first T/H circuit consumes very low power when the first T/H circuit and the conventional one have the same operation speed. The output voltage of the first stage is applied to the second T/H circuit. When the second T/H circuit is in the track phase, its input voltage is always constant because the first T/H circuit is already in the hold phase. Therefore, its output voltage approaches to the final value directly and it's settling time decreases drastically.

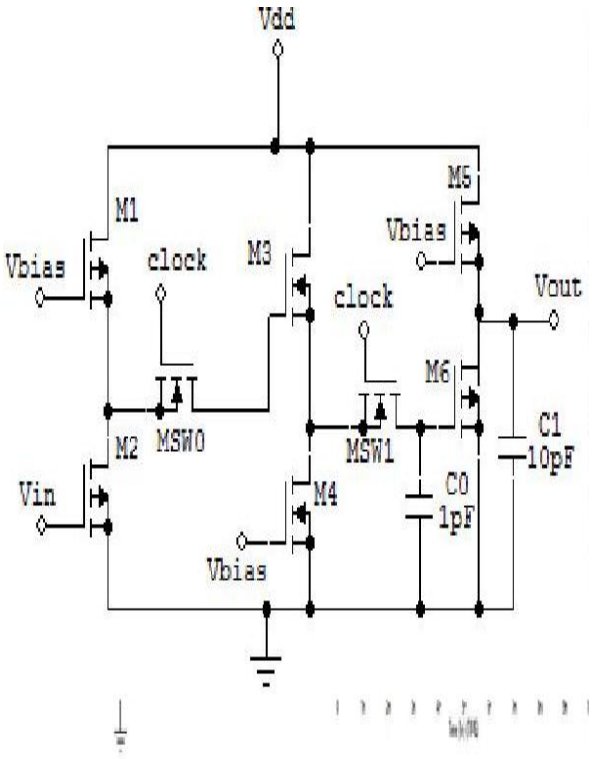


Figure: CMOS design of Two staged T/H circuit

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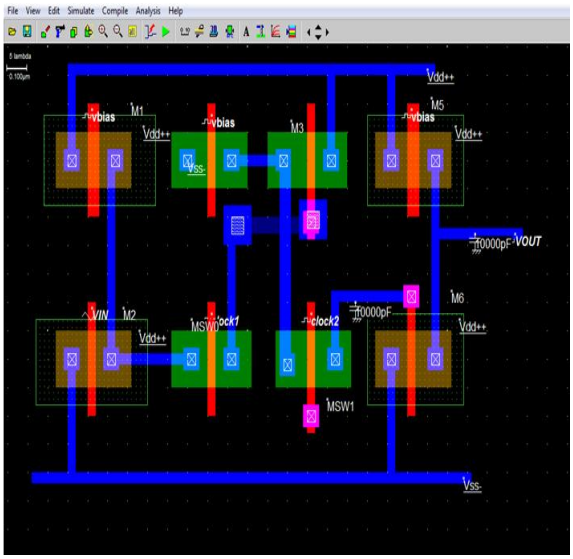
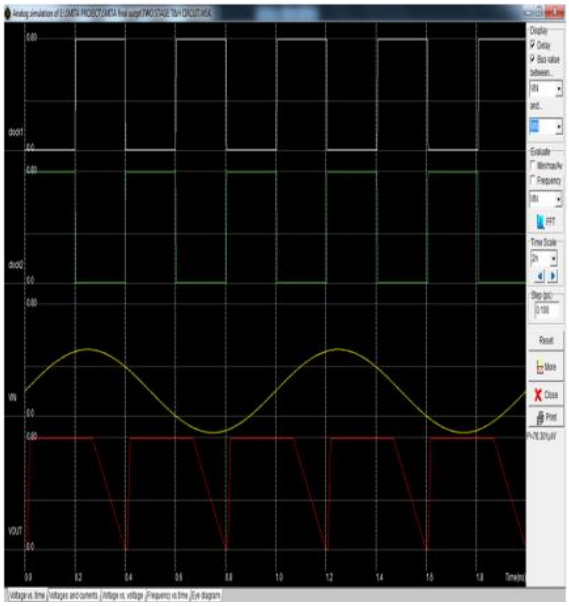
VLSI Design of Two Stage T/H circuit:



Design specification of Two Stage T/H circuit:

CMOS technology	32nm
Chip area	Width:-3.0 um Height:-1.5um Surf:4.5 um2
4 PMOS	P1:-0.200×0.060 um P2:-0.200×0.040 um P3:-0.200×0.060 um P4:-0.200×0.040 um
4 NMOS	N1:-0.200×0.040 um N2:0.200×0.040 um N3:-0.200×0.040 um N4:-0.200×0.040 um

Output waveform of Two Stage T/H circuit:



Hspice simulation of Two Stage T/H circuit:

Power consumption	76.30 uW
Amplitude of clock 1	0.80 v
Amplitude of clock 2	0.80 v
Amplitude of V_{IN}	0.50 v
Amplitude of V_{OUT}	0.80
Track time	0.98 ns
Hold time	0.08 ns

V. CONCLUSION AND FUTURE SCOPE

This paper resulted that the modules of conventional track and hold circuit, differential track and hold circuit and two staged track and hold circuit are made by using 32nm CMOS technology. The purpose of this work is to design a low-power track-and-hold circuit with a supply voltage of 0.8-1.2 V. The above result showed that the power consumption is very low which is 9.083 uW of conventional track and hold circuit, 5.107 uW is of Differntial track and hold circuit and and 76.30 uW is of two stage track and hold circuit.

We can modified this work by using less nanometer technology. In future we can make the modules in 25nm tecknology which will result the less power consumption than this. It will also consume less chip area..

VI. REFERENCES

1) A.N. Karanicolas, "A 2.7-V 300-MS/s track-and-hold amplifier," IEEE J. Solid-State Circuits, vol.32, pp.1961–1967, Dec. 1997.
2) W. Yu, S. Sen and B. H. Leung, "Distortion Analysis of MOS Track-and-Hold Sampling Mixers Using Time-Varying Volterra Series",IEEE Transactions on circuits and systems-II: Analog and Digital Signal Processing, vol. 46, No. 2, Feb.1999.
3) A. Boni, A. Pierazzi, and C. Morandi, "A 10-b 185-MS/s track-and-hold in 0.35-µm CMOS," IEEE J. Solid-State Circuits, vol. 36, pp. 195–203,Feb. 2001.
4) Mohammad Hekmat and Vikram Garg, " Design and Analysis of a Source-Follower Track-and-Hold Circuit" , EE315 (VLSI data conversion circuits) project report June 2006
5) Takahide SATO†a), Member, Isamu MATSUMOTO, Nonmember, Shigetaka TAKAGI, Member, and Nobuo FUJII, Fellow, Design of Low Power Track and Hold Circuit Based on Two Stage Structure, IEICE TRANS. ELECTRON., VOL.E91–C, NO.6 JUNE 2008