IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 3, March 2017

Improved Design of Ultra Low Power True Single Phase Clock CMOS 2/3 prescaler with 6 GHz, 199 µW

Roshan Kumar[1], Prof. Monika Kapoor[2]

PG Student, VLSI Design, ECE Department, Lakshmi Narain College of Technology, Bhopal, MP, India[1]

Associate Professor, ECE Department, Lakshmi Narain College of Technology, Bhopal, MP, India[2]

Abstract: An improved and power efficient layout is proposed for Conventional TSPC prescaler and Design-I ofbase paper and compared with the existing TSPC and E-TSPC prescalers on the basis of operating frequency and power consumption. The proposed layout of Conventional TSPC prescaler can operate up to 5.1 GHz with 264 µW power consumption at 1.8 V supply voltage for both divide by 2 and divide by 3 mode, which is three times power efficient with 20% improved frequency response. The lowest power consumption is achievedin improved layout of Design-I ofbase paper based architecture which can operate up to 6GHz and consumes 290 µW power for divide by 2 mode and 199 µW for divide by 3 mode at 1.8V supply voltage, which is two and half times power efficient with 10% better frequency response.

Keywords: Dual modulus prescaler, D Flip-flop (DFF), True single phase clock (TSPC), Microwind, DSCH, Frequency synthesizer, Clock, Propagation Delay.

I. INTRODUCTION

Frequency synthesizer plays a major role in a digital circuits where multiple and/or variable clock frequency are required. It's an electronic system that generates a range of frequencies from an oscillator or single fixed time-based signal. It converts one stable base frequency to another by using different techniques such as frequency divider, frequency multiplier and direct digital synthesizer. In a frequency synthesizer, a high speed dual modulus prescaler is the most important circuit block. It also be used in other electronic systemssuch as clock generator, timing recovery circuit etc. The power consumption of a prescaler is highest among all other blocks of synthesizer.That's why the reduction in power consumption of prescaler reflects an efficient frequency synthesizer. A dual modulus prescaler uses a wideband swallow frequency dividerand has N and N+1 division ratios.Frequency synthesizer generates variable frequency with the help of prescaler and control circuit. This control circuit consist of two counters, Programmable Counter (P) and the Swallow Counter (S) as shown in Fig. 1.The combination of Prescaler and counters P and S performs N × P + S programmable division ratio.

Three types of flip-flop designs are mostly adopted for High speedprescaler. Those are source-coupled logic (SCL) [7], [8], injection locked frequency dividers (ILFDs) and dynamic latchfrequency synthesizer. Basically prescaler is a combination of D flop-flop and logic gates. Those D flop-flop are synchronised by either single phase clock[3], [5] or multiple phase clock. Those logic gates are used between D flop-flops to generate two consecutive divisional ratios. The prescaler is a synchronous circuit so the speed of the circuit is mostly affected by logic gates and switching power also increases.

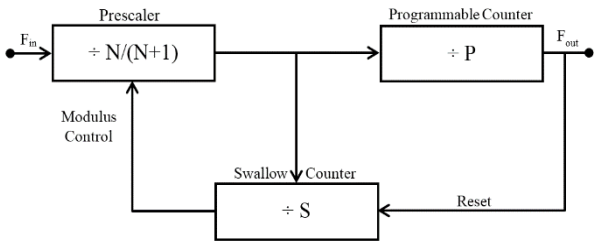

Fig. 1. Topology of the Pulse Swallow frequency divider

The CMOS N/ (N +1) source-coupled logic also known as current mode logic (CML) [7]based prescaler can be operated as high as 24 GHz [6]. But the major drawback of the prescaler is the large load capacitances which increases power consumption. On the other hand the injection locked frequency dividers (ILFDs) have very small locking range and it also required large chip area for injection locking circuit. The dynamic latch frequency synthesizer are the most power efficient and compact size frequency synthesizer but the slowest among three. For low frequency devices the dynamic latch is the best option. Different types of dynamic latch frequency synthesizer can operate on 1 GHz to 6.5 GHz. Those widely divided into two parts single clock phase frequency synthesiser and multi clock phase synthesizer. In this paper both true single phase clock (TSPC) and enhanced

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 3, March 2017

true single phase clock (E-TSPC) flip-flop based 2/3 prescaler are implemented and analysed.

II. TSPC ANDE-TSPC FLIP-FLOP

In dynamic latch frequency synthesiser, two or four phase clock frequency synthesiser are most suitable for compact circuits and the power efficiency is also better then single phase clock frequency synthesizer. These circuits can also be operated on higher frequency. But the biggest problem with multiple clock based frequency synthesiser is the clock skewing, which restricts these technics to be used in complex and big circuits. Because it is difficult to maintain equal electrical length of all the clocks through tracks to each component in entire device. So that the single phase clock frequency synthesiser is batter option for big and complex circuit. In this section TSPC [3], [9], and E-TSPC [10] based flip-flops are investigated with its power consumption and frequency response.

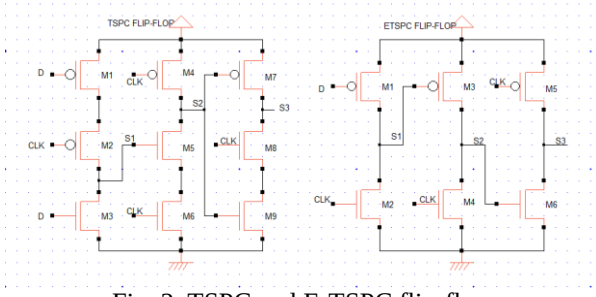

Fig. 2. TSPC and E-TSPC flip-flop

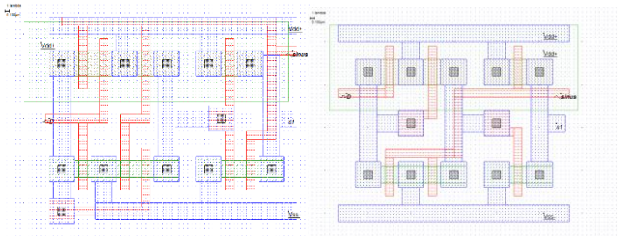

Fig. 3. TSPC and E-TSPC flip-flop Layout.

Both the flip-flops required three stages to generate output from input. The TSPC flip-flop acquires three Transistors in each stage while E-TSPC flip-flop needs only two as in Fig. 2. The calculation of load capacitances is done by connecting output (Q) of both the flip-flops to their corresponding inputs (D). The load capacitance of TSPC and E-TSPC according to method [11] and [12] is given by

$$C_{L_{TSPC}} = C_{DB_{M8}} + 2C_{GD_{M8}} + C_{DB_{M7}} + 2C_{GD_{M7}} + C_{G_{M3}} + C_{G_{M1}}$$

$$C_{L_{E-TSPC}} = C_{DB_{M6}} + 2C_{GD_{M6}} + C_{DB_{M5}} + 2C_{GD_{M5}} + C_{G_{M1}}$$

According to those equations, TSPC flip-flop has higher load capacitance than E-TSPC flip-flop. It shows the TSPC flip-flop consumes more power than E-TSPC at switching which is dependent on load capacitance is given by

$$P_{switching} = f_{clk} C_L V_{dd}^2$$

Though the TSPC has higher switching power but ideally there is on direct path between supply voltage and ground during operation. As the transistors are not identical and PMOS and NMOS are not reciprocal as long as electrical properties are concerned, some power is consumed, it is called short circuit power. It also depends on rise and fall time of the input signals and clocks. The short circuit power [13] is directly proportional to the load capacitance. Since there is one direct path always exists between each consecutive stages at the time of transition between supply voltage and ground in E-TSPC flip-flop. So that it consumes significantly more short circuit current than TSPC flip-flop. The short circuit power also dependent on the time for which a transistor is in floating state (neither high nor low) which increases with increasing frequency. Which again shows that in E-TSPC short circuit power increases with increases in clock frequency.

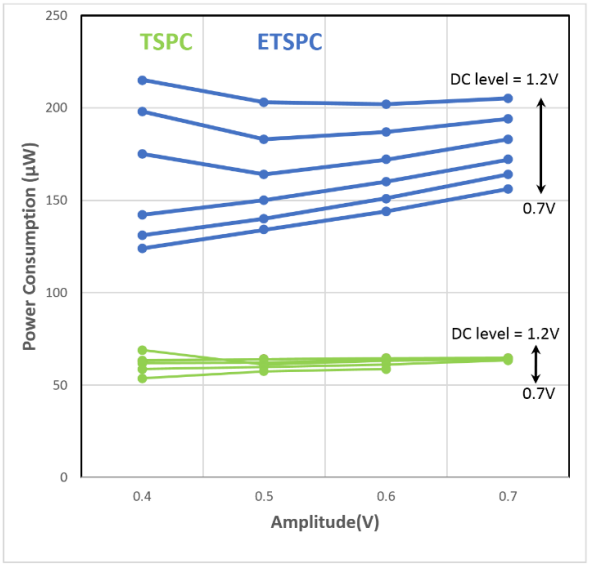

Fig. 4. Power consumption against different DC levels and amplitude of clock signal for TSPC and E-TSPC flip-flop.

Now take a glance at the input clock, it is usually generated by voltage controlled oscillator (VCO). The output of an oscillator is not a full swing signal. It always have some certain DC level with pick to pick amplitude less than supply voltage. This type of signal may not drive the circuit for some combination of DC levels and amplitudes and it also affects short circuit power.

The circuit analysis is done by Microwind using 180nm technologyat 1.8 Volts V_{dd}.Layout of both TSPC flip-flop and E-TSPC flip-flop shown in Fig. 3 are designed simulated with deferent DC levels and variable amplitudes at same 4 GHz frequency to find out dependency of circuits on output of VCO and also to analyse the power consumption. In simulation both circuits are tested on DC levels from 0.7 to 1.2 volts, and for each DC level, clock amplitude is also varied from 400mV to 700mV. The input

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 3, March 2017

is a 1 GHz signal with 50 ps of rise time and fall time. The simulation shows the power consumption of TSPC flip-flop varies from 50 to 65 µW for entire range of tested DC level and Amplitudes. On the other hand ETSPC flip-flop consumed more power from 120 to 215 µW which is not only more than double but also varies significantly with DC levels and Amplitudes. It is also observed that the output waveforms of TSPC flip-flop is quiet identical in all simulation but the wave forms of ETSPC flip-flop simulation are deferent in shape and amplitude also varies with different combinations of DC levels and amplitude of input signal. The ETSPC is not good to operate with low amplitude and DC levels as it consumes more power. The simulation results in Fig. 4 shows that the TSPC flip-flop is better than ETSPC flip-flop.

III. ANALYSIS OF TSPC ANDE-TSPC PRESCALER

The TSPC prescalers consumes less power because of minimal short circuit power consumption but maximum operating frequency is also less than ETSPC based prescalers. E-TSPC prescalers has capability of operating at higher frequency but consumes more power, E-TSPC also needs less area for fabrication. The conventional TSPC and E-TSPC prescalers uses 2 flip flops one AND gate and one OR gate,shown in Fig. 5 with schematic in Fig. 6. The E-TSPC prescaler proposed in [14] has a problem that when the prescaler performing divide by 2 operation the one of the flip-flop consumes unnecessary power while it is not participating in operation. In [15] an optimized 2/3 E-TSPC prescaler is proposed in which both AND and OR gatesare embedded in to flip-flops to reduce power consumption and propagation delay so that it can operate up to 6.7 GHz while the 2/3 prescaler unit in [14] can operate up to 5.5 GHz at supply voltage of 1.5 V. The [15] bypass the first flip-flop when divide by 2 operation is performed which reduces power consumption significantly. It is done by replacing AND gate and OR gate by two AND gates.

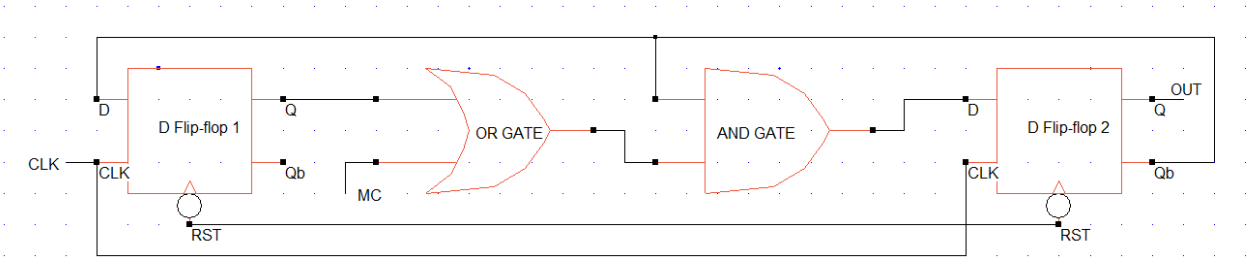

Fig. 5. Conventional TSPC 2/3 prescaler circuit

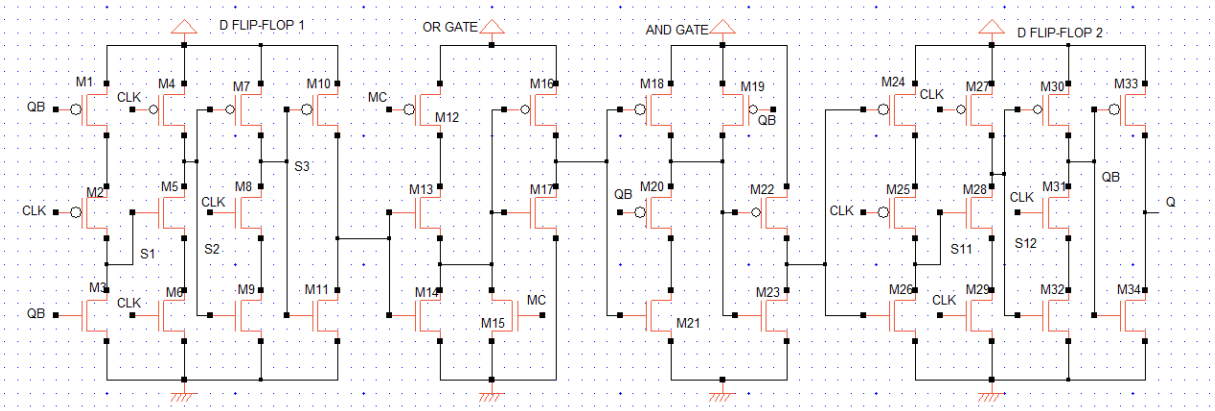

Fig 6. Conventional TSPC 2/3 prescaler gate level schematic diagram

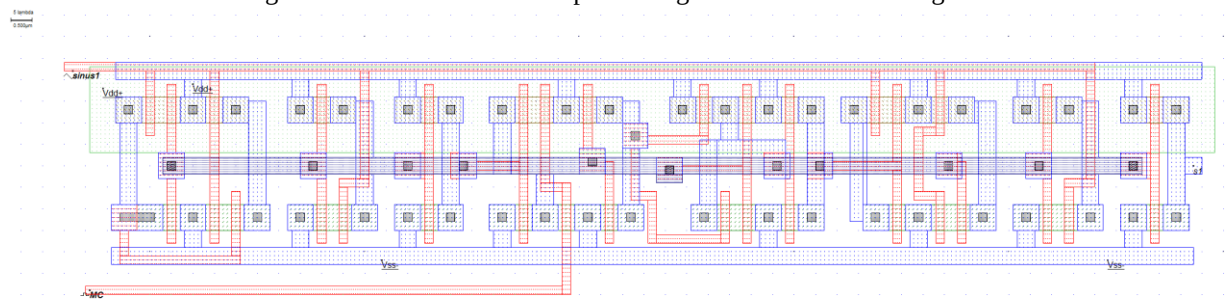

Fig. 7. Improved layout of Conventional TSPC 2/3 prescaler

DOI 10.17148/IJIREEICE.2017.5332

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 3, March 2017

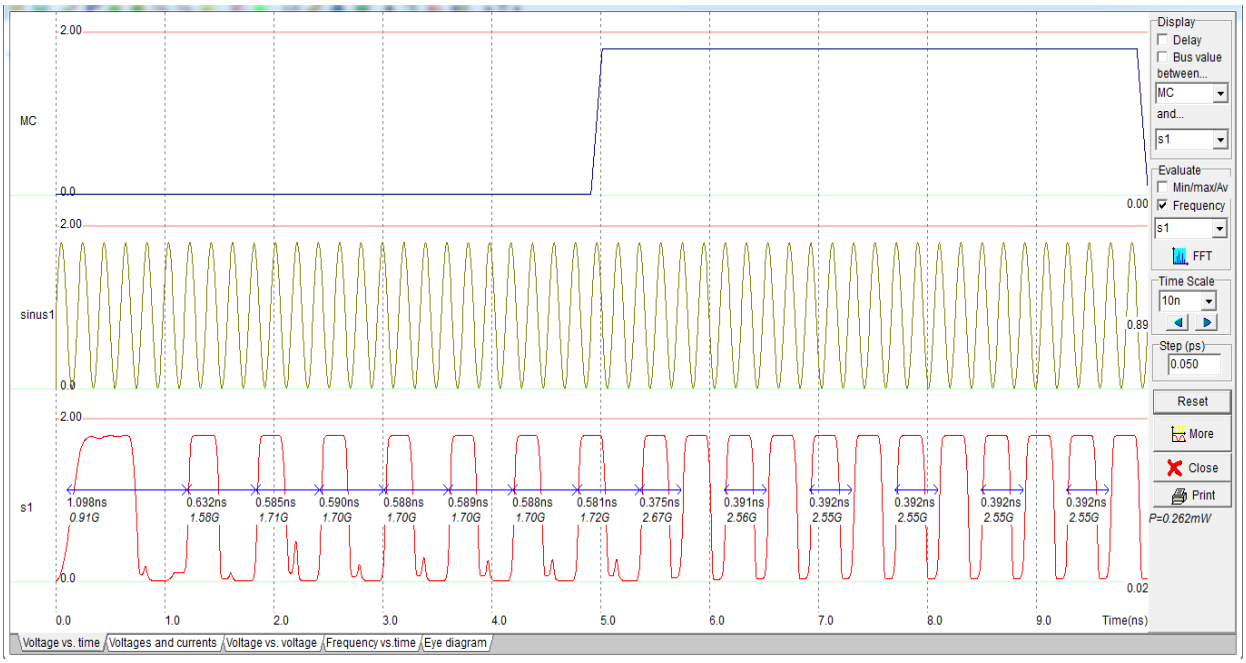

Fig. 8. Frequency response of improved layout of Conventional TSPC 2/3 prescaler at 5.1 GHz

The TSPC prescalers proposed in [1] uses two NOR gates at the places of one AND gate and one OR gate as in Fig. 9with schematic in Fig. 10. It reduces the number of transistors required in conventional TSPC prescaler which reduces propagation delay significantly so that the circuit can operate up to 5.5 GHz which is 30% faster than conventional TSPC prescaler. And in second prescaler proposed in [1] the first flip-flop is switched off using MOD control signal to save power while divide by 2 operation is performed because it doesn't contribute in divide by 2 operation. This prescaler again reduce more than three times when divide by 2 operation is performed. Both the prescalers in [1] can be operated up to 5.5 GHz frequency at 1.8 V supply voltage.

This analysis shows that TSPC prescalers are better for ultra-low power applications because they consumes significantly low short circuit power, the propagation delay and switching power can be reduced by applying different techniques which are defined in [3], [4].

IV. SIMULATION AND MEASURMENT RESULTS

All the simulations are performed using Microwind 3.5 and DSCH 3.5 software with 180nm CMOS Technology. All the parameters are same for all prescalers accept voltage. In [14] and [15] prescalers the supply voltage is 1.5 V and for other prescalers supply voltage is 1.8 V. From the simulation the [1] is best in power consumption with 5.5 GHz operating frequency. In this paper conventional TSPC prescaler and First design of base paper layout is designed in Microwind, it is found that the automated layout has propagation delay about 180- 200 ps which restricts the circuit to operate properly over 5 GHz frequency. This delay is reduces by replacing metal 2, 3 by metal 1 and metal 2 (if required) [16]. This analogy helped to reduce power loss and consumption in conventional TSPC prescaler and First design of [1] and the area of is also reduced which again helped to reduce unnecessary body currents which flows from body voltage to Gate, Drain and source terminals.

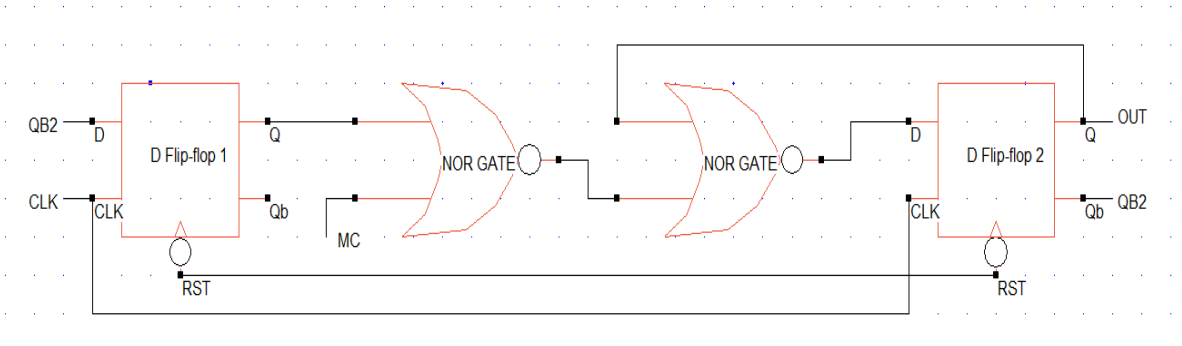

Fig. 9. TSPC 2/3 prescaler circuit proposed in [1].

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 3, March 2017

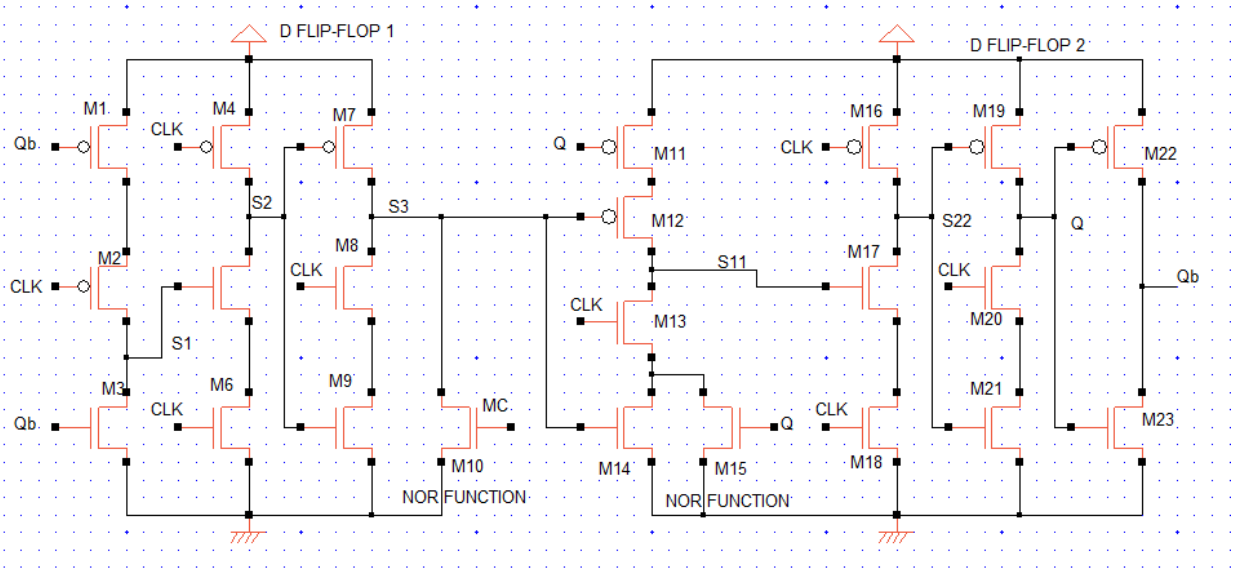

Fig. 10. TSPC 2/3prescaler gate level schematic diagram proposed in [1].

The rearrangement of transistors played the most important role because it reduced the propagation delay significantly. In Improved layout of conventional TSPC prescaler shown in Fig. 7, the W/L value is taken 1 because in Conventional TSPC prescaler due to the fact that in most of the stages there are two NMOS and one PMOS in circuit this combination generate same propagation delay because of the mobility ratio of 2:1 in NMOS and PMOS. In these combination of NMOS and PMOS power consumption reduced up to 40 % in corresponding stages, which contributed in overall reduction in power consumption and improved operation frequency up to 5.1 GHz shown in Fig. 8. The Improved layout of TSPC 2/3 prescaler proposed in [1] shown in Fig. 12 with Frequency response in Fig. 13 which can operate up to 6 GHz which is done by proper placement of transistors to reduce delay between transistors. Table 1 and Fig. 11shows the comparison among different prescalers discussed in this paper on the bases of power consumption and maximum operating frequency.

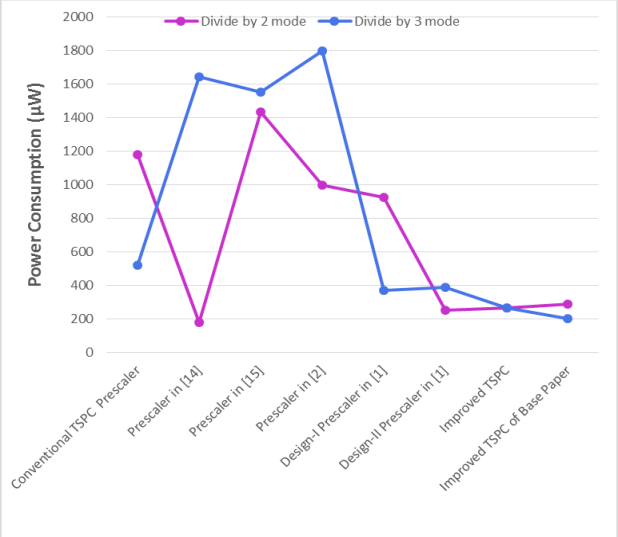

Fig. 11. Performance of different prescalers

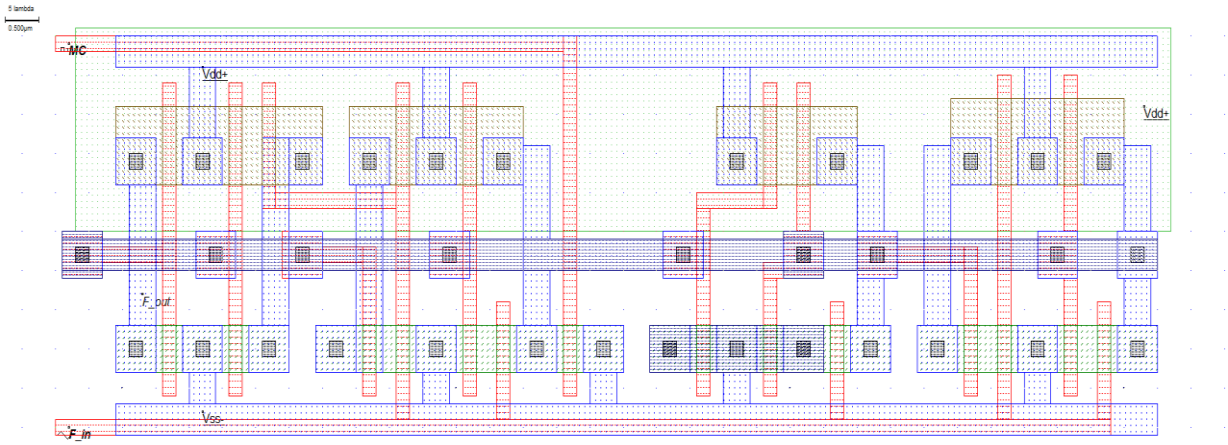

Fig. 12. Improved layout of TSPC 2/3 prescaler proposed in [1].

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 3, March 2017

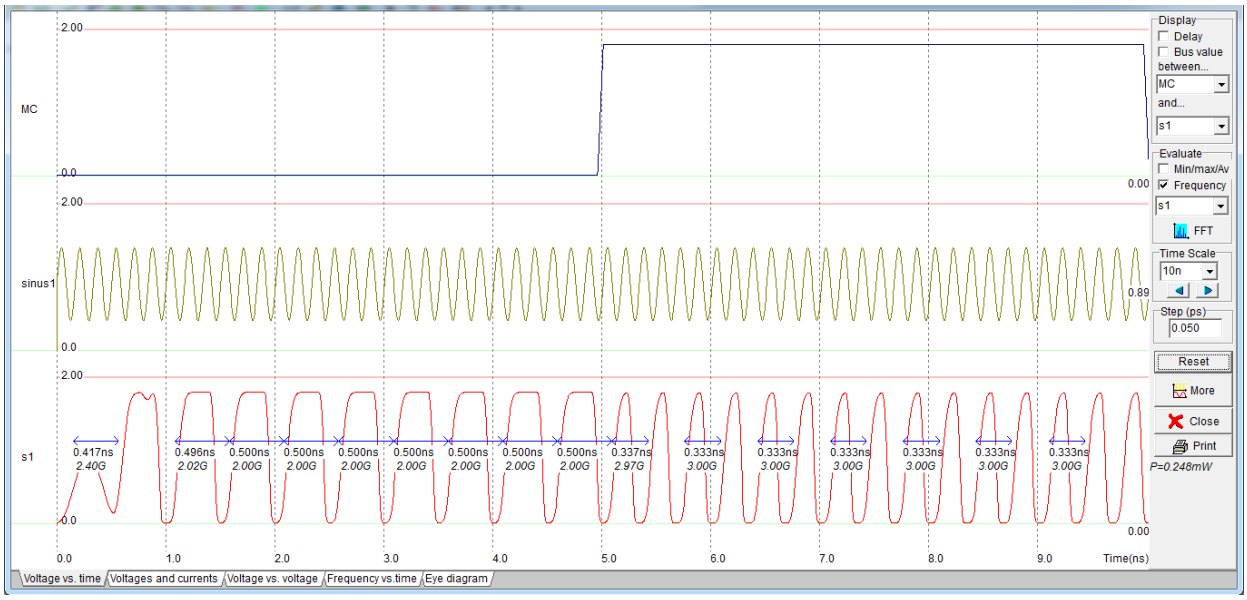

Fig. 13. Frequency response of improved layout of TSPC 2/3 prescaler proposed in [1] at 6 GHz.

Table 1. Power consumption and Maximum Frequency comparison of among different Prescalers

Design Parameters	Conventional TSPC Prescaler	Prescaler in [14]	Prescaler in [15]	Prescaler in [2]	Design-I Prescaler in [1]	Design-II Prescaler in [1]	Improved TSPC Prescaler	Improved Prescaler of Base Paper
Process (nm)	180	180	180	180	180	180	180	180
Supply Voltage (V)	1.8	1.5	1.5	1.8	1.8	1.8	1.8	1.8
Maximum Frequency (GHz)	4.2	5.5	6.7	6.5	5.5	5.5	5.1	6.0
Power consumption (µW) Divide-by-2 mode	1182	178	1433	1000	923	252	264	290
Power consumption(µW) Divide-by-3 mode	522	1643	1554	1800	369	387	263	199

V. CONCLUSION

This paper describes the response of Different prescalers on the bases of DC levels and amplitude of clock signal and analysis of TSPC and E-TSPC flip-flop and their power consumption comparison. The layout of Conventional TSPC prescaler and First design of base paper are implemented in Microwind 3.5 at 180nmat supply voltage 1.8V and customised to improve frequency response, area and to reduce power consumption. In this improvement the power consumption of Conventional TSPC prescaler is five times better in divide by 2 mode and half in divide by 3 mode and it can be operated up to 5.1 GHz. In the First design of base paper, the power consumption is reduced three times in divide by 2 mode and 85% in divide by 3 mode, the frequency response is also improved 10 % which is up to 6 GHz.

REFERENCES

[1] M. V. Krishna, M. A. Do, K. S. Yeo, W. M. Lim and C. C. Boon, "Design and Analysis of Ultra Low Power True Single Phase Clock CMOS 2/3 Prescaler," in IEEE Transaction on Circuits and Systems, vol. 57, pp. 72-82, Jan. 2010.

[2] M. V. Krishna, M. A. Do, K. S. Yeo, C. C. Boon and W. M. Lim, "A 1.8-V 6.5-GHz low power wide band single-phase clock CMOS 2/3 prescaler," in IEEE Int. Symp. on Circuits and Systems, vol. 53, pp. 149-152, Aug. 2010.

[3] Y. Ji-ren, I. Karlsson, and C. Svensson, "A true single-phase-clock dynamic CMOS circuit technique," IEEE J. Solid-State Circuits, vol. 24, pp. 62–70, Feb. 1989.

[4] Q. Huang and R. Rogenmoser, "Speed optimization of edge triggered CMOS circuits for gigahertz single-phase clocks," IEEE J. Solid-State Circuits, vol. 31, pp. 456–465, Mar. 1996.

[5] C.-Y. Yang, G.-K. Dehng, J.-M. Hsu, and S.-I. Liu, "New dynamic flip-flops for high-speed dual-modulus prescaler," IEEE J. Solid-state Circuits, vol. 33, pp. 1568–1571, Oct. 1998.

[6] H. D.Wohlmuth and D. Kehrer, "A 24 GHz dual-modulus prescaler in 90 nm CMOS," in IEEE Int. Symp. on Circuits and Systems,May

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 3, March 2017

2005, vol. 4, pp. 3227–3230.

[7] C. M. Hung, B. A. Floyd, N. Park, and O. Kenneth, "Fully integrated 5.35 GHz CMOS VCO and prescalers," IEEE Transactions on Microwave Theory and Techniques, vol. 49, no. 1, pp. 17–22, Jan. .

[8] M. Alioto and G. Palumbo, "Design strategies for source coupled logic gates," IEEE Trans. Circuits and Syst. I: Reg. Papers, vol. 50, no. 5, pp. 640–654, May 2003.

[9] J. Yuan and C. Svensson, "High-SpeedCMOS circuit technique," IEEE J. Solid-State Circuits, vol. 24, pp. 62–70, Feb. 1989.

[10] J. Navarro and W. Van Noije, "E-TSPC: Extended true single-phase clock CMOS circuit technique," in Proc. Int. Conf. on Integrated Syst. on Silicon IFIP and VLSI, London, U.K., 1997, pp. 165–176.

[11] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits, A Design Perspective, ser. Electron and VLSI, 2nd ed. Upper Saddle River, NJ: Prentice-Hall, 2003.

[12] S.-M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits, Analysis and Design, 3rd edition. New York: McGraw Hill, 2002.

[13] H. J. M. Veendrick, "Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits," IEEE J. Solid-State Circuits, vol. SC-19, no. 4, Aug. 1984.

[14] S. Pellerano, S. Levantino, C. Samori, and A. L. Lacaita, "A 13.5-mW 5 GHz frequency synthesizer with dynamic-logic frequency divider," IEEE J. Solid-State Circuits, vol. 39, no. 2, pp. 378–383, Feb. 2004.

[15] X. P. Yu, M. A. Do, W. M. Lim, K. S. Yeo, and J. G. Ma, "Design and optimization of the extended true single-phase clock-based prescaler," IEEE Trans. Microw. Theory Tech., vol. 54, no. 11, Nov. 2006.

[16] J. Yuan and C. Svensson, "New single-clock CMOS latches and flipflops with improved speed and power savings," IEEE J. Solid-state Circuits, vol. 32, no. 1, pp. 62–69, Jan. 1997.

DOI 10.17148/IJIREEICE.2017.5332