UGC Approved Journal

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 6, June 2017

An FPGA Implementation of OLS Encoder and Decoder for Efficient Data Transmission

Ms. M. Gayathri[1], Ms. Prema M.E[2]

Meenakshi Ramaswamy Engg College[1,2]

Abstract: Orthogonal Latin Square (OLS) codes that provide low latency decoding and a modular construction. For some applications, like multimedia or signal processing, the effect of errors on the memory bits can be very different depending on their position on the word. Therefore, in these cases, it is more effective to provide different degrees of error correction for the different bits. This is done with Unequal Error Protection (UEP) codes. In this paper, UEP codes are derived from Double Error Correction (DEC) Orthogonal Latin Square (OLS) codes. The derived codes are implemented for an FPGA platform to evaluate the decoder complexity and latency. The OLSC Project has two major Process Encoder and Decoder. In the Decoder Part we modified the Syndrome Computation unit as well as we designed a Complete Setup of transmitter and Receiver via Encoder and Decoder. The results show that the new codes can be implemented with lower decoding delay than traditional SEC-DED codes and with a cost similar to that of both DEC OLS and SEC-DED codes. The Proposed encoder and decoder are done by Verilog HDL and Simulated by Modelsim 6.4 c and synthesized by Xilinx tool.

Index Terms: DEP, UEP, OLS, Majority logic decoding.

I. INTRODUCTION

Error Correction Codes (ECCs) are widely used to protect memories and other electronic circuits against errors. One key requirement for the ECCs that are used in memories and circuits is that the decoders have to operate at high speed to minimize the impact on the overall circuit speed. This has brought the attention of researchers to codes that can be decoded using Majority Logic (ML). There are also the double-error correcting triple-error-detecting (DEC-TED) codes, which come at the cost of much larger overhead in terms of both the check bits and more complex hardware to implement the error correction and detection the general drawbacks 3 with these methods are latency and speed. Most of these codes require several cycles to correct the first error unlike the SEC-DED codes. Moreover, the encoding and decoding are much more complex and require several table lookups for multiplication in higher order fields. However in spite of their low check bits overhead and single cycle decoding, SEC-DED codes are not able to provide requisite reliability under certain conditions. There are several sources of errors that affect modern electronic circuits, such as manufacturing defects, circuit ageing, electromagnetic disturbances or radiation induced soft errors. Many different techniques can be used to either prevent failures from occurring or to detect and correct them. Those include modifications to the manufacturing process, circuit level and logic level techniques. Techniques at different levels are commonly combined to achieve the desired reliability target.

Orthogonal Latin Squares Decoders

The key parameters of an OLS code are its data block size k and the number of errors that can be corrected t. The block size is of the form k=m2 bits and to correct t errors, k= 2tm parity check bits are needed. For example when m= 4, the data block size is 16 bits and if t = 2, the num of parity check bits is also 16. The parity check matrix of this code.The decoding of OLS codes is done using majority logic. In particular, the decoded bit can be obtained from the values of 2t recomputed parity check bits and the bit itself. k= 16 and t = 2, four parity check bits and the bit to be decoded are used. The majority vote can be implemented in two different ways. The first option is to re-compute the four parity check bits and take a majority vote among them. When there is a majority of ones, an error has occurred and the bit is corrected.

II. RELATED WORKS

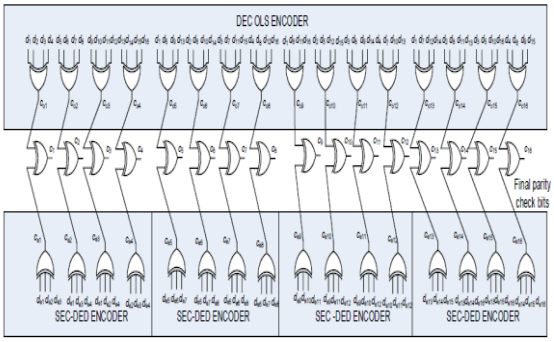
The double error correcting (DEC) BCH codes have not found favorable application in SRAMs due to non-alignment of their block sizes to typical memory word widths and particularly due to the large multi-cycle latency of traditional iterative decoding algorithms. This work presents DEC code design that is aligned to typical memory word widths and a parallel decoding implementation approach that operates on complete memory words in a single cycle. The practicality of this approach is demonstrated through ASIC implementations, in which it incurs only 1.4ns and 2.2ns decoding latencies for 16- and 64-bit words, respectively, using 90nm ASIC technology. A comparative analysis between conventionally used ECC and DEC ECC for reliability gains and costs incurred has also been performed. C. L. Chen and M. Y. Hsiao

UGC Approved Journal
IJIREEICE
ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526
International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 6, June 2017

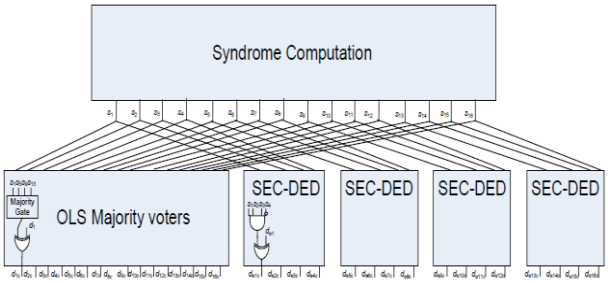
was proposed this paper presents a state-of-the-art review of error-correcting codes for computer semiconductor memory applications. The construction of four classes of error-correcting codes appropriate for semiconductor memory designs is described, and for each class of codes the number of check bits required for commonly used data lengths is provided. The implementation aspects of error correction and error detection are also discussed, and certain algorithms useful in extending the error-correcting capability for the correction of soft errors such as a-particle-induced errors are examined in some detail was done by R. Nasser and J. Draper.

III. PROPOSED SYSTEM

Two techniques to derive UEP codes from DEC OLS codes based are presented. The proposed codes ensure that important bits are corrected when there is a double error and that all single errors are corrected. Additionally, some double errors that affect the least significant bits can also be corrected. The codes can be decoded in parallel with low complexity and latency and do not require any additional parity bit compared to standard DEC OLS codes



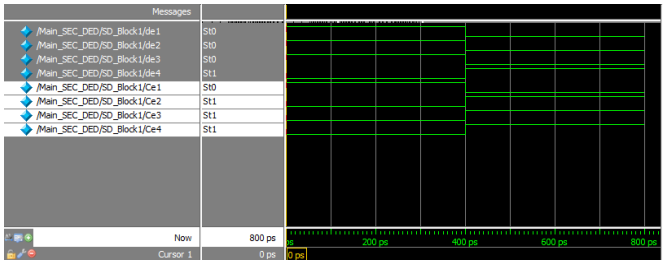
Encoder For The Proposed (48, 16, 16) DEC OLS Code



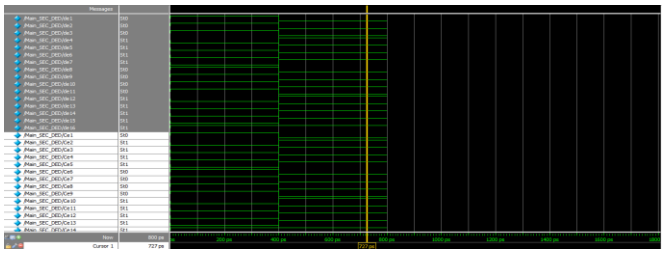
Decoder For The Proposed (48,16,16) DEC OLS Code

IV. RESULTS AND DESCRIPTION

SEC DED Encoder



SEC-DED Main



UGC Approved Journal

IJIREEICE

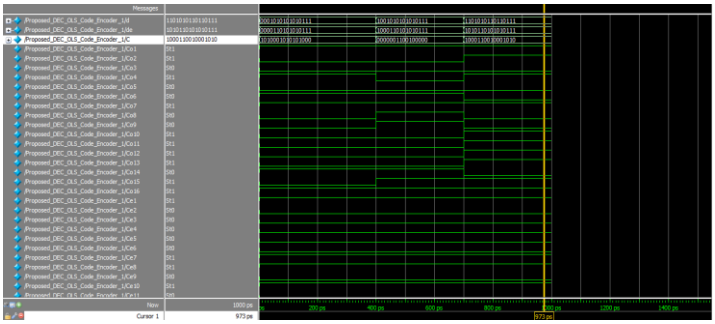
ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

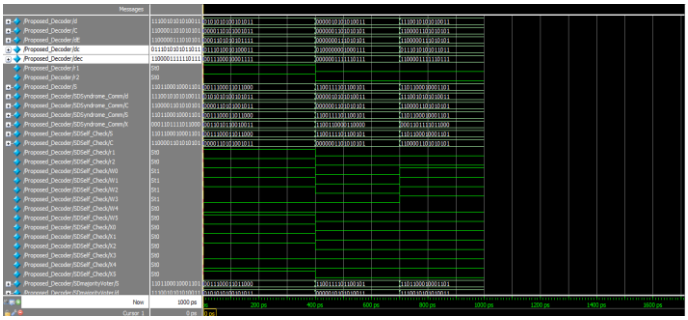
ISO 3297:2007 Certified

Vol. 5, Issue 6, June 2017

Proposed DEC OLS Code Encoder



PROPOSED OLSC DECODER



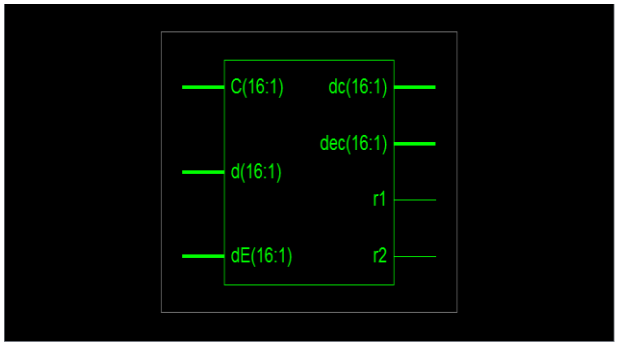
DEVICE UTILIZATION SUMMARY FOR ENCODER

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	32	3,840	1%	
Logic Distribution				
Number of occupied Slices	16	1,920	1%	
Number of Slices containing only related logic	16	16	100%	
Number of Slices containing unrelated logic	0	16	0%	
Total Number of 4 input LUTs	32	3,840	1%	
Number of bonded IOBs	48	97	49%	
Total equivalent gate count for design	192			
Additional JTAG gate count for IOBs	2,304			

DEVICE UTILIZATION SUMMARY FOR DECODER

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	90	3,840	2%	
Logic Distribution				
Number of occupied Slices	48	1,920	2%	
Number of Slices containing only related logic	48	48	100%	
Number of Slices containing unrelated logic	0	48	0%	
Total Number of 4 input LUTs	90	3,840	2%	
Number of bonded IOBs	78	97	80%	
Total equivalent gate count for design	636			
Additional JTAG gate count for IOBs	3,744			

RTL SCHEMATIC FOR PROPOSED DECODER



UGC Approved Journal

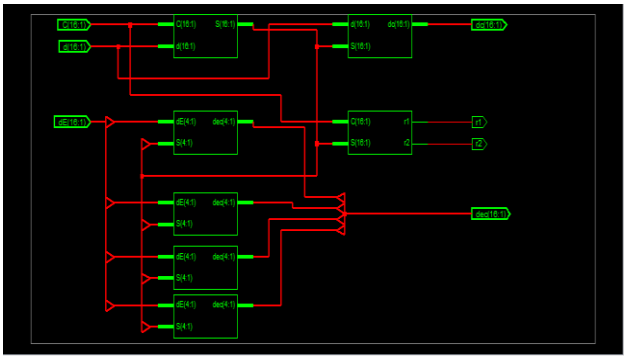
IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 6, June 2017



COMPARISON TABLE

	Area in Number of LUT		Delay		
Method Name	**LUT**	**Gate Count**	**Delay**	**Gate or Logic Delay**	**Path or Route Delay**
Proposed Encoder	32	323	7.165ns	6.364ns	0.801ns
Modified Encoder	32	192	10.764ns	7.567ns	3.197ns
Proposed Decoder	90	895	13.221ns	8.478ns	4.743ns
Modified Decoder	90	636	13.259ns	8.478ns	4.781ns

V. CONCLUSION

In this paper, two techniques to derive Unequal Error Protection (UEP) codes from Double Error Correction (DEC) Orthogonal Latin Squares (OLS) codes have been presented. The derived UEP codes can protect part of the word with DEC and the other part with SEC-DED. The codes can be decoded in parallel with low latency. Finally they do not require any additional parity bits compared to a standard OLS code. The implementation results for an FPGA platform have confirmed the low complexity and latency of both the encoder and the decoder. Future work will consider the derivation of UEP codes from OLS codes that can correct more than two errors. For example a TEC OLS code can be extended to also provide DEC for additional bits. It would also be interesting to derive a formal and general proof of the UEP capabilities of the proposed codes that does not rely on a case by case analysis and exhaustive error pattern testing.

REFERENCES

[1] N. Kanekawa, E. H. Ibe, T. Suga and Y. Uematsu, "Dependability in Electronic Systems: Mitigation of Hardware Failures, Soft Errors, and Electro-Magnetic Disturbances", Springer Verlag, 2010.
[2] T.Heijmen, "Soft Errors from Space to Ground Historical Overview," Soft Errors in Modern Electronic Systems, Springer, 2011.
[3] M. Nicolaidis, "Design for soft error mitigation", IEEE Trans. on Device and Materials Reliability, vol. 5, no. 3, pp. 405–418, Sept. 2005.
[4] A. DeHon, N.Carter, H.Quinn, "Final Report for CCC Cross-Layer Reliability Visioning Study", Computing Community Consortium, http://www.cra.org/ccc/xlayer.php.
[5] G.C. Cardarilli, M. Ottavi, S. Pontarelli, M. Re and A. Salsano, "Fault tolerant solid state mass memory for space applications", IEEE Trans. Aerosp. Electron. Syst., vol. 41, no. 4, pp. 1353-1372, Oct. 2005.
[6] W. K. Huang, Y.-N. Shen, and F. Lombardi, "New approaches for the repairs of memories with redundancy by row/column deletion for yield enhancement," IEEE Trans. Computer-Aided Des. Integr. Circuits Syst., vol. 9, no. 3, pp. 323–328, Mar. 1990.
[7] C. L. Chen and M. Y. Hsiao, "Error-correcting codes for semiconductor memory applications: a state-of-the-art review", IBM J. Res. Develop., vol. 28, no. 2, pp. 124-134, Mar. 1984.
[8] E. Fujiwara, "Code Design for Dependable Systems: Theory and Practical Application", John Wiley & Sons, Inc., 2006.
[9] M.Y. Hsiao "A class of optimal minimum odd-weight column SEC-DED codes", IBM J. Res. Develop.,vol. 14, no. 4, pp. 395–301, Jul. 1970.
[10]E. Ibe, H. Taniguchi, Y. Yahagi, K. Shimbo and T. Toba, "Impact of scaling on neutron-induced soft error rate in SRAMs From a 250 nm to a22 nm Design Rule", IEEE Trans. on Electron Devices, vol. 57 , no. 7, pp. 1527-1538,July2010.
[11] S. Lin and D. J. Costello, "Error Control Coding" (2nd Ed.), Englewood Cliffs, NJ: Prentice-Hall. 2004.