



A Novel VLSI Design of Hybrid Carry Skip Adder Implementation based on Verilog HDL

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Abstract: This paper, we present a carry skip adder (CSKA) structure that has a higher speed yet lower energy consumption compared with the conventional one. The speed enhancement is achieved by applying concatenation and incrementation schemes to improve the efficiency of the conventional CSKA (Conv-CSKA) structure. In addition, instead of utilizing multiplexer logic, the proposed structure makes use of AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates for the skip logic. The structure may be realized with both fixed stage size and variable stage size styles, wherein the latter further improves the speed and energy parameters of the adder. Finally, a hybrid variable latency extension of the proposed structure, which lowers the power consumption without considerably impacting the speed, is presented. This extension utilizes a modified parallel structure for increasing the slack time, and hence, enabling further voltage reduction. We will implement 8 Bit, 16 Bit, and 32 Bit Existing and Proposed adders. Now we are proposing a Real time Digital Counter or Clock Circuits using our proposed carry-skip adder. The proposed structures are assessed by comparing their speed, power, and energy parameters with those of other adders design by Verilog HDL and Simulated by Modelsim 6.4 c and Synthesized by Xilinx tool and proposed system implemented in FPGA Spartan 3 XC3S 200 TQ-144.

Index Terms: Carry skip adder (CSKA), energy efficient, high performance, hybrid variable latency adders, voltage scaling.

I. INTRODUCTION

The ever increasing demand for mobile electronic devices requires the use of power efficient VLSI circuits. Computations in these devices need to be performed using low power, area efficient circuits operating at greater speed. Addition is the most basic arithmetic operation; and adder is the most fundamental arithmetic component of the processor. Adders are key building block in arithmetic and logic units (ALUs) and hence increasing their speed and reducing their power/energy consumption strongly affect the speed and power consumption of processors. There are many works on the subject of optimizing the speed and power of these units, which have been reported in obviously, it, is highly desirable to achieve higher speeds at low power/energy consumptions, which is a challenge for the designers of general purpose processors. One of the effective techniques to lower the power consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the switching energy on the voltage and addition to the knob of the supply voltage, one may choose between different adder structures/families for optimizing power and speed. There are many adder families with different delays, power consumptions, and area usages. Examples include ripple carry adder (RCA), carry increment adder (CIA), carry skip adder (CSKA), carry select adder (CSLA), and parallel prefix adders (PPAs). The descriptions of each of these adder architectures along with their characteristics may be found in [6]. The RCA has the simplest structure with the smallest area and power consumption but with the worst critical path delay.

II. RELATED WORK

A simple strategy for the design of a single-level CSKA. The method is based on the VSS technique where the near-optimal numbers of the FAs are determined based on the skip time (delay of the multiplexer), and the ripple time (the time required by a carry to ripple through a FA). The goal of this method is to decrease the critical path delay by considering a non integer ratio of the skip time to the ripple time on contrary to most of the previous works, which considered an integer ratio. In all of the works reviewed so far, the focus was on the speed, while the power consumption and area usage of the CSKAs were not considered. Even for the speed, the delay of skip logics, which are based on multiplexers and form a large part of the adder critical path delay, has not been reduced.

Conventional structure of the CSKA

Complex layout

Large power consumption and area usage

Critical path delay, has not been reduced



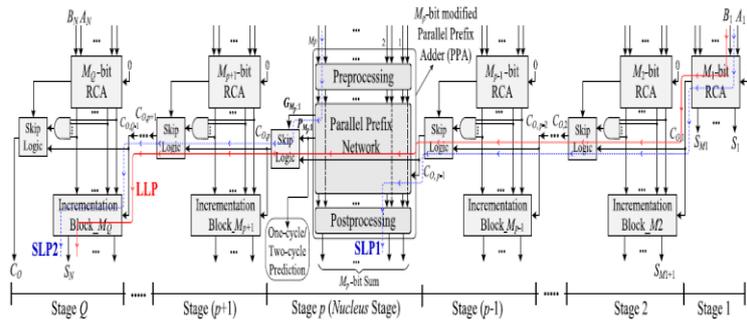
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III. PROPOSED SYSTEM

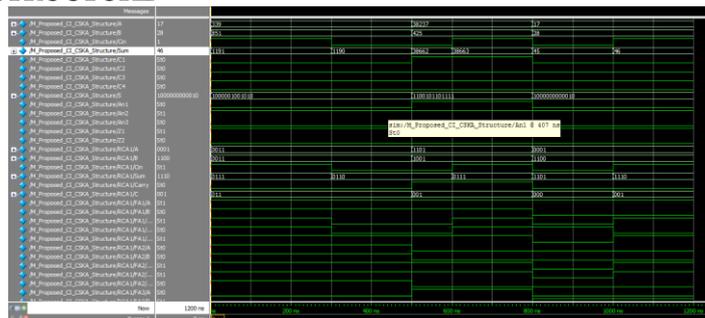
Proposing a modified CSKA structure by combining the concatenation and the incrementation schemes to the Hybrid CSKA (Hybrid-CSKA) structure for enhancing the speed and energy efficiency of the adder. The modification provides us with the ability to use simpler carry skip logics based on the AOI/OAI compound gates instead of the multiplexer. Providing a design strategy for constructing an efficient CSKA structure based on analytically expressions presented for the critical path delay. Investigating the impact of voltage scaling on the efficiency of the proposed CSKA structure. Proposing a hybrid variable latency CSKA structure based on the extension of the suggested CSKA, by replacing some of the middle stages in its structure with a PPA, which is modified in this paper.



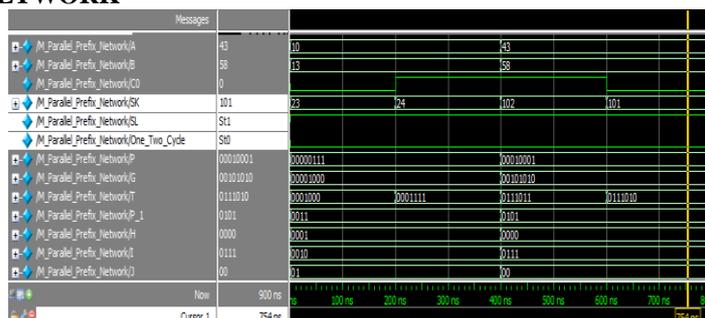
The adder contains two N bits inputs, A and B, and Q stages. Each stage consists of an RCA block with the size of M_j ($j = 1, \dots, Q$). In this structure, the carry input of all the RCA blocks, except for the first block which is C_i , is zero (concatenation of the RCA blocks). Therefore, all the blocks execute their jobs simultaneously. In this structure, when the first block computes the summation of its corresponding input bits (i.e., S_{M1}, \dots, S_1), and C_1 , the other blocks simultaneously compute the intermediate results [i.e., $\{ZK_{j+M_j}, \dots, ZK_{j+2}, ZK_{j+1}\}$ for $K_j = j-1$ $r=1$ M_r ($j = 2, \dots, Q$)], and also C_j signals. In the proposed structure, the first stage has only one block, which is RCA. The stages 2 to Q consist of two blocks of RCA and incrementation. The incrementation block uses the intermediate results generated by the RCA block and the carry output of the previous stage to calculate the final summation of the stage.

IV. RESULT ANALYSIS

PROPOSED CI-CSKA STRUCTURE



PARALLEL PREFIX NETWORK



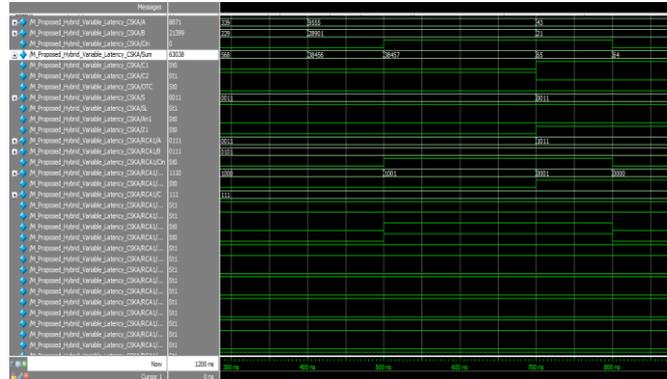


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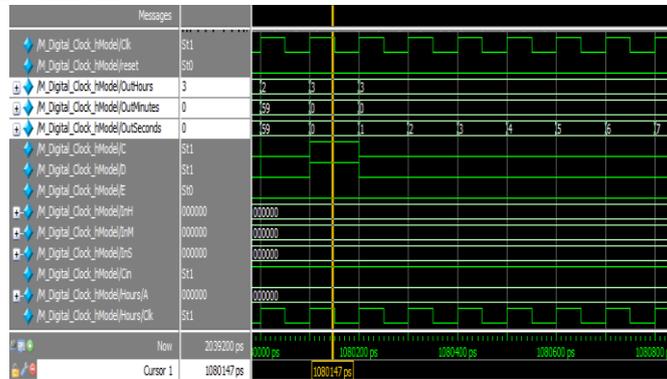
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PROPOSED HYBRID VARIABLE LATENCY CSKA

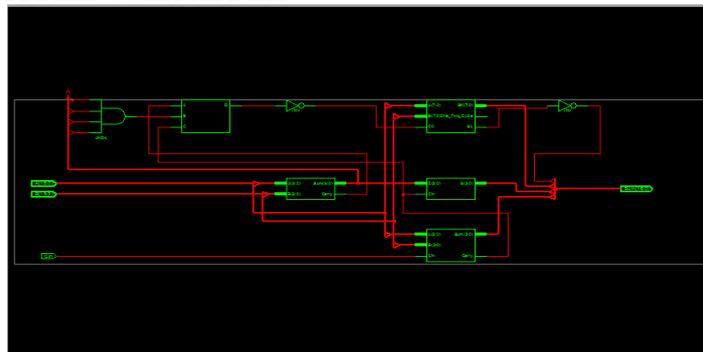


APPLICATION DIGITAL WATCH



V. SYNTHESIS RESULTS

RTL SCHEMATIC OF HYBRID CSKA ADDER



TECHNOLOGY DIAGRAM





AREA DELAY COMPARISON

Method name	Area in number of LUT			Memory in kilobytes	Delay		
	LUT	Gate count	Slices		Delay	Gate delay	Path delay
Conventional structure of the CSKA	44	264	26	176936	40.262ns	17.485ns	22.777ns
Proposed CSKA Structure	49	294	29	177512	23.461ns	11.975ns	11.486ns
Proposed Hybrid Variable Latency CSKA	47	297	27	177512	22.888ns	11.975ns	10.913ns

VI. CONCLUSION

A static Hybrid CSKA structure called HY-CSKA was proposed, which exhibits a higher speed consumption compared with those of the conventional one. The speed enhancement was achieved by modifying the structure through the concatenation and incrementation techniques. In addition, AOI and OAI compound gates were exploited for the carry skip logics. The results revealed considerably lower PDP for the VSS implementation of the CI-CSKA structure over a wide range of voltage from super-threshold to near threshold. The results also suggested the CI-CSKA structure as a very good adder for the applications where both the speed and energy consumption are critical. It exploited a modified parallel adder structure at the middle stage for increasing the slack time, which provided us with the opportunity for lowering the energy consumption by reducing the supply voltage. The efficacy of this structure was compared versus those of the variable latency RCA, C2SLA, and hybrid C2SLA structures. Again, the suggested showed the lowest delay and PDP making itself as a better candidate for high-speed low-energy applications.

REFERENCES

- [1] I. Koren, *Computer Arithmetic Algorithms*, 2nd ed. Natick, MA, USA: A K Peters, Ltd., 2002.
- [2] R. Zlatanovici, S. Kao, and B. Nikolic, "Energy-delay optimization of 64-bit carry-lookahead adders with a 240 ps 90 nm CMOS design example," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 569–583, Feb. 2009.
- [3] S. K. Mathew, M. A. Anders, B. Bloechel, T. Nguyen, R. K. Krishnamurthy, and S. Borkar, "A 4-GHz 300-mW 64-bit integer execution ALU with dual supply voltages in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 44–51, Jan. 2005.
- [4] V. G. Oklobdzija, B. R. Zeydel, H. Q. Dao, S. Mathew, and R. Krishnamurthy, "Comparison of high-performance VLSI adders in the energy-delay space," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 6, pp. 754–758, Jun. 2005.
- [5] B. Ramkumar and H. M. Kittur, "Low-power and area-efficient carry select adder," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 2, pp. 371–375, Feb. 2012.
- [6] M. Vratonjic, B. R. Zeydel, and V. G. Oklobdzija, "Low- and ultra low-power arithmetic units: Design and comparison," in *Proc. IEEE Int. Conf. Comput. Design, VLSI Comput. Process. (ICCD)*, Oct. 2005, pp. 249–252.
- [7] C. Nagendra, M. J. Irwin, and R. M. Owens, "Area-time-power tradeoffs in parallel adders," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 43, no. 10, pp. 689–702, Oct. 1996.
- [8] Y. He and C.-H. Chang, "A power-delay efficient hybrid carrylookahead/ carry-select based redundant binary to two's complement converter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 1, pp. 336–346, Feb. 2008.
- [9] C.-H. Chang, J. Gu, and M. Zhang, "A review of 0.18 μm full adder performances for tree structured arithmetic circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 6, pp. 686–695, Jun. 2005.
- [10] D. Markovic, C. C. Wang, L. P. Alarcon, T.-T. Liu, and J. M. Rabaey, "Ultralow-power design in near-threshold region," *Proc. IEEE*, vol. 98, no. 2, pp. 237–252, Feb. 2010.
- [11] R. G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, "Near-threshold computing: Reclaiming Moore's law through energy efficient integrated circuits," *Proc. IEEE*, vol. 98, no. 2, pp. 253–266, Feb. 2010.
- [12] S. Jain et al., "A 280 mV-to-1.2 V wide-operating-range IA-32 processor in 32 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb. 2012, pp. 66–68.
- [13] R. Zimmermann, "Binary adder architectures for cell-based VLSI and their synthesis," Ph.D. dissertation, Dept. Inf. Technol. Elect. Eng., Swiss Federal Inst. Technol. (ETH), Zürich, Switzerland, 1998.
- [14] D. Harris, "A taxonomy of parallel prefix networks," in *Proc. IEEE Conf. Rec. 37th Asilomar Conf. Signals, Syst., Comput.*, vol. 2, Nov. 2003, pp. 2213–2217.
- [15] P. M. Kogge and H. S. Stone, "A parallel algorithm for the efficient solution of a general class of recurrence equations," *IEEE Trans. Comput.*, vol. C-22, no. 8, pp. 786–793, Aug. 1973.