UGC Approved Journal

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 7, July 2017

A low cost Self-Driven Synchronous rectification Converter for 20V Portable Instrument

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Abstract: This paper presents an optimized and enhanced DC-DC converter design for 20V output for portable instrument application. The proposed design is based on isolated push pull topology switched mode power supply. Self-driven synchronous rectification (SDSR) is introduced in the rectification stage in order to create an improved way of rectifying process. N-Channel and P-Channel MOSFETs are used to simplify the synchronous rectification control circuit. Both MOSFETs offer ultra low On-resistance which can be used to achieve higher efficiency than the conventional converter. This converter operates at high speed switching frequency to gain high power-to-volume ratio. In addition, minimum deadtime is set in the design to ensure high efficiency in input-output power transfer. Passive low pass filter is implemented to produce ripple free output voltage in the design. The finalize topology which is push pull with self-driven synchronous rectification is constructed using simple control circuit but maintains good efficiency in its operation. Experimental results show that the proposed converter reacts very well with the self-driven synchronous rectification method. Input voltage is set at 12V and switching frequency is set at 30 kHz in order to minimize the switching stress and conduction losses. Practical implementation of the converter shows that the converter operates at a maximum efficiency of 84.1% and only produces 50mVp-p ripple output voltage which is considered good for a regulated DC output.

Keywords: Self-driven synchronous rectification, SDSR, SMPS, MOSFETs, deadtime, regulated DC output.

I. INTRODUCTION

DC-DC conversion is a process to convert a DC input voltage to another level of DC output voltage usually at a different level than the input. With different conversion technique, output voltage can be customized from as small as few volts to as high as kilovolts. Basically, DC-DC conversion is not as simple as the idea of converting a level of DC input voltage to another DC output voltage level. The conversion process needs good integration between input stage, input-output isolation stage and the output stage. Input stage consists of input power circuit and drive control usually implemented by high frequency technique. Input-output isolation is made of high frequency transformer and the output stage consists of rectifying and filtering circuit. If any of these parts cannot integrate harmoniously, the conversion process will not operate as desired.

Another factor that influences the performance and cost of a DC-DC converter is the component selection. Semiconductor industry offers a lot of discrete devices to be used in DC power supply design. Depending on the desired design characteristic, usage of higher rating and well protective component such as transistor brings extra cost to the production. For isolated topologies which have included the use of magnetic elements, the selection of core material and type will also determine the performance of the DC-DC conversion process. Nowadays, with the advanced in semiconductor industry, there is practical method to provide an efficient, controllable, and fast operation DC power supply due to the present of high switching operation, great noise isolation and well regulated bus voltage output.

In SMPS, basically there are two types of topologies which are non-isolated and isolated topologies. Basic topologies in the non-isolated topology are buck, boost, buck-boost and cuk converter while for isolated family, there are flyback, half-bridge, full-bridge and push-pull converter. Each topology has its own plus and minus criteria and different topology comes with different characteristic. For instance, one topology has low parts count and cost but only capable of handling limited amount of power while another has relatively higher parts count and cost but capable of handling much higher output power. In addition, another important parameter need to be determined also is the efficiency. Therefore, identity of each topology does not resemble the weakness of the design but it can encourage researchers to improve and redesign new converter based on the basic topology.

Recent development in SDSR topologies [1-10] obviously implementing N-Channel MOSFETs for the power switches and the synchronous rectification (SR) switches. Besides, isolated topologies with symmetrical transformer characteristic such as half-bridge, full-bridge and push-pull are also the preferred choice for the SDSR topology. The transformer associated with these topologies can react very well with the deadtime adjustment. Therefore, SR circuit

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Vol. 5, Issue 7, July 2017

consists of N-Channel and P-Channel MOSFET combined with an isolated topology such as push-pull is most suitable for a new SR converter design. N-Channel and P-Channel MOSFET can be used side by side because secondary side of a chopper transformer generates positive and negative voltage waveforms relative to each other, so the complexity of the SR control circuit can be reduced significantly with the using of both MOSFETs. Frequency operation should be below 100 kHz to reduce switching stresses.

II. PRINCIPLE OF OPERATION

In this design, the proposed topology uses 12V input voltage switched at 30kHz. Isolation is performed using push pull transformer and the output voltage at the secondary side is stepped up to 20V.
The synchronous rectification (SR) circuit is divided into two subcircuits namely SR1 and SR2. SR1 consists of Q1 and Q2 while SR2 consists of Q3 and Q4. Q1 and Q3 are P-Channel type while Q2 and Q4 are N-Channel type and all of them are enhancement mode MOSFETs. SR1 is triggered by Self-driven1 signals while SR2 is triggered by Self-driven2 signals. Fig. 1 shows the proposed push pull with self-driven synchronous rectification topology.

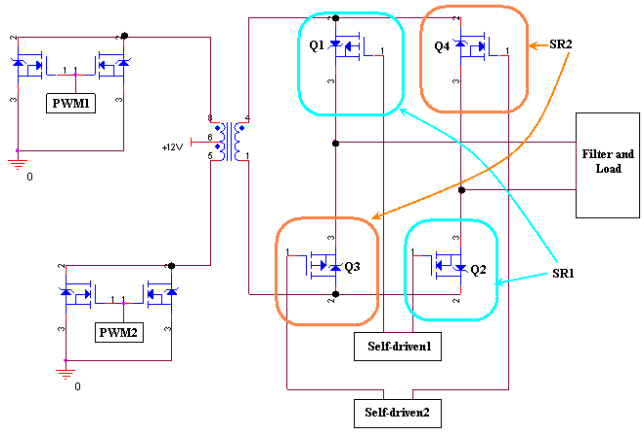

Fig. 1 Push Pull with Self-driven Synchronous Rectification (SDSR) circuit.

Basically, the arrangement of the SR MOSFETs uses similar concept like inverter. Unlike inverter that allows bidirectional current path through the load, combination of N-Channel and P-Channel is implemented to achieve unidirectional current path. Moreover, with non centre tapped secondary winding transformer, this rectification can be easily done and simplicity in the SR circuit is highly expected. The key to allow unidirectional path lies with MOSFET's internal body diode. At initial conduction point when gate-to source voltage is below the threshold value, the current is channeled through the body diode. The conduction is strictly limited within the deadtime period introduced earlier in the transformer secondary winding waveform. After the threshold value is reached, MOSFETs will be turned ON and current will flow through them. In order to maintain the same current direction, MOSFETs are configured to be reversed to achieve the unidirectional path. As a result, current is forced to flow from source to drain in N-Channel whereas for P-Channel, current is forced from drain to source.

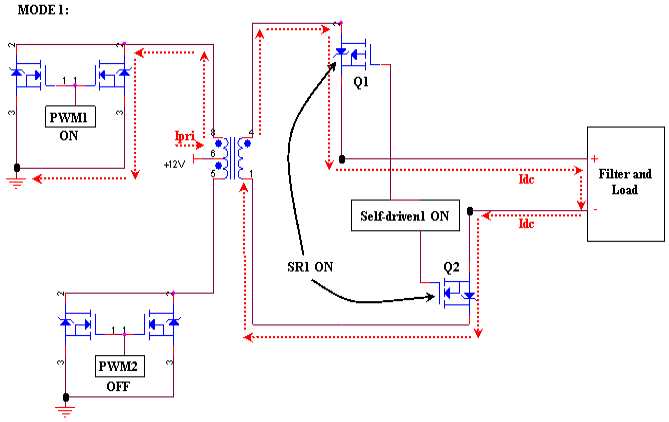

Fig. 2 SR mode 1 operation.

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There are two modes involved in the SR operation. From Fig. 1, SR1 is controlled by the Self-driven1 signals and SR2 by the Self-driven2 signals. At any time, only one SR conducts. For example, SR1 conducts in the first half cycle and SR2 conducts in the next half cycle and that completes the full cycle operation. This arrangement also prevents short circuit in the SR circuit. Fig. 2 and Fig. 3 show the SR operation in mode 1 and mode 2 respectively. Mode 1 is the operation when SR1 is ON and mode 2 is when SR2 is ON.

In mode 1, secondary transformer terminal 4 has positive voltage with respect to terminal 1. During operation when Self-driven1 is off, current initially flows from terminal 4 to Q1's body diode then to load and finally through Q2's body diode back to terminal 1. After a very short deadtime period, Self-driven1 is ON triggering Q1 and Q2 to fully ON. Current then flows through Q1 and Q2. As a result, positive DC voltage is generated in the half cycle operation of SR at load.

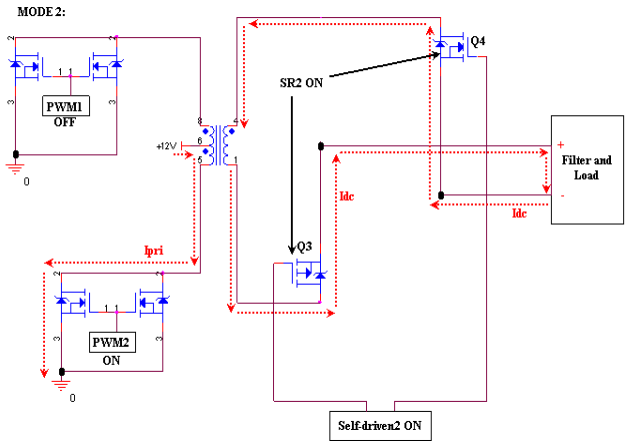

Fig. 3 SR mode 2 operation.

In mode 2, transformer terminal 1 has positive voltage with respect to terminal 4. When Self-driven2 is off, current will flow from Q3's body diode to load and finally through Q4's body diode back to transformer terminal 4. After a short deadtime, Self-driven2 is ON. Q3 and Q4 will fully ON allowing current flows through them. Positive DC voltage is generated in similar direction with mode 1 at load and completes the full cycle operation. This process periodically repeats and ensures constant positive polarity DC output voltage at load. Fig. 4 shows the ideal timing for the complete SR operation in full cycle.

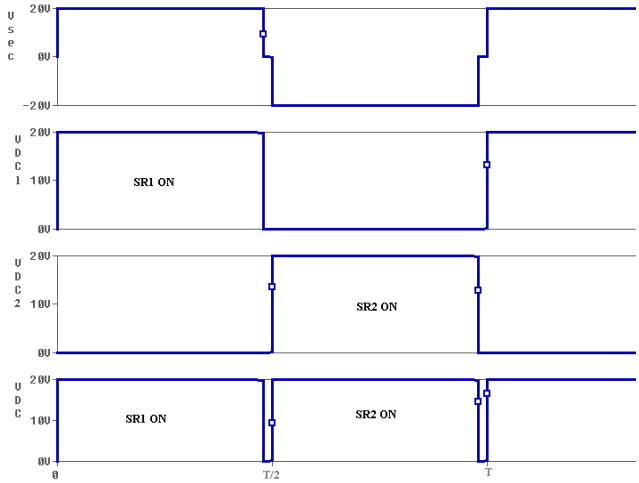

Fig. 4 Ideal timing for SDSR circuit

V_{sec} is the AC voltage generated at the secondary side of the push pull transformer shown in Fig. 1. V_{DC1} is the DC output voltage generated at load when SR1 is ON in mode 1. V_{DC2} is the DC output voltage generated at load when SR2 is ON in mode 2. V_{DC} is the actual DC voltage seen at load in full cycle before any filtering is applied.

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III.DESIGN AND CONSTRUCTION OF SDSR CIRCUIT

Conventional rectification using diode generates higher loss especially in low output voltage power supply. Synchronous rectification is proved to be very suitable to overcome that problem. Also with higher switching operation, there is no doubt that SR is the best choice.

For this design that uses 20V as output voltage and 30 kHz as operating frequency, synchronous rectification (SR) is chosen as the best rectification method. The suitable SR control technique for this low output voltage is a self-driven control. No extra winding is used in the SR control circuit making it the best and simplest way of controlling the SR switches. Referring to Fig. 1, the SR control circuit is simplified using Self-driven1 and Self-driven2.

For SR1 to conduct, Self-driven1 must be ON and also for SR2 to conduct, Self-driven2 must be ON. In this design, each SR circuit has a combination of N-Channel and P-Channel MOSFET. Therefore, each self-driven control has two different gate signals. One signal to drive the N-Channel MOSFET and another signal to drive the P-Channel MOSFET. N-Channel works with positive gate drive while P-Channel works with negative gate drive. Corresponding to Fig. 2 and Fig. 3 respectively, Q1 and Q3 need negative drive while Q2 and Q4 need positive gate drive.

Table 1 shows the drive characteristics for both self-driven signals.

Table 1 Drive characteristics for Self-driven1 and Self-driven2

	Negative Drive	Positive Drive
Self-driven1	Q1	Q2
Self-driven2	Q3	Q4

At any time during half cycle conduction, one terminal in the transformer secondary side is always positive with respect to the other terminal. Thus, positive and negative drive waveforms can be easily obtained from the transformer. A simple voltage divider circuit can be used to allow the self-driven synchronous rectification conduction.
In this design, IRFZ340N is used for N-Channel MOSFET while IRF9530N is used for P-Channel MOSFET. Table 2 shows the differences between the two MOSFETs.

Table 2 Enhancement mode N-Channel and P-Channel MOSFET comparison

	IRFZ34N	IRF9530N
MOSFET type	N-Ch	P-Ch
Static drain-to-source On-resistance, $R_{ds(on)}$	0.040Ω	0.200Ω
Threshold gate voltage, $V_{gs(th)}$	4V	-4V
Maximum gate-to-source voltage, V_{gs}	20	-20V

Fig. 4 shows the ideal secondary AC voltage waveform, V_{sec}. This waveform have +20V and -20V that can be used to drive the N-Channel and P-Channel MOSFET respectively. Ideally, the waveform can be fed directly to the MOSFETs gate but in reality, condition such as spike may deny the direct feeding.

From Table 2, voltage above 4V should be applied to N-Channel and -4V to P-Channel to bypass the threshold voltage. Any voltage between 4.1V to 20V and -4.1V to -20V can be used to fully ON the N-Channel and P-Channel respectively. In this design, the gate-to-source maximum voltage is set to 10V for N-Channel and -10V for P-Channel. For gate saturation, a maximum of 15mA is enough and the divider resistor can be calculated.

Gate-to-source divider resistor, R_{gs} value is given by,

$$R_{gs} = R = \frac{10}{(15m)} = 667\Omega$$

However, 560Ω is used due to available practical value. For a better clamp voltage, zener diode is placed in parallel with R_{gs}. Fig. 5 shows both self-driven control circuits in the SR topology.

For complete operation, Self-driven1 will trigger SR1 (Q1,Q2) in first half cycle while Self-driven2 will trigger SR2 (Q3,Q4) for the other half cycle.

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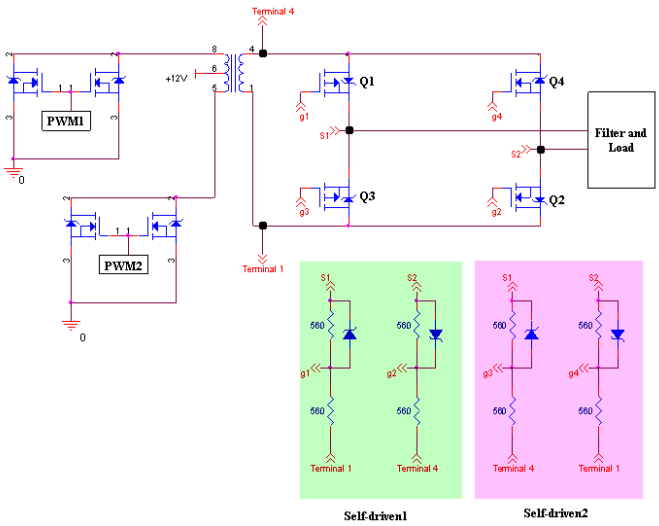

Fig. 5 Self-driven control circuits in SR topology.

Fig. 6 shows the complete circuit of the proposed push pull with SDSR topology design. This complete circuit integrates all parts which are power switches and drive control, chopper transformer, SDSR and low pass filter.

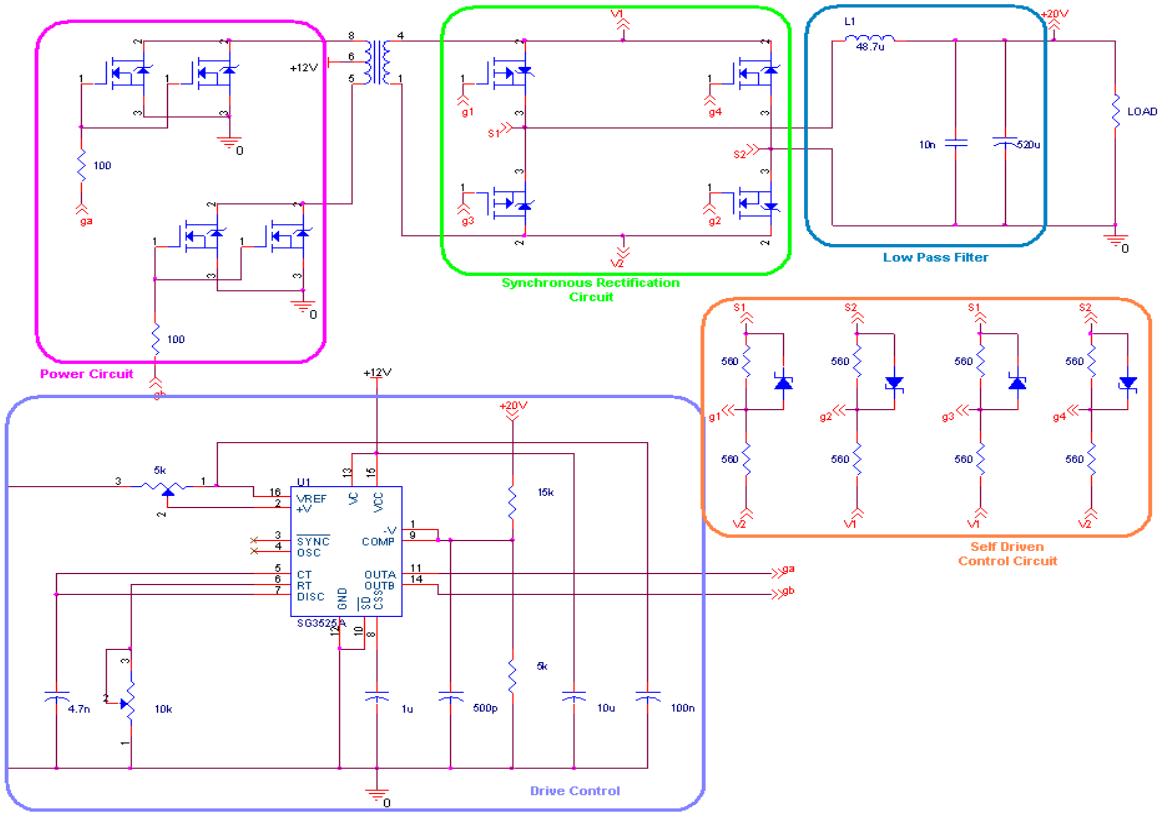

Fig. 6 Complete circuit of the proposed SDSR

IV. EXPERIMENTAL RESULTS

The gate drive control signals for driver circuit are generated from commercial IC SG3525A. Using this IC, the switching frequency is set to 30 kHz with duty cycle limited to 48% for half cycle. This is the typical value recommended by the manufacturer to be used in designing DC-DC converter using this voltage control mode IC. The 2% margin is used for the deadtime period in order to avoid any simultaneous conduction in the power circuit conduction during push and pull conduction. Each MOSFET has its own rise and fall times. If the duty cycle is set

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nearly to the ideal value which is 50%, there is large possibility of short circuit in all MOSFETs during transition period. Besides, the duty cycle also should not set below 45% for half cycle because with the decreasing of the duty cycle value resulting in lower performance of the DC-DC converter. Therefore, the appropriate value should be considered accurately to realize a high performance DC-DC converter.

Fig. 7 shows the driver control signals where a 12V, 30kHz smooth pulse voltage are generated from the IC. The signals are applied to g_a and g_b of the power switches. In order to limit the fast transient response surging to the gate, gate resistor is added in series with the gate terminal with 100Ω value. Fig. 8 shows the gate-source voltage, Vgs applied at the power circuit MOSFETs.

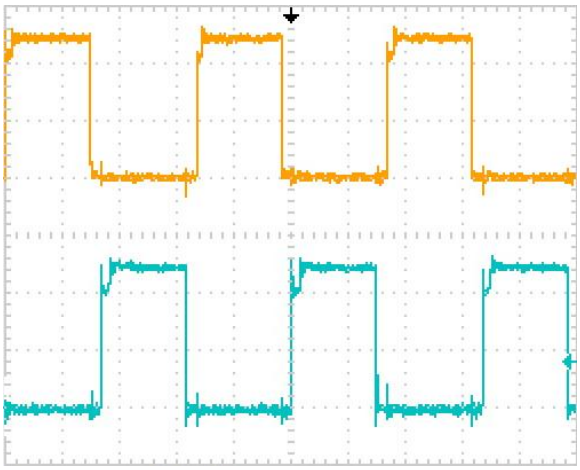

Fig. 7 Control drive signals for both legs in power circuit.
(Scales: 5V/div; 10μs/div).

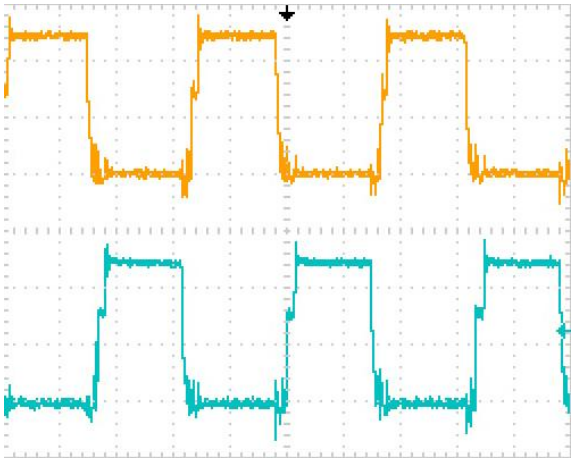

Fig. 8 Control drive signals with gate resistor added.
(Scales: 5V/div; 10μs/div).

Fig. 9 shows the control signals side by side. Deadtime was introduced in the signals and the power circuit should operate without short circuit occurrence.

Fig. 10 shows the voltage waveforms at the primary side of the chopper transformer. Although two N-Channel MOSFETs are enough for the push-pull conduction, but to minimize the switching losses and stresses endured by the switching devices under high frequency operation, each leg has two set of MOSFETs in parallel to divide the stresses equally as shown in Fig. 6.

AC waveforms generated have some spiking when the MOSFET is turned ON. Clearly, the amplitude of the AC waveforms is equal to the input voltage.

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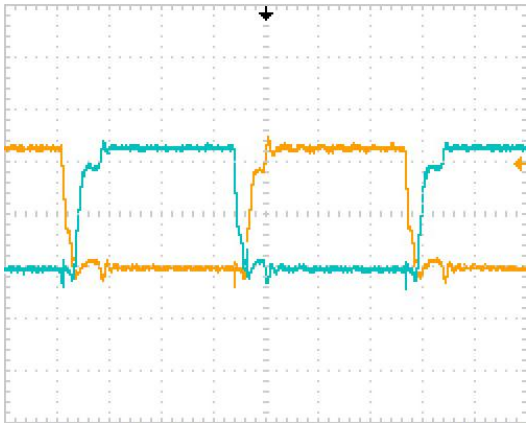

Fig.9 Vgs for both power drive MOSFETs.
(Scales: 5V/div; 5µs/div).

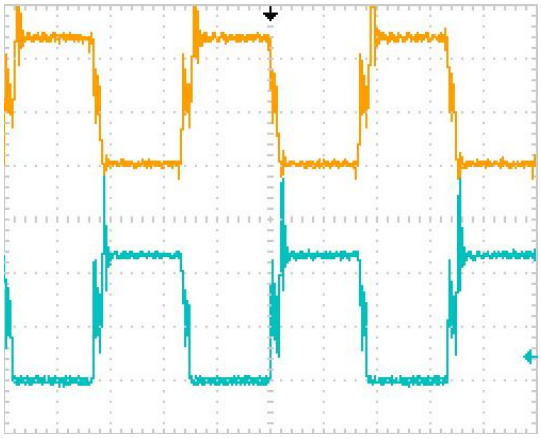

Fig. 10 AC waveforms of both primary windings in chopper transformer. (Scales: 5V/div; 10µs/div).

Fig. 11 shows the AC waveforms of the secondary side chopper transformer. The (a) figure shows the secondary waveforms relative to each other. Basically, these are the waveforms that will be fed to the gate control of the SDSR control circuit. Again, the importance of the deadtime is really needed here to make sure the SDSR control circuit did not overlapping with each other during the switching transition between MOSFETs in the SR control circuit. From the (b) figure, deadtime is visible during the on-off switching transition. This is the combined secondary waveforms of the chopper transformer. The output voltage has 22V peak amplitude with significant spiking.

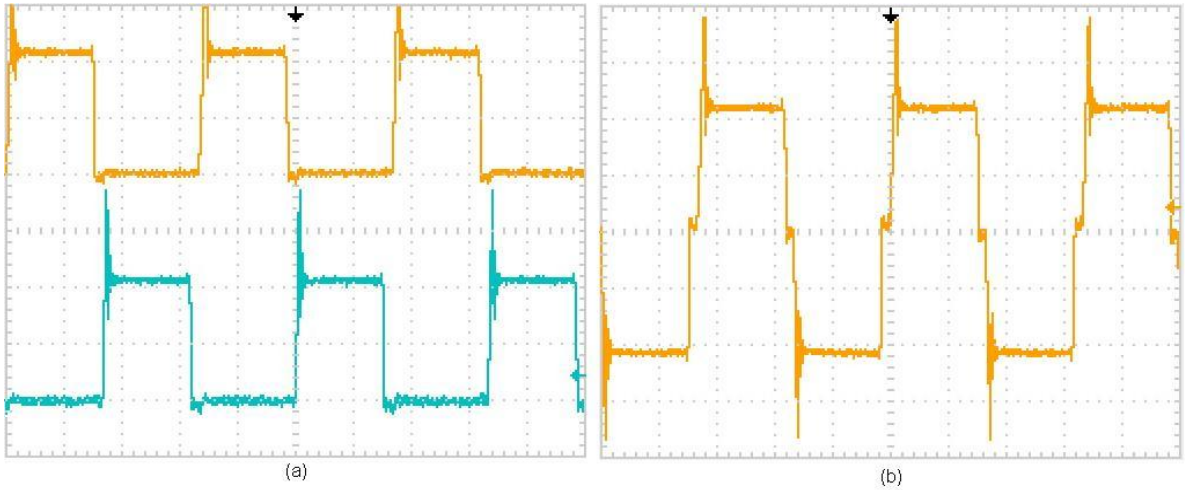

Fig. 11 (a) Output waveforms at the secondary side in relative to each other (b) Combined secondary AC voltage waveform. (Scales: 10V/div; 10µs/div).

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Fig. 12 shows the DC output voltage before and after filtering stage. Figure (a) shows the DC output with double rectification using SR. The rectified DC output waveform fairly has no drop compared with the amplitude of the AC waveform from the secondary side chopper transformer. It is verified that the SDSR technique is really reliable in producing output waveform with no loss at all.
Figure (b) shows the regulated DC voltage after filtering using low pass filter without any surge or any disturbances at all. Apparently, right selection of switching MOSFETs rating briefly above the output voltage rating is enough to make a reliable design without the use of snubber circuit. More protection scheme to the design introduces more cost and may lower overall efficiency because extra components are needed to set up the extra circuit.

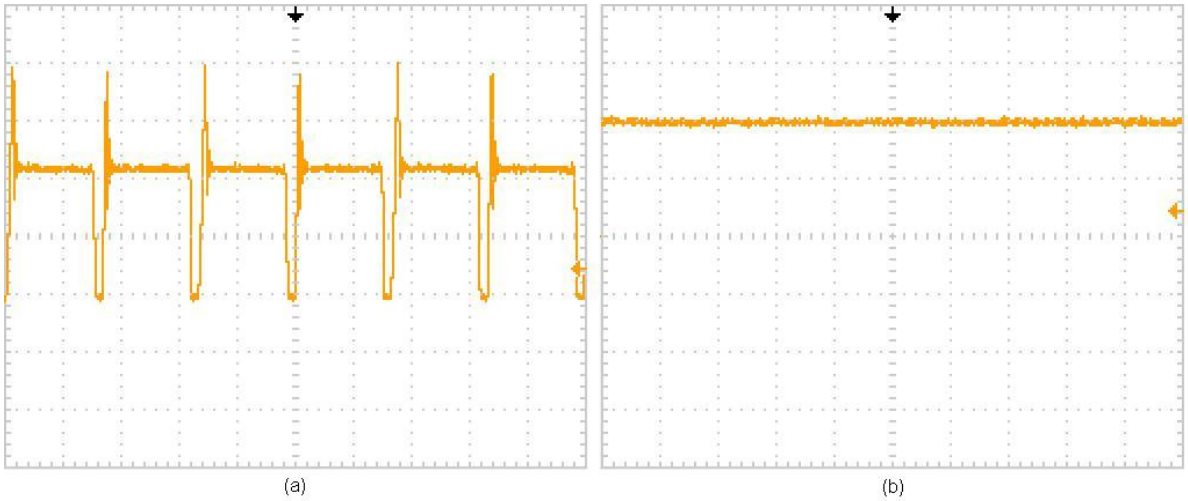

Fig. 12 (a) DC output waveform before filtering
(b) DC output waveform after filtering. (Scales: 10V/div; 10µs/div).

Fig. 13 shows the peak to peak ripple of the DC output waveform. The peak to peak ripple of the output waveform is approximately $50mV_{p-p}$ and considered small for a regulated DC output.

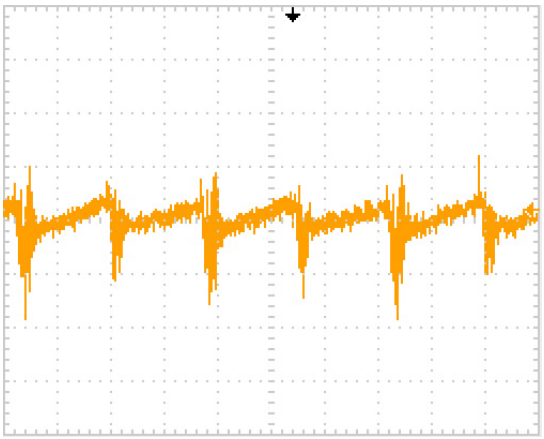

Fig.13 Peak to peak ripple waveform of the DC output voltage.
(Scales: 50mV/div; 10µs/div).

The proposed prototype is tested using 60W resistive load. Measurement result shows that the efficiency achieved by the proposed design is 84.1% at the operating frequency of 30 kHz.

V. CONCLUSION

The study focuses on the design of a DC-DC converter with synchronous rectification (SR) method for low voltage application. The drive control scheme for the converter is based on the voltage mode control generated from commercial IC in the drive circuit. Self-driven synchronous rectification consists of MOSFETs is used in the rectifying stage. In this design, combination of N-Channel and P-Channel MOSFETs are used to simplify the SR circuit.

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However, this technique is valid for non centre tapped secondary side transformer only. Once the system is built and the initial tests are performed, they demonstrate that the proposed design achieves 84.1% efficiency at 30 kHz frequency. SR control circuit is found to be very simple when only potential divider is implemented to realize it. The constructed converter also has low DC output voltage ripple which is below 1% indicating good regulated DC output. Overall, this DC-DC converter has simple switching technique with reliable and efficient SR control circuit for low voltage application.

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BIOGRAPHIES

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