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# Cascade H-Bridge Multilevel Inverter Fed Induction Motor Drive

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**Abstract:** Here in the proposed work the main focus is done on FFT analysis of output voltage of cascade H-bridge multilevel inverter employing selective harmonic elimination method. In selective harmonic elimination, a particular order of harmonic is selected and based on it, width of pulse is decided so that output voltage will be free from that harmonic[1]. Also focus is done on improving the efficiency of the multilevel inverter and quality of output voltage waveform. Selective Harmonics Elimination method is used to reduce the Total Harmonics Distortion (THD) value and to eliminate the lower order harmonics[2]. This topology is suitable for any number of levels. It reduces cost and complexity hence it is opt for industrial applications. In this paper fifth and seventh harmonics have been eliminated. Simulation work is done using the MATLAB software and experimental results have been presented to validate the theory.

**Keywords:** CHBMLI, SHE, Induction Motor.

## 1. INTRODUCTION

Multilevel inverters are DC to AC power conversion systems composed of an array of power semiconductors and capacitive voltage sources that, when properly connected and controlled[3], can generate a multi-step voltage waveform with variable and controlled frequency, phase and amplitude. The stepped waveform is synthesized by selecting different voltage levels generated by the proper connection of the load to the different capacitive voltage sources. This connection is performed by the proper switching of the power semiconductors[4]. The number of levels of inverter can be defined as the number of steps or constant voltage values that can be generated by the inverter between the output terminal and any arbitrary internal reference node within the converter.

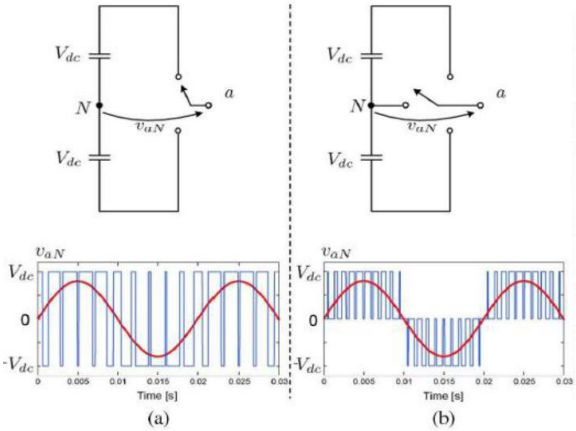


Fig 1 Output voltage waveform of (a) two-level inverter (b) three-level inverter

Typically, it is a dc-link node, and it is usually denoted by 'N' called neutral. To be called a multilevel inverter, each phase of inverter has to generate at least three different voltage levels. This differentiates the classical two-level voltage source inverter (2L-VSC) from the multilevel inverter family. The concept showing the difference in Waveform and circuit diagram between two-level and three-level inverter are shown in figure below

It is worth mentioned that, generally different voltage levels are equidistant from each other in multiples of $V_{dc[5]}$.

There are many ways to combine power semiconductors and capacitive DC sources to generate multilevel output voltages. However, only some of them have become important from a practical point of view, and these are analyzed in the following section.

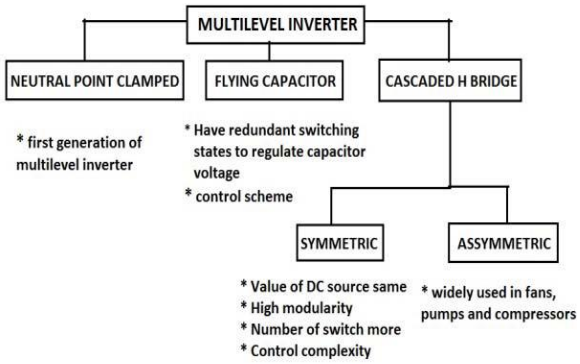


Fig 2: Types of multilevel inverter

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The development of multilevel inverters over the last decades has matured into three widely accepted topologies:

1) Neutral-point clamped (NPC) or diode clamped (DC),
2) Flying capacitor (FC)
3) Cascade H-bridge inverter

In the proposed work, only Cascade H-bridge multilevel inverter is described in detail.

## 2. CASCADE H-BRIDGE MLI TOPOLOGY

A cascaded type multilevel inverter consists of series connection of full H-bridge inverter units. The general function of this multilevel inverter is to synthesize desired ac output voltage from several Separate DC Sources (SDCS), which may be obtained from batteries, fuel cells or solar cells. The ac output voltage obtained from MLI is in the form of steps so here steps are specified in term of levels. In m-level MLI of cascade bridge type, (m-1)/2 units of full H-bridge inverters are required for each single phase unit[6].

Here m = number of levels in phase to ground ac output voltage of multilevel inverter.

Each full bridge inverter requires one dc source and four IGBTs with feedback diodes. So for five levels, two units of full bridge inverters are required, with total number of eight switches per phase.

In this inverter topology all the switches are switched at fundamental frequency which causes low switching losses due to which it shows more reliability and feasibility. Fig 3 shows the structure of a three-level cascaded inverter with SDCS. Each SDCS is connected to an H-bridge inverter[7].

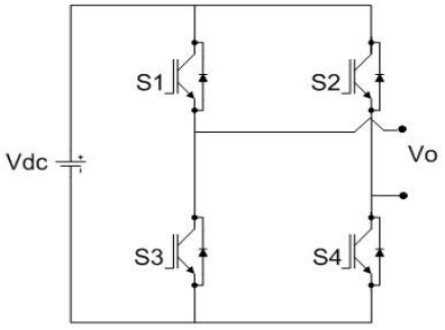


FIG:3 Three-Level cascade H-Bridge MLI

Table1: switching pattern of CHB MLI

| Output Voltage $V_o = V_{AN}$ | Switch states | | | |
|---|---|---|---|---|
| | $S_1$ | $S_2$ | $S_3$ | $S_4$ |
| $V_{dc}$ | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| | 0 | 0 | 1 | 1 |
| $-V_{dc}$ | 0 | 1 | 1 | 0 |

The output terminals of various full bridge inverters are connected in series to make stepped AC output voltage. Unlike the diode-clamped or flying capacitors inverter, the cascaded inverter does not require any voltage-clamping diodes or voltage-balancing capacitors.

## 3. PROPOSED METHODOLOGY

**Selective harmonic elimination (SHE) in cascade H-bridge multilevel inverter:**

In selective harmonic elimination method, there are some particular order of harmonics of output voltage of MLI are selected, according to the order of harmonics the correct instant of switching of any switch of particular single phase full bridge inverter is decided by following equations[8].

For eliminating $5^{th}$ and $7^{th}$ order harmonics from seven-level inverter, which employ three full bridge inverters,

$$\cos\alpha + \cos\beta + \cos\Upsilon = 0.8 * 3 \quad (1)$$
$$\cos 5\alpha + \cos 5\beta + \cos 5\Upsilon = 0 \quad (2)$$
$$\cos 7\alpha + \cos 7\beta + \cos 7\Upsilon = 0 \quad (3)$$

Here $\alpha < 90$, $\beta < 90$, $\Upsilon < 90$,

By some iteration in MATLAB, the switching angles for 7-level cascaded H-bridge multilevel inverter are calculated.

$$\alpha = 11.5^o, \quad \beta = 28.71^o, \quad \Upsilon = 57.1^o$$

However if we require to change the magnitude and frequency of output voltage of MLI employing SHE[9], then magnitude of output voltage cannot be changed, because width of pulse is fixed as per the elimination of particular order of harmonic using SHE. The frequency of output voltage can be changed by varying explicit period.

## 4. SIMULATIONS AND RESULT

The simulation if three phase seven level cascade H-bridge MLI fed induction motor was done using matlab.

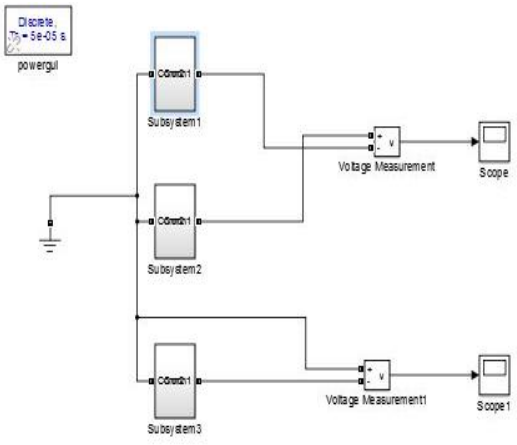


Fig 4: Simulation diagram for seven-level inverter


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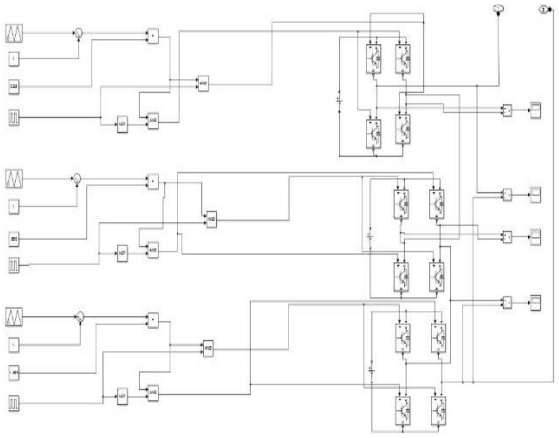

Fig 5: Control strategy for phase A of seven-level inverter

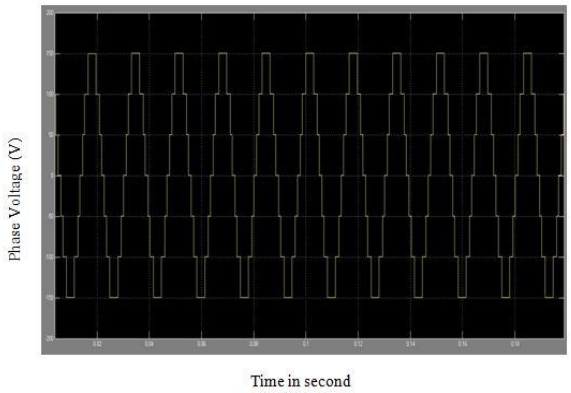


Fig 6 Output phase to neutral voltage waveform of seven-level inverter

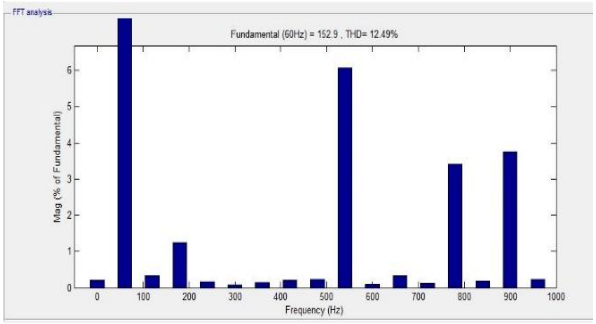


Fig 7 FFT analysis of phase to neutral voltage waveform of seven-level inverter

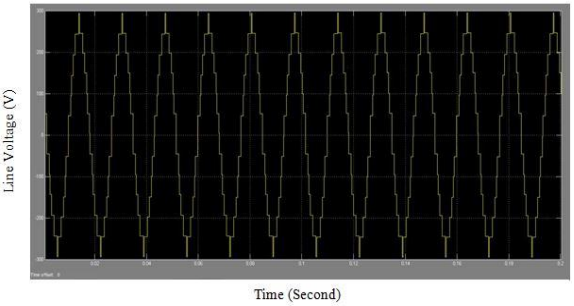


Fig 8 Output line-line voltage waveform of seven-level inverter

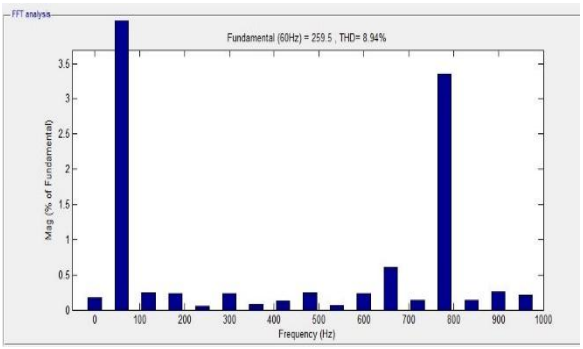


Fig 9 FFT analysis of line to line voltage waveform of seven-level inverter

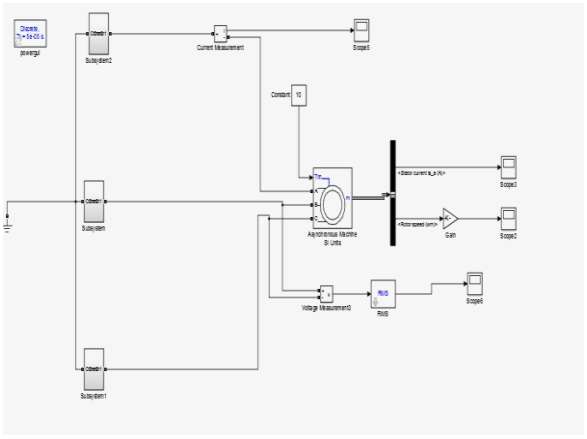

Fig 10: Simulation diagram for seven-level inverter fed induction motor drive

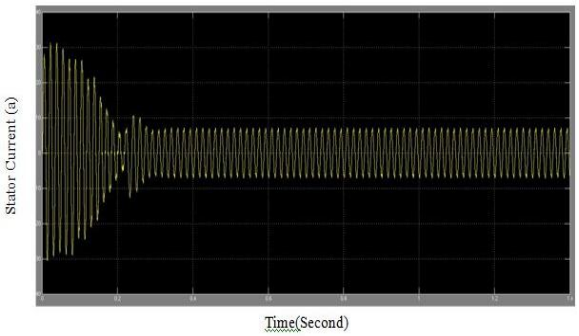


Fig 11 waveform of stator current of three phase induction motor

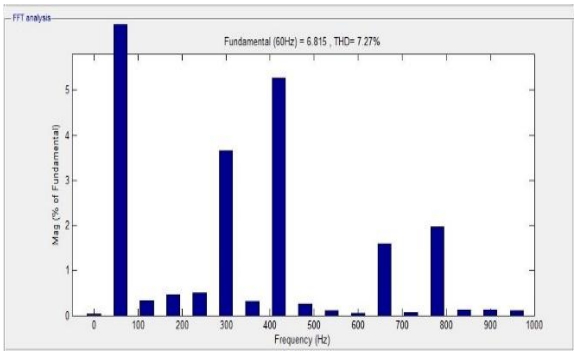


Fig 12 FFT analysis of stator current of three phase induction motor


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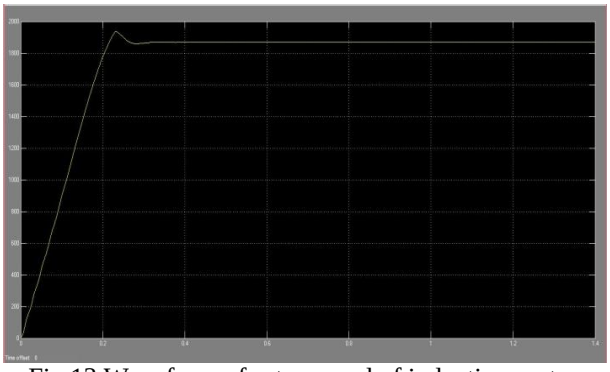

Fig 13 Waveform of rotor speed of induction motor

## 5. CONCLUSION

In FFT analysis of multi-level inverter, the control strategy for all the switches is made by using Matlab. In this method, pulse width of output voltage of full bridge inverter is decided by the order of harmonic, which has to be removed from output voltage of MLI. So here magnitude of output voltage can only be controlled by external circuitry. In the proposed scheme THD of line-line voltage of 8.94% can be obtained. A generalized control strategy is made by using Matlab with the help of which multi-level inverter of any level can be made.

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