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Implementation of Memory for Industrial Applications: A Comparative Study

Shrunkhala Naik[1], Sonia Kuvelkar[2], Jan Gunke[3]

Master of Engineering, Microelectronics ETC Department, Goa College of Engineering, Ponda, India [1]

Assistant Professor, ETC Department, Goa College of Engineering, Goa University, Ponda, India [2]

Head of Architecture & Innovation Department R&D Siemens Ltd, Verna, India[3]

Abstract: Industrial applications require non volatile memory for long term storage of critical data such as configuration data, parameters and the device firmware. To serve this purpose, most devices are equipped with a SD card. However, in certain applications, it is beneficial to replace this SD card with a non-replaceable memory. In this work, a detailed study of memory technologies and the different ways in which they can be interfaced with a device was performed. The results are supported by a comparative study as well as behavioural simulations.

Keywords: Flash, MRAM, FRAM, Verilog

I. INTRODUCTION

Industrial devices require a non-volatile storage device for long-term storage of recorded information and parameters required for configuration. The most common used storage device is a SD card. At times, a device may have to be removed for testing purpose. In such cases, the SD card stores the parameters so that the device can be re-configured. SD card allows a simple plug-and-play process, thus adding functional flexibility to the device.The SD cards are generally industrial or commercial grade cards hence are expensive as compared to the consumer grade cards. Some applications require a low-cost way rather than a flexible solution, to store the data. In such cases the SD card can be replaced with a non-volatile, non-replace-able memory. This study shows how non-volatile memories can be used as substitute for SD cards. The second section explains about the memory structures and interfaces. The third section shows a comparison between the different memories. The fourth section summarizes the pros and cons of each implementation. The paper is concluded with the conclusion and references

II. MATERIALS AND METHODS

A. Flash [1]

i) Cell Structure:

The cell structure of today's flash memories is based on the floating gate (FG) technology. As shown in the figure 1, the structure is similar to a MOS transistor with the only major difference being the additional gate. This additional gate, known as the floating gate, is electrically isolated by the surrounding oxide. Thus, any electrons placed on it are retained for a number of years. The external gate, known as the control gate, is the contact terminal for the gate voltage (V_g). The injection or removal of electrons from this floating gate modifies the threshold voltage (V_{th}) of the cell. The following table summarizes the operation:

Operation	Electrons in FG	FG state	V_{th}	Current flow on application of a fixed voltage V_g	Cell state	Bit stored
Program	Injected	Charged	Higher than normal	No	Off	0
Erase	Removed	Discharged	normal	Yes	On	1

Table 1: Flash memory operation

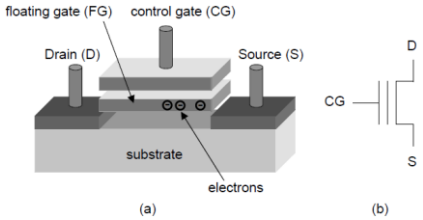

Figure 1: Flash memory cell

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Since the storage mechanism is based on charging, there is a tendency of leakage after a certain number of electron injections and removals. Thus, the number of times the flash cell can be reliably programmed and erased is limited.
In the early days of its introduction, flash memory was used to store only one bit per cell. However with the advancement in scaling, the number of bits per cell is ever-increasing. This work considers the single-level cell (SLC) and Multi-level cell (MLC). The increase in cell density increases the susceptibility to data corruption since the same voltage band has to accommodate the increasing number of bits per level. This decreases the voltage gap between each level thus making it more vulnerable to errors.

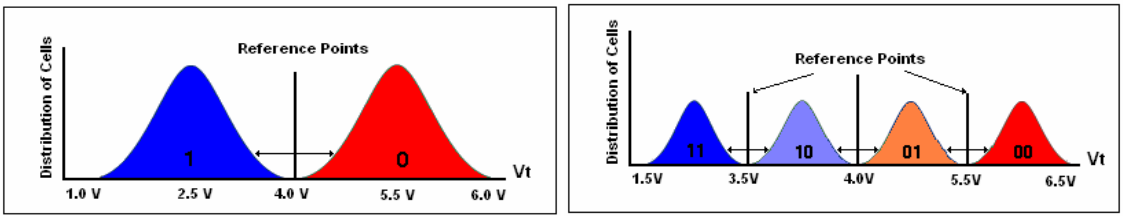

Figure 2: MLC v/s SLC NAND Flash

Hence, retention, endurance and reliability are major issues pertaining to flash memories.

ii) Interface:
When an external memory device is interface with the host system, the host processor expects a hard disk drive (HDD). HDDs are physically divided into sectors, each of 512B. However the construction of a flash device differs from that of a HDD i.e. instead of sectors, a flash memory unit is made up of pages, blocks and planes. Therefore, a sector access by the host must be translated into a page access on the flash. This is done by a Flash translation layer (FTL) i.e. FTL that maps the logical to physical addresses. FTL can be implemented on a memory controller or on the host as a part of firmware or in-built controller [1].

One drawback of Flash memory is that a cell cannot be over-written instead has to be erased before it is programmed. Moreover, it has limited number of Program-erase cycles per block and once a block has reached the limit it can no more store data and is termed as bad block. When 70-80% of the blocks reach the limit the device fails. Thus, in the absence of any lifecycle management mechanisms, the device will fail much earlier. The device endurance can be increased by implementing life cycle management mechanisms such as ECC, Bad block management and wear levelling. Over the years, as the oxide around the FG experiences fatigue i.e. the charge leakage exceeds the tolerable levels, multiple read errors tend to occur. In these conditions, it is crucial to have a mechanism that can detect and correct the errors. Error correction code (ECC) encodes data in such a way that a decoder can identify and correct errors in the data. Thus flash device require a controller that is capable of implementing an efficient ECC algorithm. This minimizes possible errors and helps to extend the lifetime of the memory device.

In write-intensive applications, where-in data writes occur more often than reads, it is possible that a particular block is written more number of times than the other blocks. Since every write is accompanied by an erase, if this erase pattern continues that particular block will fail earlier than other blocks. Thus, a situation is possible where 70% of blocks have failed while the remaining 30% are unused. This will reduce the overall endurance of the device and cause it to fail earlier than expected. Hence, it is critical to spread the writes over the entire flash device. This is done by a scheme called wear leveling where blocks of static data are swapped with blocks containing data often updated. This further has two schemes: Static, Dynamic and Global. It has to be implemented by the controller. Hence, a flash memory can be interfaced only if the above functions are implemented on a controller or are a part of the firmware running on the host processor.

B. MRAM [2]
i) Cell Structure:
The element responsible for charge storage in a magnetic random access memory is a magnetic tunnel junction (MTJ). An MTJ is made up of two magnetic storage elements, one with a fixed magnetic polarity and other with a variable polarity, separated by a thin insulating material. To read the state of the cell, current is passed through it and the electrical resistance across the MTJ is measured. If the magnetic moments in each of the elements are parallel, the cell resistance is low and the electrons are able to tunnel through the barrier.

If the magnetic moments are anti-parallel, the MTJ resistance is high thus, preventing the electron tunnelling. A low resistance indicates 'ON' state while high resistance indicates 'OFF' state.

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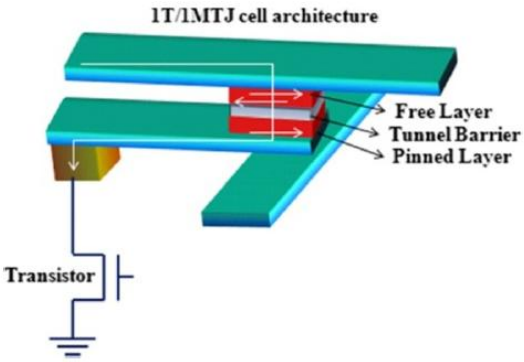

Figure 3: MRAM memory cell

ii) Interface:

MRAM is available as serial and parallel interface. The serial interface MRAM can be connected to an SPI port while the parallel interface is pin-to-pin compatible with asynchronous SRAM interface. Thus MRAM can be interfaced via SPI interface or an asynchronous SRAM interface, both of which require minor changes to the host firmware.

C. FRAM [2]

i) Cell Structure:

A Ferromagnetic random access memory cell is similar to a dynamic random access memory cell where-in the leaky capacitor in the DRAM structure is replaced with a ferroelectric capacitor in FeRAM. The cell stores bits based on the polarization properties of the ferroelectric substance i.e. lead zirconate titanate (PZT) and these bits are read by sensing the ferroelectric state of the capacitor. Positive polarization corresponds to state '1' while negative polarization indicates state '0'.

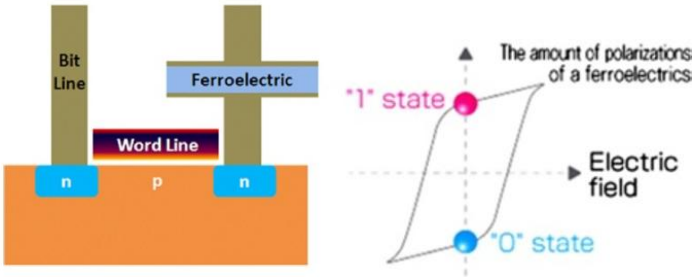

Figure 4: FeRAM memory cell & hysterisis loop

ii) Interface:

FRAM is available with serial or parallel interface. Hence it can be interfaced to the host via a SPI port or asynchronous SRAM interface. Unlike MRAM, a few points have to be taken care of while interfacing it to an SRAM interface. They are as follows:

- Confirm CE operation-

In SRAM, chip enable (CE) is an active low signal that has to be driven low in order to latch a new address at the beginning of every read/write cycle. For the subsequent address bus changes, the CE signal can remain low. However this is not true for FeRAM. In case of FeRAM, the address bus changes for every memory access require a corresponding falling edge of the CE signal. Thus, unlike SRAM, it is not allowed to ground the CE pin.

- Supply voltage levels-

In case of a battery backed SRAM, it is necessary to check VDD levels to switch to battery supply. When VDD levels drop beyond certain values, the user accesses are normally blocked so as to not drain the battery unnecessarily. Since FeRAM is a non-volatile storage, it does not require any monitoring. Thus, this provision need not be provided in the FRAM design. Nonetheless, as a common design practice, the processor must be reset when VDD drops below certain levels so as to prevent memory accesses in this situation.

Following is a Verilog simulation of F-RAM FM28V102A (1Mbit F-RAM Memory) device which indicates the toggling of CE during write operation.

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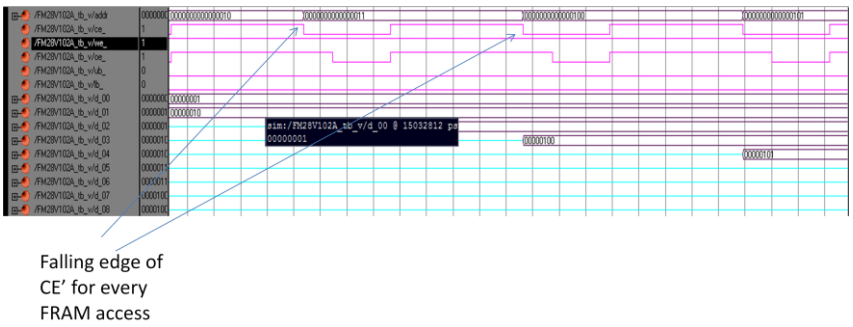

Figure 5: Verilog simulation for FRAM memory

III. COMPARISON

Industrial applications require high-endurance, reliable, cost-efficient memory that is easy to implement. The following table summarizes the comparison with respect to these requirements. The values are obtained from an electronic distributor called digikey [3]. The memory chips chosen for comparison are Micron 4GB SLC Flash, Micron 4GB MLC Flash, Micron 2Gb NOR flash, Everspin 16Mb MRAM, Cypress 4Mb FRAM.

	SLC NF	MLC NF	NOR Flash	MRAM	FRAM
R/W Endurance	100K	10k	1000K	Unlimited	10^12
Retention (years)	10	10	10	>20	10
Capacities available	512 Gbit	2 Tbit	2Gbit	64 Mbit	8 Mbit
Cost/chip	$28/ 4GB	$4/ 4 GB	$17/2Gb	$23-39/ 16 Mb	$11-14 / 4 Mb
File management required	Yes	Yes	Yes	No	No
Ease of Implementation	Requires a dedicated controller to implement FTL and Lifecycle management functions			Requires minor FW changes	Requires FW changes

TABLE 1: COMPARISON OF THREE MEMORIES WITH RESPECT TO INDUSTRIAL REQUIREMENTS

IV. RESULTS AND DISCUSSION

This section highlights the pros and cons of using each memory for an application and the interfaces that it can be connected to.

Table 2: Summary of pros and cons of each memory

Memory	Pros	Cons	Interface
Flash	-lowest cost for a given chip density - highest available capacity	-Lifecycle management functions required - intelligent hardware controller required -Increases cost and board area	SD/SPI/ asynchronous SRAM
FRAM	High endurance	-Not suitable for high density applications - High cost per chip -burdens host firmware for timing compatibilities	asynchronous SRAM
MRAM	-Unlimited endurance -Minor firmware adaptations	-Not suitable for high density applications -High cost per chip	asynchronous SRAM

V. CONCLUSION

In this work, three main non volatile memories were studied to evaluate their fitness for industrial applications. This study also includes the method to interface each of these to the host device and also summarizes the pros and cons of each memory and its implementation.

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