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Area and Delay Efficient DSP Architecture

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Abstract: An area and delay efficient Digital Signal Processor (DSP) system is proposed in this paper. The proposed system implements Fast Fourier transform, correlation and convolution on a single platform. For implementing a system with reduced area and delay, a modified carry look ahead adder and array multiplier has been utilized. This complete DSP system is described using VHDL and is synthesized by using Xilinx synthesis tool. The Fast Fourier Transform (FFT) is one of the rudimentary operations in the digital signal and image processing field. Some of the very vital applications of the fast Fourier transform include Sound filtering, Partial differential equations, Signal analysis, Data compression, Image filtering ,Multiplication etc. Fast Fourier transform (FFT) is an highly efficient implementation of the Discrete Fourier Transform (DFT). This paper concentrates on the implementation of the Fast Fourier Transform (FFT), based on Decimation-In-Time (DIT) domain by using Radix-2 algorithm. By utilizing a fixed geometry addressing, block fixed point structure and pipeline designing, the data will acquire higher precision and dynamic range. The results show that the design is strongly extensive, efficient and occupies little resource. This proves to be a good method to meet the digital signal processing requirements at high-speed. In this paper, we have extended the utility of the system towards convolution and correlation applications, which are the most important applications in digital signal processing.

Keywords: Digital signal processor (DSP), Fast fourier transform, Convolution, Correlation, Carry look ahead adder.

I. INTRODUCTION

A digital signal processor (DSP) system is a specialized microprocessor with an architecture optimized for the fast operational requirements of digital signal processing. Digital signal processing (DSP) has many advantages over analog signal processing. Digital signals are more robust when compared to analog signals with respect to process variations and temperature. Digital signal processing algorithms generally require a large number of mathematical operations to be performed quickly and simultaneously on a specified set of data. Signals are constantly converted from analog form to digital form, manipulated digitally, and then again converted back to analog form.

Most of the DSP applications have constraints on latency; that is, for the system to perform correctly, the DSP operation must be completed within some fixed amount of time, and deferred processing is not viable. Most of the general-purpose microprocessors and operating systems can successfully execute DSP algorithms, but are not viable to be used in portable devices such as PDAs and mobile phones because of space constraints and power supply limitations. A specialized digital signal processor will, however, tend to provide a low-cost solution, with lower latency and better performance, and no requirements for large batteries or specialized cooling.

The important features of DSP are: ability to perform Single Instruction Multiple Data (SIMD) operations, ability to perform DFT and FFT; that is, Discrete Fourier Transform and FFT Fast Fourier Transform [5], [6]. It can be implemented with embedded processors or in general purpose computers that may or may not include specialized microprocessors called digital signal processors. Digital Signal Processor (DSP) is optimized specially for digital signal processing. It also support features as microcontroller or an applications processor.DSP operations process the continuous signals and data. A DSP (Digital Signal Processor) system is a specialized microprocessor with an architecture developed for the fast operational needs of digital signal.

The proposed system performs three main signal processing applications: Fast Fourier Transform (FFT), Convolution and Correlation.

II. DSP ARCHITECTURE

The proposed DSP system architecture consists of four stages. It includes decoder, fetch machine, execution unit and register set. This system, in general performs the basic signal processing operations more efficiently. The DSP system architecture is shown in figure1.

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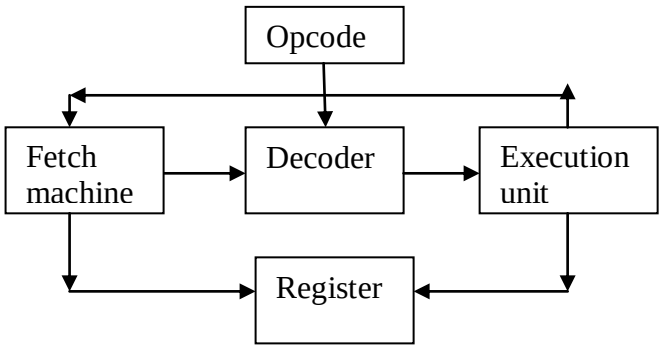

Fig. 1 DSP system architecture

Figure 1 shows the DSP system which is separated into several stages. The first stage is the fetch stage where an instruction is fetched from memory and as soon as the
instruction fetch cycle gets completed, this machine signals the decoder to decode the instruction. The next stage is the decoder where the decoder decodes the instruction upon completion of the instruction fetch cycle. The decoder reads bit 2 down to 0 of the IR, decides which of the three operations the CPU needs to perform, and signals one of the next stages to begin its operation. The next state is the execution unit where the signal processing operations are performed. The data is taken from four general purpose registers for convolution and correlation and from eight general purpose registers for fast fourier transform(FFT).After performing the operations, the result will be shown in output device.

III.INSTRUCTION SET

The DSP system performs three DSP operations. Each instruction is decoded by an internal decoder and the DSP machine fetches an instruction from the memory. In the proposed DSP system, a three bit opcode is used to allow system to perform various signal processing applications, that is, opcode specifies the intended operation to be performed.

TABLE I INSTRUCTION SET

Instruction	Opcode	Operation performed
FFT	000	Perform FFT operation
Convolution	001	Perform convolution operation
Correlation	010	Perform correlation operation

IV.DSP OPERATION

The proposed system is implemented to perform DSP applications like fourier transform, convolution and correlation. Here for convolution and correlation, we used general multiplication. Convolution [4] process is an integral concatenation of two signals which has many applications in numerous areas of signal processing. The most popular application of convolution is the determination of the output signal of a linear time invariant system (LTI) by convolving the input signal with the impulse response of the system. Convolving two signals in time domain is equivalent to the process of multiplying the Fourier transform of the two signals. In signal processing, cross-correlation is a measure of similarity of two signals as a function of a time-lag applied to one of them. This technique is also known as a sliding inner-product or sliding dot product. It is commonly used for searching a long-duration signal for a known, shorter feature. It also has applications in pattern recognition, single particle analysis, neurophysiology, cryptanalysis and electron tomographic averaging.

A. Fast Fourier Transform(FFT)

The Fourier Transform is the basis of many signal processing and communication applications. It is the analysis of the signal in its frequency domain. The Fourier transform has many applications, in field of physical science that uses sinusoidal signals, such as applied mathematics, engineering physics, and chemistry. Most of the fields nowadays make use of discrete and digital data. Thus the determination and evaluation of Fourier Transform of discrete signals is of prime importance .Such a transform is called Discrete Fourier Transform (DFT). The FFT algorithm eliminates the redundant calculation which is required in computing the Discrete Fourier Transform (DFT) and thus is very suitable for efficient and novel hardware implementation. In addition to the process of calculating efficient DFT, the FFT also

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finds applications in linear filtering, correlation analysis and digital spectral analysis. Fast Fourier Transform (FFT) is thus an efficient algorithm to evaluate DFT. Radix-2 Decimation-in-time (DIT) Fast Fourier Transform (FFT) is obtained by dividing the DFT into two portions. The Basic Butterfly operation of radix-2 DIT FFT algorithm of eight signals is shown in Fig 2. The mathematical equation representing discrete fourier transform is given as

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-j\frac{2\pi kn}{N}} \qquad (1)$$

where the value of k ranges from 0 to N-1. Discrete Fourier Transform(DFT),Fast Fourier Transform(FFT) are the DSP operations mentioned in this paper. The processor uses a kind of discrete transform that is used in Fourier analysis. This transforms one function into another, which is called simply the DFT or frequency domain representation of the original function whereas Fast-Fourier transform (FFT) is an efficient algorithm that quickly computes a DFT. The Radix-2 decimation-in-time (DIT) FFT divides the DFT into two portions. Figure 2.2 shows the Basic Butterfly4 operation of the Radix-2 DIT FFT algorithm of eight signals. The Fast Fourier Transform (FFT) has almost become ubiquitous and is most important in high speed signal processing. Using this particular transform, signals can be moved to the frequency domain where filtering and correlation can be performed with fewer operations .The implementation of fast fourier transform requires complex multiplication and additions. This increases the power of the system. However, this power can be reduced by using real-imaginary swapping and sign inversion. The power can further be reduced by using power efficient adders .Use of power efficient multipliers can enhance the functioning of fast fourier transform. In addition to computing DFT, the FFT also finds applications in linear filtering, correlation analysis and digital spectral analysis.

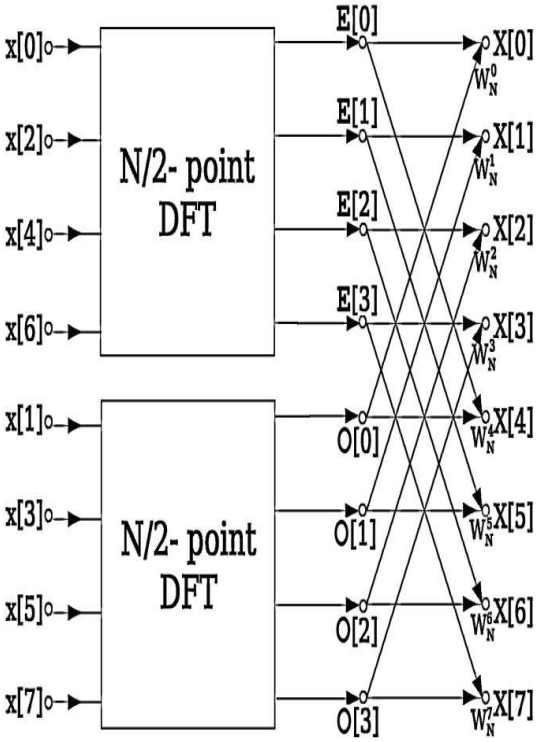

Fig. 2 Butterfly operation

B. Convolution

Convolution is concatenation of two signals. It is a mathematical operation just like addition and multiplication. Multiplication and addition takes two numbers as input and produces another number as output. Convolution, on the other hand, takes two signals as input and produces another signal as output. DSP processors basically depend on filtering applications that need circular convolution or linear convolution to be performed on inputs. The proposed system uses linear convolution. The linear convolution is a basic digital signal processing (DSP) operation which relates impulse response and input signal to obtain desired output. The behavior of a linear, time-invariant (LTI) discrete time system with x [n] as the input signal and an output signal y [n] is described by the convolution sum. It is denoted as y[n] = x[n] * h[n], where h[n] is the harmonic function. If x[n] is a finite length sequence of length N, and

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h[n] is a finite length sequence of length M, then the output of convolution operation y(n) contains N+M-1 number of samples. The formula for determining discrete linear convolution is

$$y(n) = \sum_{k=-\infty}^{\infty} x(k)h(n-k) \qquad (2)$$

In the proposed system, the two input sequences x (n) and h (n) consist of four samples each and hence, sixteen partial products are calculated and after this computation, they are added to get the final convolution sequence y[n]. In the proposed method, the partial products are calculated by using the Array multiplier. The multiplier required for this particular system is 4×4 bit. The output of each multiplier will be eight bits long. Thus, each sample in convolution output will have eight bits. Convolution outputs y [6] and y [0] are direct partial products.

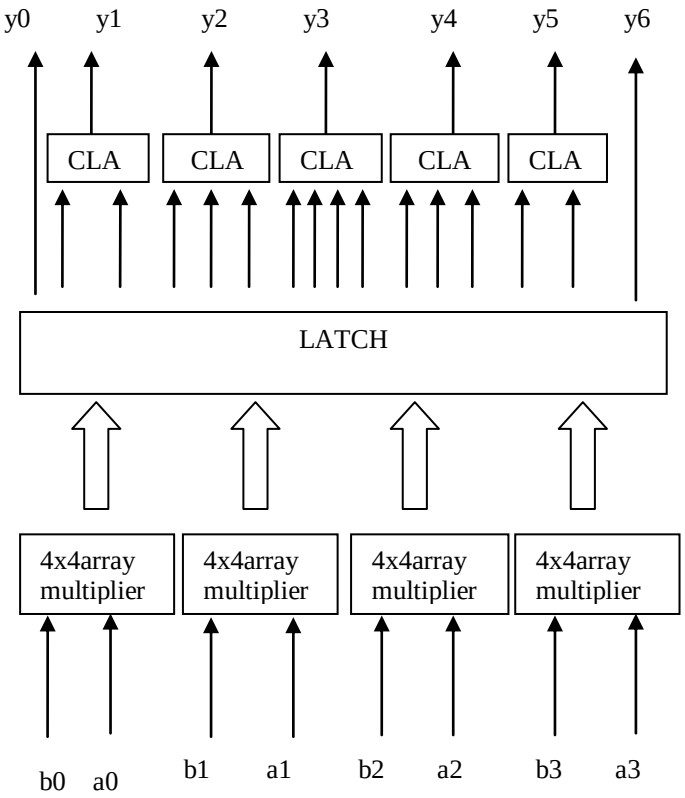

Fig. 3 Block diagram of convolution

In this paper, 4 × 4 convolution is implemented in order to reduce the cost. This can be extended for N × N convolution.
In this system, 4-bit long input samples are applied to 4x4 array multiplier. The output of each array multiplier is eight bit long. In order to perform further operation of addition, all outputs are latched using a d latch. To generate partial products y2, y3 and y4,carry look ahead adders(CLA) are used.

C. Correlation

Correlation is a measure of similarity between two signals. It is another mathematical operation just like convolution. There are two basic types of correlation: autocorrelation and cross-correlation. It is denoted as y[n] = x[n] * h[-n], where h[n] is a harmonic function. If x[n] is a finite length sequence of length N, and h[n] is a finite length sequence of length M, then the output of correlation operation y(n) contains N+M-1 number of samples.The general formula for correlation is

$$y(n) = \sum_{k=-\infty}^{\infty} x(k)h(k-n) \qquad (3)$$

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Cross-correlation is a measure of similarity between two waveforms as a function of a time-lag applied to one of them. In this paper, computation and evaluation of cross-correlation is done similar to that of the convolution using the direct method. The cross- correlation between two signals x (n) and h (n) means to convolve the reverse of h (n) with x(n). Auto-correlation is the cross-correlation of a signal with itself. It is defined as the similarity between the observations as a function of the time lag between them. Here only one sequence is given as input. Auto-correlation of x(n) means to convolve the sequence of x(n) with the reverse of x(n) itself.

V. SIMULATION RESULTS

The proposed DSP system design was simulated and synthesized using Xilinx Integrated Environment (ISE) version 14.7. Figure 4 shows the RTL schematic. Figure 5, 6 and 7 show the simulation results of FFT, convolution and correlation. In order to reduce the delay, various architectures have been proposed. Area and delay efficient DSP architecture is obtained by using modified carry look ahead adder and array multiplier. Table II shows the area and delay of the proposed architecture. Delay and power consumed has been reduced while comparing proposed with the existing method.

TABLE II Comparison of proposed method with existing

Design	Delay (ns)	Area (number of transistors used)
Design using Ripple carry adder and array multiplier	17.35	8928
Proposed Design	15.29	2304

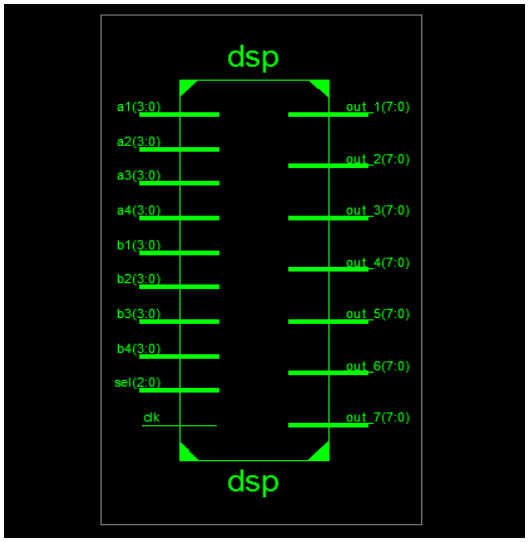

Fig. 4 RTL schematic of DSP system

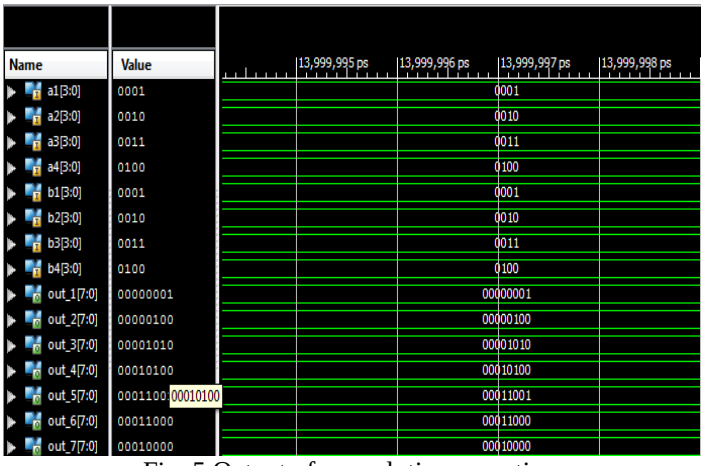

Fig. 5 Output of convolution operation

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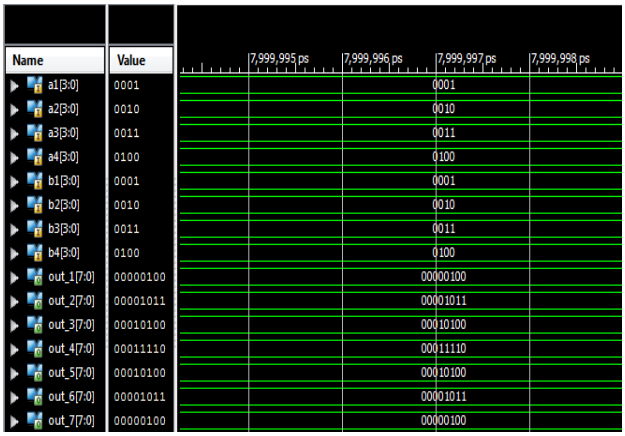

Fig.6 Output of correlation operation

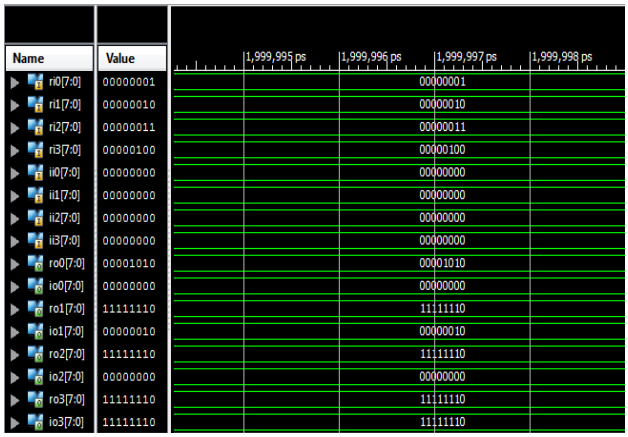

Fig. 7 Output of FFT operation

VI. CONCLUSION

The simulation results of the DSP system depict the proper functioning of the three main signal processing applications: FFT, convolution and correlation. The proposed system is implemented using VHDL. The proposed system performs signal processing operations efficiently and reduced area and low power is achieved. A modified carry look ahead adder and array multiplier is used to reduce the area and delay. The implemented design can be viewed in waveform and can be easily upgraded by increasing the memory of the system and can thus be implemented with higher bit value

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