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Design and Implementation Multiphase DC-DC Converters for Hybrid Electric Vehicle

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Abstract: Proportional Integral Derivative (PID) controller is the most recommended controller in industries that does not require precise analytical model of the system to be controlled. This paper presents a Design, Analysis and Modeling of PID (Proportional -Integral-Derivative) controller based on FPGA (Field-Programmable Gate Arrays) for Synchronous Multiphase DC-DC Converters in Automotive Applications. Mat lab Simulink is used for the PID controller design to generate a set of coefficients associated with the desired controller characteristics. This simulation platform also integrates tools for a future implementation of the PID controller embedded in a FPGA controller. The main contribution of this work is to implementation of a PID controller that can be used independently of the number of phases of the converter, making it suitable to be applied in a wide range of high power applications. This controller has been designed having in mind, the goal of developing a real-time FPGA-based controller, so the complexity has been reduced to a minimum. Hybrid vehicles, aerospace, naval industry, process control, manufacturing, robotics and automation and transpiration system power systems can also benefit from the development of this controller.

Keywords: PID Controller, controller design, FPGA design, DC-DC converter.

I. INTRODUCTION

The objective of a controller design is to make a physical system behave in a useful fashion, causing its output to track a desire reference input even in the presence of noise, modeling error and disturbances. In the control system, one of the main components is the controller, which generates the appropriate control signal for the physical system to regulate the system performance. The Proportional-Integral-Derivative (PID) controller is one of the most common types of feedback controllers that are used in dynamic systems .It is used in the wide variety of control systems due its simple structure and robust performance. This controller has been widely used in many different areas such as aerospace, Hybrid vehicles, naval industry process control, manufacturing, robotics, and automation and transpiration system. The efforts being made to its design, justifies its popularity. The implementation of PID controllers has gone through several stages of evolution; recently FPGAs have become an alternative solution FPGA technology is now considered by an increasing number of designers in various fields of applications. The digital controller of switching dc-dc converter has been a popular topic in power electronics field. In the control of switching dc-dc converter, PID compensation has been widely used due to its remarkable efficiency, simplicity of implementation and converter with the PID Controller broad applicability and low power consumption. Another advantage of FPGA-based platforms is their ability to execute parallel operations, allowing parallel architectural design of

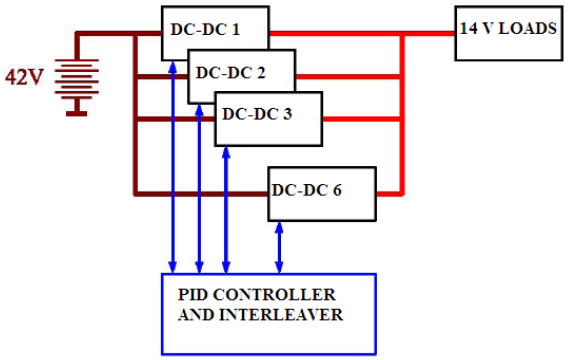

Fig.1. Block diagram of the proposed interleaved

digital controller. The implementation of the digital PID algorithm on FPGA is designed as a specialized computation processor. This PID circuit can be embedded into a process calculator. In general, real time applications. The proposed solution is to design and modeling a multiphase converter of 6 phases, as shown in Fig.1, that can be included in a dual power system inside a car with batteries of 42/14V. Employing such a high number of phases minimizes the passive components size in each one and also reduces the stress level due to lower currents. However, such a high number of phases imply a specific control scheme that allows synchronization between phases, in order to reduce output voltage ripple of the converter and equalize output currents among all the phases.

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This paper presents a simple methodology for FPGA implementation of PID controller for DC-DC Converter. Our approach starts with modeling and simulation of the controlled system of synchronous buck converter in Mat lab/Simulink. The structure in use implements PID control laws in discrete time system. So, the controller is formulated in the continuous-time domain and controller equations are discretized to implement the controller as a computational algorithm.

II. PID CONTROL ALGORITHM

A typical closed loop system using a PID controller is showninFig.1.The PID block provides the compensation in the feedback control of the switching converters. The ideal continuous time PID controller can be expressed as:

$$u(t) = K_P[e(t) + \frac{1}{T_i}\int_0^t e(t)dt + T_d\frac{d}{dt}e(t)] \quad (1)$$

Where u(t) is the control output, Kp is constant coefficient of the proportional gain, Ti is integral time, Td is the derivative time and e is the error between the reference VRef and output Vo, the s-domain expression of the corresponding PID controller can be given as:

$$u(s) = \left[K_P + \frac{K_i}{s} + K_d.s\right]e(s) \quad (2)$$

Where KP, Ki, and Kd are the proportional, integral and the derivative gains of the controller, respectively. For digital PID control with sampling periods Ts, the following digital PID control algorithm can be obtained by replacing the derivative term and the integral term with a backward difference function and a sum using rectangular integration respectively. The difference equation is given by:

$$u(n) = K_P\{e(n) + \frac{T_s}{T_i}\sum_{j=0}^{n} e(j) + \frac{T_d}{T_s}[e(n) - e(n-1)]\} \quad (3)$$

Where index n and j refer to the time instant. The digital PID block can further be simplified as:

$$u(n) = K_P.e(n) + K_i\sum_{j=0}^{n} e(j) + K_d[e(n) - e(n-1)] \quad (4)$$

Where Ki=KP.TS/Ti is the digital integral coefficient, Kd=KPTd/TS is the digital derivative coefficient and KP is the digital proportional coefficient. To compute the sum, all the past errors have to be stored. This algorithm is called the "position algorithm"

An alternative algorithm is characterized by the calculation of the control output u(n),based on u(n-1) and the correction term Δu(n). To derive the recursive algorithm, first calculate u(n-1) based on equation (4) as:

$$u(n-1) = K_P.e(n-1) + K_i\sum_{j=0}^{n-1} e(j) + K_d[e(n-1) - e(n-2)] \quad (5)$$

Then calculating the correction term as:

$$\Delta u(n) = u(n) - u(n-1) \quad (6)$$

$$\Delta u(n) = a\,e(n) + b\,e(n-1) + c\,e(n-2) \quad (7)$$

Where, a = (KP+Ki+Kd), b = (KP+2Kd) and c=Kd .The equation (7) is called incremental algorithm. The current control output is calculated as:

$$u(n) = u(n\text{-}1) + \Delta u \quad (8)$$

$$u(n) = u(n\text{-}1) + ae(n) + be(n-1) + ce(n-2) \quad (9)$$

For the implementation, the incremental algorithm (8) avoids accumulation of all past errors e(n),but require to store the previous value of control output u(n-1) only. In the switching converter the incremental PID algorithm is used in the compensator for calculation of duty cycle command d (n) corresponding to the error e(n). Consequently, the discrete time-domain equation for the output of the compensator is obtained as

$$d[n] = d[n-1] + a.e[n] + b.\,e[n-1] + c.\,e[n-2] \quad (10)$$

Where e(n), e(n-1), e(n-2) are the error signals of the nth, (n-1)th and (n-2)th sample, respectively. The d(n-1) is the duty-cycle command stored from the previous cycle, d(n) is the current duty cycle command which is the controller output for nth sample.

When controlling time-invariant system, the PID parameters can be constants and evaluated off-line. For FPGA implementation of PID architecture, the controller coefficients a, b and c uses fixed values and are determined off-line from the well design controller to be discussed in next section.

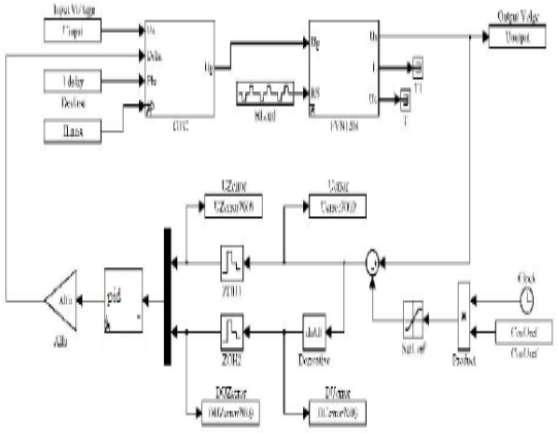

Fig.2. A single buck converter employing the simulation library

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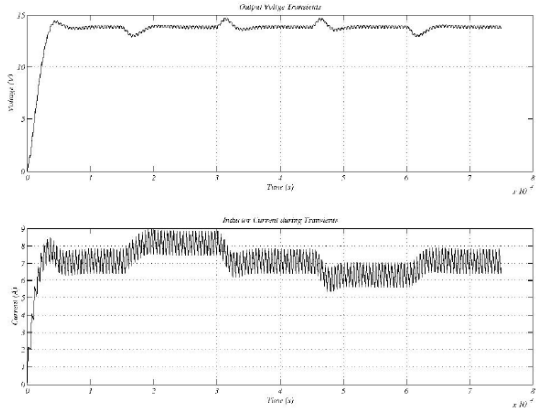

Fig.3. Simulation results for a single buck converter with PID controller.

III. PID CONTROLLER DESIGN

The performance of a closed loop converter is highly influenced by controller parameters. The controller ensures stable operation of the converter. To design the PID controller for Synchronous buck converter; a linearized model of the plant is developed as shown in Fig.3.The transfer function for each module is developed to obtain the plant model Gsys .

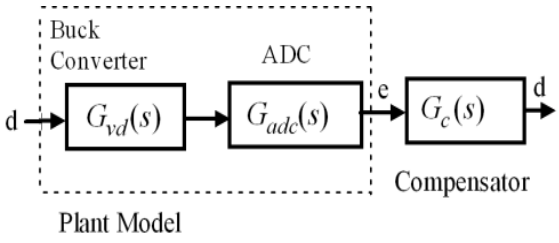

Fig.4. Linearized plant model of the closed loop synchronous buck converter

1) Power stage model Gvd(s)
For the general buck converter, the small signal control to output transfer function Gvd(s) is given by [9]

$$G_{vd}(s)=\frac{V_i(s.r_C.C+1)}{s^2LC\left(\frac{R+r_C}{R}\right)+s\left(r_C.C\left(\frac{R+r_L}{R}\right)+\frac{L}{R}+r_L.C\right)+\left(\frac{R+r_L}{R}\right)} \quad (11)$$

The following parameters are considered for the model Vi = 5V (nominal), R=1-2Ω, V0=2.5±2%, rC=5mΩ, rL=10mΩ, fs=200 KHz, L=12µH and C=47µf. With the specified parameters, Gvd (s) is given by:

$$G_{vd}(s)=\frac{1.175e-006.s+5}{5.654e-010\,s^2+6.706e-006.s+1.005} \quad (12)$$

2) ADC model Gadc(s)
The ADC gain depends on the resolution of ADC. The 8-bit ADC operating with reference voltage of 4.0V provides the resolution of VQ =15.6 mV, Hence the ADC gain is Kadc=64. Let tadc is the conversion time of ADC then the transfer function of ADC is given by:

$$G_{adc}(s)=K_{adc}.e^{-t_{adc}} \quad (13)$$

The plants model Gsys(s) is obtained as:

$$G_{sys}(s)=K_{adc}.G_{vd}.e^{-s(t_{adc}+dT_s)} \quad (14)$$

The total time delay associated is normally taken equals to switching period i.e Ts=(tadc+dTs).The plants function Gsys(s) is given as:

$$G_{sys}(s)=K_{adc}.G_{vd}.e^{-s(T_s)} \quad (15)$$

In the digital redesign approach an analog controller is first designed by ignoring the effects of S/H associated with the ADC and the DPWM circuits i.e initially assuming Kadc=1 in (17).With specified design parameters, the plants function Gsys(s) is then given by:

$$G_{sys}(s)=G_{vd}e^{-sT_s}=\frac{1.175e-006\,s+5}{5.654e-010s^2+6.706e-006s+1.005}e^{5e-006s} \quad (16)$$

A block diagram for the digital system needed to implement the real-time PID controller in an FPGA is show in Fig. 7. All the circuits in that system were designed using the Xilinx "System Generator" Toolbox for Simulink.

With this tool, the design process allows to directly program the FPGA without leaving Simulink. Nevertheless, it is also possible to obtain an intermediate VHDL description file for the whole system to optimize the FPGA implementation through the use of the Xilinx Foundation ISE tools, specific for this task.

It is shown in Fig. 8 the XUP Virtex2-Pro board used to implement the fuzzy controller. This boards hosts a XC2VP3O FPGA from Xilinx.

This FPGA has almost 31,000 logic cells, each constituted by on 16x1 tiny RAM [LUT(Look Up Table)] and one flip-flop. The FPGA also has 136 18x18 hardware multipliers, as well as 2 Mbits of dedicated RAM.

IV. FPGA BASED PID CONTROLLER DESIGN

The switching converter and controller form a closed loop feedback system to regulate the output voltage V0.The output voltage is sampled by an A/D converter, compared with Vref reference voltage to produce the digital error signal e[n].The sampling occurs once per switching period Ts. For dynamic and static voltage regulations require that:

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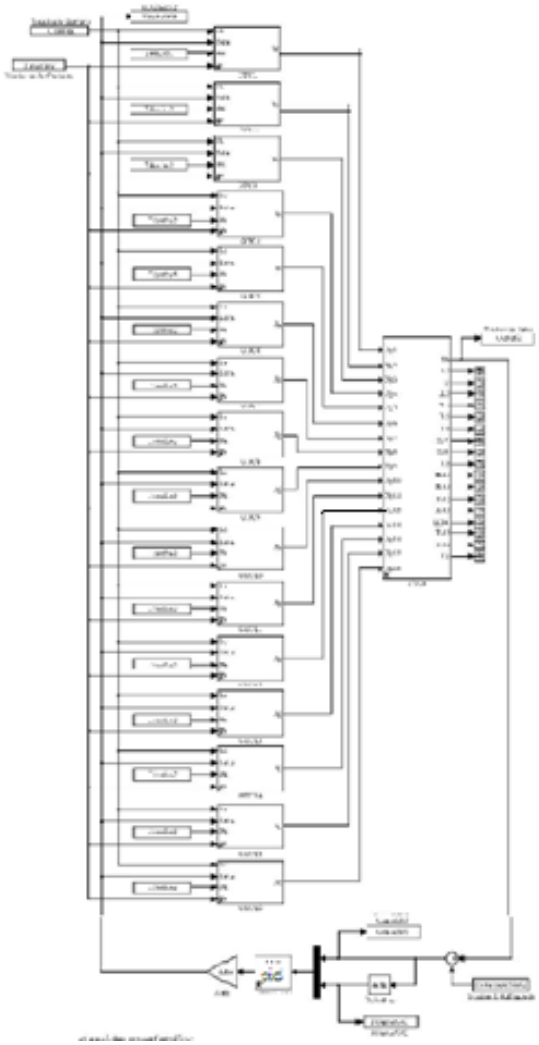

Fig.5. Simulink model for 16 buck interleaved converters with PID controller

- Vo(t) must always (including load or input voltage transients) stay in the specified range around reference Vref, from Vref-(ΔV0)max/2 to Vref+(ΔV0)max/2 .
- In addition, in steady state the dc output voltage must equal the reference voltage, with some allowed tolerance, V0=Vref ±ΔV0/2.

To meet these requirements, the analog equivalent Vq of the least significant bit (LSB) in the A/D characteristic must not be greater than specified ΔV0, but also that the conversion range must include only a relatively small range (ΔV0)max of voltages around the reference.
In our design, for dynamic voltage regulation requires that Vo should stay 5% around the reference of 2.5V, i.e total allowed variation around reference is (ΔV0)max =125 mV. In addition, for the static voltage requirement, ΔV0=1% of 2.5V. So, in steady state the dc output voltage must equal the reference voltage, with some allowed tolerance, V0=2.5 ±12.5mV. The Vq of the least significant bit (LSB) in the A/D characteristic is 15.6 mV. The digital representation of the error signal takes only nine possible values from -4 to +4(decimal).Only 4-bits are needed to represent the digital error signal e[n], leads to a simpler implementation of compensator. The purpose of the compensator is to take the current and previous samples of the error signal and compute the new value of the duty ratio d, which is the variable that controls the switching converter through the PWM. The control law in the compensator can be designed control law in the compensator can be designed as described in section (IV).The standard implementation of linear control laws in the compensator is possible using digital adders and multipliers. Taking advantage of the fact that only a few bits are used to represent the error e[n], the require computation is also implemented using three look-up tables (LUTs) and a adder. The current e[n] and previous values e[n-1], e[n-2] of the digital error signal serve as addresses to the corresponding location in the LUT. Since the error signal e can take only few different values, the number of entries in the LUTs is relatively small.

In this methodology the PID parameters are determined working with a time-invariant process in floating point numerical representations. Having obtained the discrete time equation, now our focus is on the implementation of control law of (23) using FPGAs (simulated, synthesized and implemented using Xilinx FPGA).For implementation of architecture is given:

The comparison is made between two architectures in terms of power consumption and resource utilization. In these architectures, the actual controller parameters are amplified by a factor of 256 and then rounded to their nearest value, to obtain the integer coefficients, the % rounding error involved is very small as shown in table 2. The amplification factor depends on the precision required. For large precision a large value of amplification factor is required, but then the area consumption will be more. So a tradeoff between area and precision exists for choosing amplification factor. The max. data values corresponding to controller co-efficient, when max.value of error is taken and the min. no of bits required to represent these dataset are given in table2.The coefficient and error inputs are taken in 2's complement format. So all mathematical operations are performed in 2's complement number system in both the cases. In LUTs based design, since the error signals takes nine different values.

Hence the architecture have three LUTs for e[n], e[n-1] and e[n-2] each having nine pre-calculated values. The minimum number of bits required to represent the numbers in the LUT's is given in Table2.But for uniformity, 16-bits are used to represent data in three LUT's. The architecture of Fig.6 has number of blocks error_ generator, error_seprator, Three Multipliers and Duty calculator. The error_gererator takes 8-Bit data from ADC output, which samples the output V0 of converter and compared with the reference voltage Vref and a 4-bit error data is generated.

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The function of error separator is to provide three error datasets e[n],e[n-1] and e[n-2].These dataset are applied to respective Multipliers as shown in Fig.6.The multiplied dataset of three multiplier are applied to Duty calculator block. The function of this block is to calculate the duty correction for each switching cycle and to determine the duty command word for each switching cycle by applying the duty corrections. The duty correction determined in the n-th switching cycle is added up with duty command of the (n-1) switching cycle. This duty command is then scaled 1/256 to obtain the actual. value. In the second architecture of Fig, same principle is applied, with three multipliers are replaced with three LUTs and corresponding instantaneous error signal acts as address to these LUTs. Table 2 shows the Constant coefficient values for Multiplier IP Core based architecture and Word length for LUT based architectures for three LUTs.

Table1: Constant coefficient value and LUT word length for Multiplier and LUT based Architecture

Controller Parameters	Parameter values (PV)	P=PV*256 (Amplified values)	Rounded Value (RV)	Rounding Error (%)	Max. data value RV*(±e[n]max)	Min. no. of bits Required to represent
A	13.10	3353.6	3353	17.8e-3	±13414	15
B	-24.80	-6348.8	6348	12.6e-3	±25395	16
c	11.80	3020.8	3020	26.4e-3	±12083	15

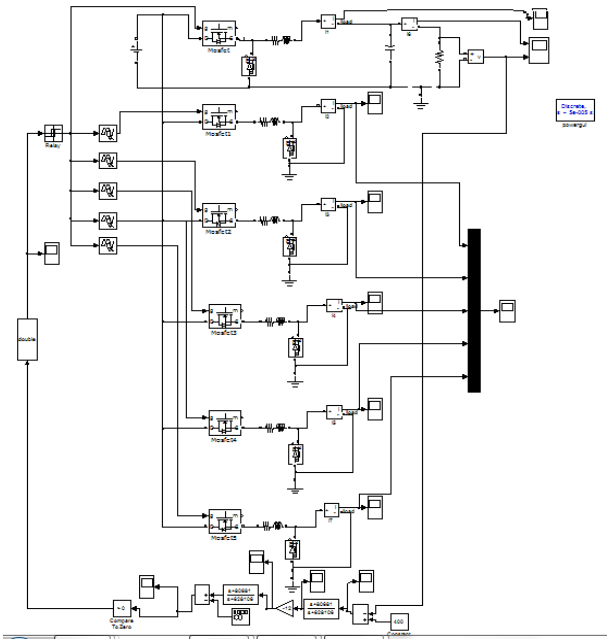

Fig.6. Simulation diagram of the proposed interleaved converter with the PID Controller

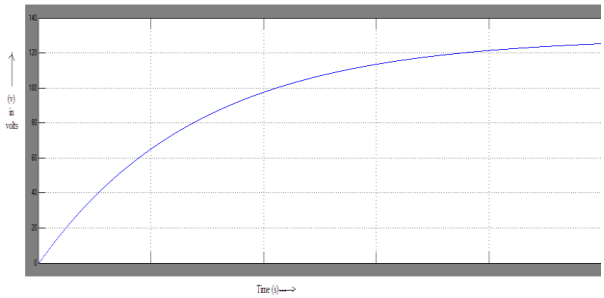

Fig.7. Simulation of output voltage from soft start to stable regime.

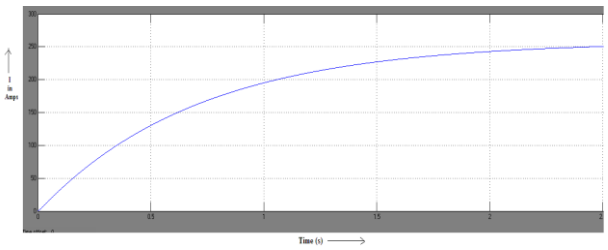

Fig.8. Simulation of output Current from soft start to stable regime.

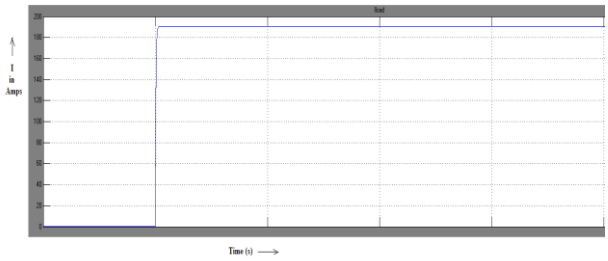

Fig .9. Individual converter inductor current.

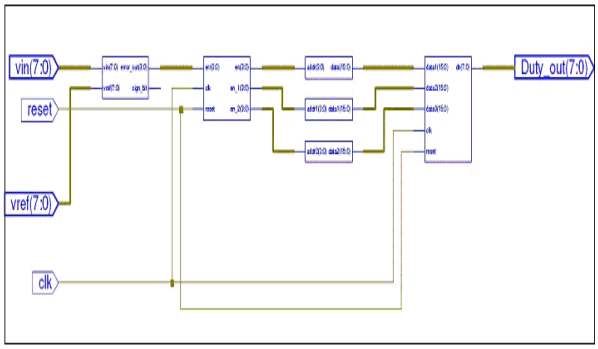

Fig 10: RTL of PID implementation using Look-up (LUT's) table

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V. CONCLUSION

This paper presents a design of PID controller when targeting Synchronous multiphase dc-dc converter in automotive applications. It is observed that, the look up table based design consume very less number of FPGA resources and hence the small area, at the same time the power consumption of look up table based design is less than multiplier based. A novel PID controller for interleaved parallel converters has been designed to achieve both speed and being able to fit inside an FPGA, analyzed to so that it fulfilled the specifications of automotive applications and simulated using a non-linear model of the power stage. The PID controller shows a good dynamic during soft transients and stable regime. This PID controller is ready to be implemented in an existent FPGA framework system previously crafted for this purpose. Following this work, more intensive test of multiphase dc-dc converter can be developed, analyzed and compared.

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