

Enhancement of Distributed Power Flow Controller during Series Converter Failures

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Abstract: The Distributed Power Flow Controller (DPFC) is a new device within the FACTS family. It is emerged from the UPFC and has relatively low cost and a high reliability. The DPFC consists of two types of converters that are in shunt and series connected to grids. The common dc link between the shunt and the series converters is eliminated. The active power exchange between the shunt and series converters that is through the common dc link in the UPFC, is now through the transmission line at the 3rd harmonic frequency. The redundancy of the series converters provides the high reliability of the system. In this paper, the DPFC behaviour during the failure of a single series converter unit is considered. A control scheme to improve the DPFC performance during the failure is proposed. The principle of the control is based on the facts that, the failure of single series converter will lead to unsymmetrical current at the fundamental frequency. By controlling the negative and zero sequence current to zero, the failure of the series converter is compensated. In this paper, the principle of the DPFC are firstly introduced, and followed by the behavior of the DPFC during the failure of a single series converter. The design of the control scheme and corresponding simulation are presented. Therefore, the cost of the DPFC system is lesser than the UPFC. The simulation is done using Matlab/Simulink software which is implemented on simple four bus system to expose the device control features and their impact on increasing capability of power transfer.

Keywords: Power Flow Control, Current Control, symmetrical component, Voltage Source Converter, Distributed Power Flow Controller, Unified Power Flow Controller.

I. INTRODUCTION

In nowadays power system, there is a great desire for the fast and reliable control of the power flow because of the growing demand of energy, the aging of networks and distributed generation. The Distributed Power Flow Controller (DPFC) recently presented in [1], is a powerful compact device within the family of FACTS devices, which provides a higher reliability than conventional FACTS devices at lower cost. It is derived from the UPFC and has the same capability to simultaneously adjust all the parameters of the power system: line impedance, transmission angle, and bus voltage magnitude [2].

Within the DPFC, the common dc link between the shunt and series converters is eliminated, which provides flexibility for independent placement of series and shunt converter. Of one large three-phase converter, the DPFC employs multiple single-phase converters (D-FACTS concept [3]) as the series compensator.

In this way, the series converters can float with respect to the ground thus reducing the cost of high voltage isolation. The DPFC uses the transmission line to exchange active power between converters at the 3rd harmonic frequency [1]. This concept not only reduces the rating of the components but also provides a high reliability because of the redundancy. The scheme of the DPFC in a simple two-bus system is illustrated in Fig.1.

The high reliability of the DPFC is provided by the redundancy of the converters. If one converter fails, the others will continue operation. However, the failed converter will stop providing the desired voltage, thereby causing asymmetry of the series converters and reducing the performance of the DPFC.

In this paper, the behavior of the DPFC during a single series converter failure is discussed. A control scheme that improves the DPFC performance during series converter failure is proposed, and the design of the control scheme and corresponding simulation are also presented.

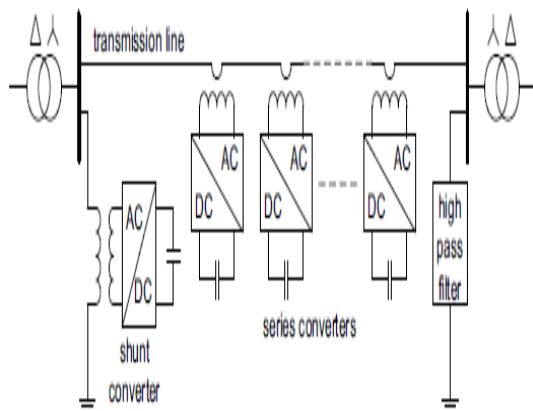


Fig.1. Schematic diagram of DPFC converter

II. DPFC PRINCIPLE

A. Introduction of the DPFC

Multiple individual converters cooperate together and compose the DPFC, see Fig. 1. The series converters consist of multiple units that are connected in series with the transmission lines. They can inject a voltage where the phase angle is controllable over 360o and where the magnitude is controllable as well, thereby controlling the active and reactive power flow through the line. The converter connected between the line and ground is the shunt converter. The function of the shunt converter is to compensate reactive power to the grid and to supply the active power required by the series converter. The unique control capability of the UPFC is given by the back to back connection between the shunt and series converters, which allows the active power to freely exchange. To ensure the DPFC have the same control capability as the UPFC, a method that can let active power exchange between converters with eliminated dc link is the pre condition.

Within the DPFC, there is a common connection between the ac terminals of the converters in different lines, which is the transmission line. Therefore, it is possible to exchange the active power through the ac terminals. The method is based on the power theory of non-sinusoidal components. According to the Fourier analysis, a non-sinusoidal voltage and current can be expressed by the sum of sinusoidal functions in different frequencies with different amplitudes. The active power resulted by this non-sinusoidal voltage and current is defined as the mean value of the product of voltage and current. Since the integrals of all the cross-product of terms with different frequencies are zero, the active power can be expressed by:

$$P = \sum_{i=1}^{\infty} V_i I_i \cos \phi_i \quad (1)$$

where V_i and I_i are the voltage and current at the n th harmonic frequency respectively, and ϕ_n is the corresponding angle between the voltage and current. Equation (1) describes that active power at different frequencies is isolated from each other, and voltage or current in one frequency has no influence on the active power at other frequencies. The independency of the active power at different frequencies gives the possibility that a converter without power source can generate active power at one frequency and absorb this power from other frequencies.

The 3rd harmonic is selected to exchange the active power in the DPFC, because it is a zero-sequence harmonic and can be naturally blocked by Y-Δ transformers, which are widely used in power system to change voltage level. B. DPFC control principle To control the multiple converters, DPFC consists of three types of controllers; they are: central controller, shunt control and series control, as shown in Fig.2.

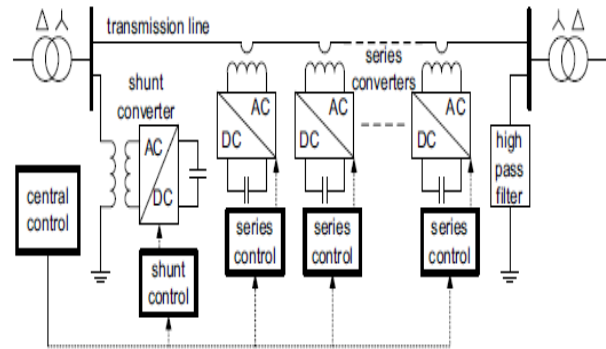


Fig. 2. Block diagram of the control of a DPFC

The shunt and series control are localized controllers and are responsible for maintaining their own converters' parameters. The central control is focus on the DPFC functions in power system level. The functions of each controller are listed:

- Central control: The central control generates the reference signals for both the shunt and series converters of the DPFC. It is focus on the DPFC applications in the power system level, such as power flow control, low frequency power oscillation damping and balancing unsymmetrical components, etc. According the system requirement, the central control gives corresponding voltage reference signals for the series converters, and reactive current signal for the shunt converter. All the reference signals generated by the central control are at the fundamental frequency.
- Shunt control: The objective of the shunt control is to inject a constant 3rd harmonic current into the line to supply active power for the series converters. At the mean time, it maintains the capacitor dc voltage of the shunt converter by absorbing active power from the grid at the fundamental frequency, and injects required reactive current at the fundamental frequency to the grid.
- Series control: Each series converter has its own series control. The controller is used to maintain the capacitor dc voltage of its own converter by using the 3rd harmonic frequency components, and to generate series voltage at the fundamental frequency that is required by the central control.

III. DPFC BEHAVIOR DURING SERIES CONVERTER FAILURE

Two types of failures can happen in the DPFC series converters: short circuit and open circuit. The short circuit for the series converters is not a problem, because it will not interrupt the transmission line. However, when the series converters have an open circuit, the transmission line will be also open circuit thereby influencing the whole network. To prevent the open circuit of the series converters, a bypass circuit is provided for each series converter. A crowbar is in parallel to the output terminals of the series converter. Once the series converter has an open circuit, the crowbar will be connected and provide the bypass for the transmission line. Accordingly, the

failed series converter appears short circuit to the transmission line, therefore the voltage injected by series converters becomes unbalance between phases. This unbalanced series voltage leads to unsymmetrical current in the line thereby decreasing power quality of the network. Assuming the DPFC is placed in a two port transmission network as shown in Fig. 1 with v_s and v_r on the sending and receiving ends bus voltages respectively. The total voltage injected by all series converters is v_{se} , and the number of series converter unit per phase is n . The voltage injected by series converters with failed converters in phase a is given by:

$$v_{se} = \begin{bmatrix} \frac{n-k}{n} v_{se,a} \\ v_{se,b} \\ v_{se,c} \end{bmatrix} \quad (2)$$

where k is the number of failed converter in phase a. By using sequence analysis, this unbalanced series voltage can be represented by:

$$v_{se} = \begin{bmatrix} v_{se}^+ \\ v_{se}^- \\ v_{se}^0 \end{bmatrix} \quad (3)$$

and the relationship between v_{se}^- , v_{se}^0 and the number of the failed converter is:

$$v_{se}^- + v_{se}^0 = \frac{k}{n} v_{se} \quad (4)$$

Therefore, the unbalanced line current at the fundamental frequency caused by the series converter failure is:

$$\begin{bmatrix} i_1^+ \\ i_1^- \\ i_1^0 \end{bmatrix} = \begin{bmatrix} 1/Z_1^+ & 0 & 0 \\ 0 & 1/Z_1^- & 0 \\ 0 & 0 & 1/Z_1^0 \end{bmatrix} \begin{bmatrix} V_s - V_{sr} + V_{se}^+ \\ V_{se}^- \\ V_{se}^0 \end{bmatrix} \quad (5)$$

where $Z_1^{+, -, 0}$ is the transmission line impedance in positive, negative and zero sequence respectively. As shown in (refeq:Iun), the line current at the fundamental frequency consists of negative and zero sequence components during the single series converter unit failure. Their magnitudes depend on the negative and zero sequence line impedance and the number of failed converters.

The series converter failure will not only influent the current at the fundamental frequency, but also the 3rd harmonic frequency. The faulty series converter do not require any active power, therefore the required active power between phases is different which results a change of the 3rd harmonic current. To find the 3rd harmonic current in each phase, the equivalent network of the DPFC at the 3rd harmonic is needed, as shown Fig. 3.

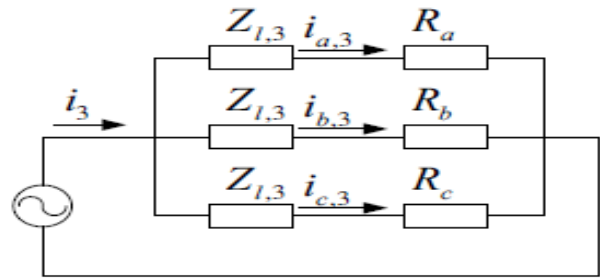


Fig.3. the corresponding arrangement of the DPFC at the 3rd harmonic

I_3 is the constant 3rd harmonic current generated by the shunt converter. At the 3rd harmonic frequency, the series converters are control to only generate or absorb active power, and they act like variable resistors. Therefore the series converters can be represented by the resistances $[R_a R_b R_c]$ at the 3rd frequency. The power consumed by the resistors is $[P_{se}]$ and it is given by:

$$P_{se} = \text{Re}(V_{se} I_3) \quad (6)$$

The distribution of the 3rd harmonic current over the three phases follows from:

$$\begin{cases} i_{a,3} + i_{b,3} + i_{c,3} = i_3 \\ Z_{l,3} \cdot i_{a,3} + \frac{P_{se,a,3}}{i_{a,3}^*} = V \\ Z_{l,3} \cdot i_{b,3} + \frac{P_{se,b,3}}{i_{b,3}^*} = V \\ Z_{l,3} \cdot i_{c,3} + \frac{P_{se,c,3}}{i_{c,3}^*} = V \end{cases} \quad (7)$$

where V is the voltage at the 3rd harmonic frequency across the transmission line. As equation (7) is not linear, it is difficult to the achieve analytical solutions for the 3rd current $[i_{a,3}, i_{b,3}, i_{c,3}]$. However, by applying a series typical DPFC parameters and solving the equations numerically, it is found that the nonzero sequence 3rd current $[i_{a,3}, i_{b,3}, i_{c,3}]_{+, -}$ is around 10% of nominal line current. To eliminate the 3rd harmonic current leakage and balance the unsymmetrical current at the fundamental frequency, a supplementary control is needed.

IV. CONTROL SCHEME TO IMPROVE THE PERFORMANCE

The principle of the supplementary control is to let the remained converters in the line with the fault converters inject more voltages to maintain the voltage balance between phases at the fundamental frequency. As the series converters are centralize controlled, this supplementary control is within the central controller. There are two requirements of the supplementary control:

- The controller should be able to distinguish the phase with the faulty converter and give correct compensation voltage reference.

- The communication between central control and series converters in different phases should be independent to enable the series converters in one phase to generate different voltage from the other phases.

One approach to compensate the converter failure is to let series converters report their status of the operation (active/ inactive) back to the central controller. The controller generates corresponding reference signals for each phase according to the number of the active converters. However, there are two major drawbacks of the method. First, this method highly relies on the communication between the converters and the central controller. Any false report will lead to an incorrect compensation. Second, the failed series converter is not pure short circuit and there will be a small unpredictable inductance inserted because of the single-turn transformer, and this inductance cannot be compensated by this method.

The proposed control scheme is based on the fact that, the failure of a single series converter will lead to unsymmetrical current at the fundamental frequency. By controlling the negative and zero sequence current to zero, the failure of the series converter is automatically compensated. For this purpose, two current control loops is added to the existing DPFC controller to control zero and negative sequence current, respectively. These two supplementary controllers are located in the central controller. All these controllers operate all the time. The control scheme of the central control with these supplementary controllers is shown in Fig. 4.

The sequence analyzer processes the three-phase line current first. The positive sequence current is used for power flow control purposes and the other sequence currents are for series converter failure compensation. When there is no failed series converter, the negative and zero sequence current is zero. In the case of series converter failure, the two current controllers force the negative and zero sequence current to become zero. The voltages created by the two controllers are added together with the positive voltage to construct the reference signals for the series converters in different phases.

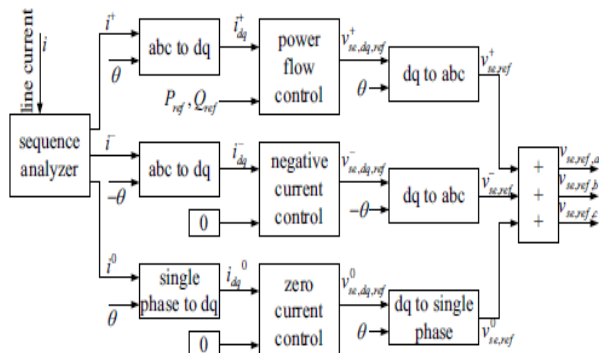


Fig.4. Control scheme for unbalance compensation

V. CONTROLLER DESIGN

A popular method for current control - synchronous PI control is employed for the zero and negative sequence controller because of the simplicity for implementation [4]. The idea is to transform ac currents and voltages into a rotating reference frame, where the controlled currents are constant in ‘steady state’. Ordinary PI controllers can be used on the transformed values, and the outputs of the controls can be transformed back to the fixed reference frame.

For the negative components, the conventional Park Transformation is used. As the zero sequence currents are in-phase, the single-phase Park Transformation [5], [6], [7] is employed. Both transformations utilize the bus voltage at the fundamental frequency as the rotation reference frame.

The structures of the zero and negative sequence network with the DPFC are similar.

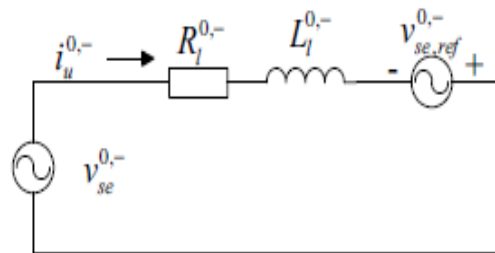


Fig.5. Simplified zero and negative sequence network with the DPFC

By replacing the DPFC series converter by ideal voltage sources, the simplified zero and negative sequence network with the DPFC can be represented as Fig. 5.

where $V_{se}^{0,-}$ is the unbalanced zero and negative sequence voltage injected by DPFC series converters with the faulty converter, $i_l^{0,-}$ is the corresponding unbalanced current within the line. I is the unequal current that flows through the line. Correspondingly $L_l^{0,-}$ and $R_l^{0,-}$ are the inductance and resistance that are correlated to the negative and zero sequences $V_{se}^{0,-,ref}$ is the unequal compensated voltage that is supplied by a series converter. The correlation among voltage and current is given by d-q transformation.

The current control parameter is calculated by internal model control (IMC) method [8], [9]. As the disturbance (unbalanced voltage) is unpredictable, additional inner feedback loops are added to active damp the disturbance for each control loop. Accordingly, the control scheme of the unbalanced current compensation is illustrated in Fig. 4. The function $F(s)$ is the controller function, and can be calculated by the IMC method as:

where αd and αq are the bandwidth for d and q components control respectively. A proper design of the active damping is to make it have the same time constant as the control loop, therefore the active conductance for each control loop can be

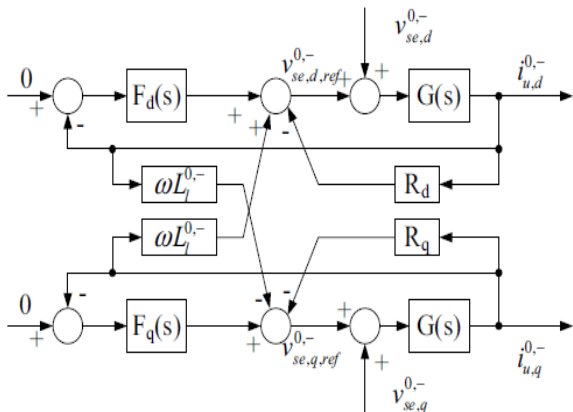


Fig. 6. Unbalanced current control scheme

VI. SIMULATION RESULTS

The simulation has been done in MATLAB/Simulink. The DPFC is tested in a two-bus system, where two fixed voltage sources are connected to the two transformers to represent the infinite buses. Both the bus voltages are 1pu with 1.5 differences. Three inductors represent the three-phase transmission line. To simplify the calculation, two sets of three series converter are connected to control the power flow through the line, each series converter generated 0.012pu voltage at the fundamental frequency. At t=1s, one of the series converter is short circuited manually.

The system behaviour with and without the supplementary controller is presented. Fig.7. shows the currents and voltages of series converter, voltage, currents delta side of the transformer at the fundamental frequency.

As shown, without the controller, the 3-phase system becomes unsymmetrical during the converter failure. The supplementary controller successfully compensates the phase difference caused by the series converter failure. In this case, one converter has a fault in phase a, therefore the control signal for phase a should be twice larger than without the fault, and the control signals for the rest phases should be unchanged. The magnitude of the series converter reference voltage and voltage injected by all series converters. Fig.7. shows the voltages, currents and Fig.9 & 10 shows the currents, active and reactive power.

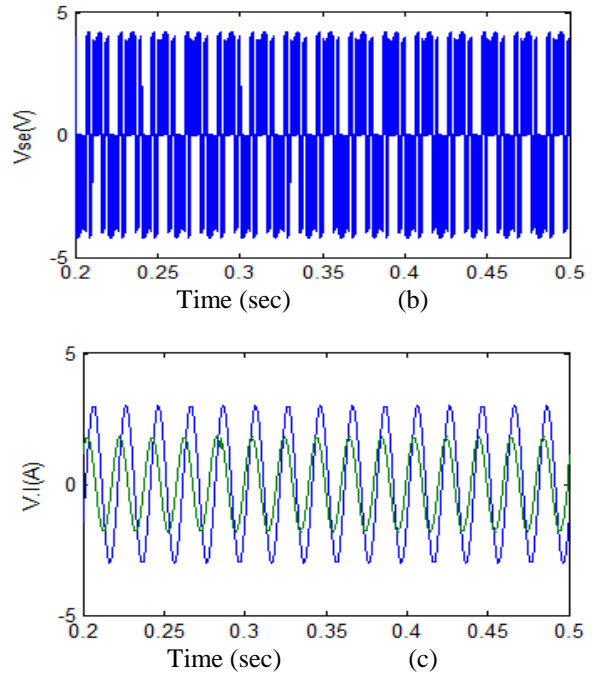
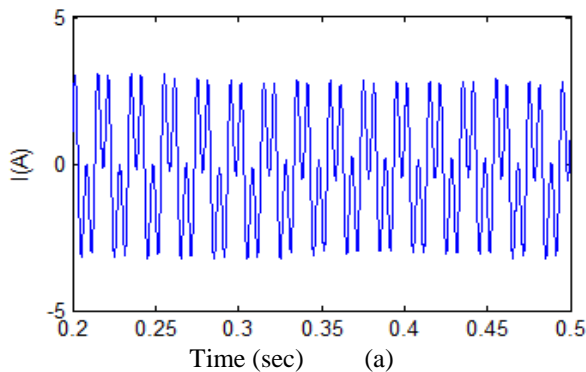


Fig.7.(a) series converter current (b) series converter voltage (c) bus voltage and current at delta-side of the transformer

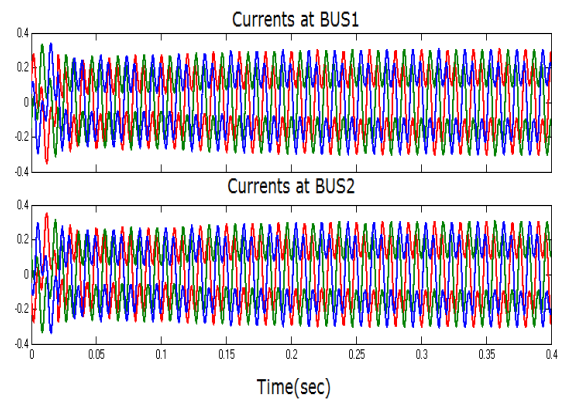


Fig.9. 3-phase voltage and current with DPFC at bus3

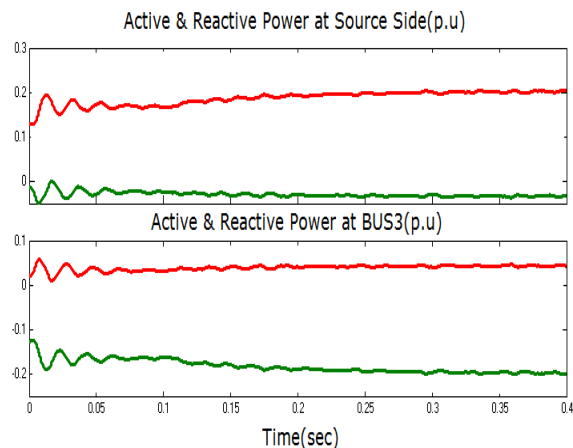


Fig.11. Active & Reactive power with DPFC converter

VII. CONCLUSION

This manuscript analyzed the DPFC performance during a failure of a single series converter unit. Series converters are protected by crowbar diodes to prevent over-voltage at the secondary side of the single-turn transformer. Therefore the failed series converter unit appears short-circuit to the transmission line and the voltage injection is unbalanced between phases. Because of this unbalance, the power network becomes asymmetric thereby resulting unsymmetrical current at the fundamental frequency. Also, the 3rd harmonic current that used to be zero sequence contains positive and negative components thereby leaking to rest of networks. A supplementary control scheme is proposed to add at the DPFC central control to improve the DPFC performance during series converter failure. Its principle is to monitor the zero and negative sequence components of the line current and control them to be zero. The control scheme has been simulated in MATLAB, and it proved that the asymmetric caused by the failure can be totally compensated.

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REFERENCES

- [1] Z. Yuan, S. W. H. de Haan, and B. Ferreira, "A new facts component: Distributed power flow controller (dpfc)," in Power Electronics and Applications, 2007 European Conference on, 2007, pp. 1–4.
- [2] L. Gyugyi, "Unified power-flow control concept for flexible ac transmission systems," Generation, Transmission and Distribution [see also IEE Proceedings-Generation, Transmission and Distribution], IEE Proceedings C, vol. 139, no. 4, pp. 323–331, 1992.
- [3] D. Divan and H. Johal, "Distributed facts - a new concept for realizing grid power flow control," in Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th, 2005, pp. 8–14.
- [4] M. Milosevic, G. Andersson, and S. Grabic, "Decoupling current control and maximum power point control in small power network with photovoltaic source," in Power Systems Conference and Exposition, 2006. PSCE '06. 2006 IEEE PES, 2006, pp. 1005–1011.
- [5] J. Salaet, S. Alepuz, A. Gilabert, and J. Bordonau, "Comparison between two methods of dq transformation for single phase converters control application to a 3-level boost rectifier," in Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual, vol. 1, 2004, pp. 214–220 Vol.1.
- [6] S. Shinji, "A robust single-phase pll system with stable and fast tracking," Industry Applications, IEEE Transactions on, vol. 44, no. 2, pp. 624–633, 2008.
- [7] R. Zhang, M. Cardinal, P. Szczesny, and M. Dame, "A grid simulator with control of single-phase power converters in d-q rotating frame," in Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Annual, vol. 3, 2002, pp. 1431–1436 vol.3.
- [8] H. Namho, J. Jinhwan, and N. Kwanghee, "A fast dynamic dc-link power-balancing scheme for a pwm converter-inverter system," Industrial Electronics, IEEE Transactions on, vol. 48, no. 4, pp. 794–803, 2001.
- [9] R. Ottersten, "On control of back-to-back converters and sensorless induction machine drives," Phd Thesis, Chalmers University of Technology, 2003.

BIOGRAPHIES



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