IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 4, Issue 3, March 2016

Fast and Wide Range Voltage Conversion Technique by Using 45nm Technology

K. Sathya[1], M. Saravanan[2]

PG Scholar, Department of ECE, SNS College of Technology, Tamilnadu, India[1]

Assistant Professor, Department of ECE, SNS College of Technology, Tamilnadu, India[2]

Abstract: A low-power level shifter (LS) using power gating technique is proposed for logic voltage shifting from near/sub-threshold to above-threshold voltage domain. Level shifter allow for effective interfacing between voltage domains supplied by different voltage level. Usually conventional level shifter which can shift any voltage level signal to a desired higher level with low leakage current. The new circuit combines the multi-threshold CMOS technique along with topological modifications to provide a wide voltage conversion range with limited static power, dynamic power and total energy per transition. When implemented in a 45-nm technology process the proposed design converts 500mV input signals to 1V output signal with lesser dynamic power, static power and total. Due to the area minimization heat dissipation also there. Using level shifter (DCVS) to reduce the heat dissipation in the circuit and also power supply.

Keywords: CMOS Technique, DCVS, Level Shifter (LS), Power Gating Technique, Voltage Conversion Technique.

1. INTRODUCTION

A.MULTISUPPLY VOLTAGE TECHNIQUE

Multi supply voltage domain (MSVD) technique is emerging as an effective method to reduce both dynamic and leakage powers in today's system-on-chips. This approach consists of partitioning the design into separate voltage domains (or voltage islands), each operating at a proper power supply voltage level depending on its timing requirements. Time critical domains run at higher power supply voltage (VDDH) to maximize the performance, whereas non critical sections work at lower power supply voltage (VDDL), so that dynamic and static power can be reduced without impacting on the overall circuit performance. For extremely low-power applications, the presence of circuit sections operating in subthreshold regime is a valuable option.

In an MSVD system, level shifters (LSs) are required on the boundaries between the circuit subsections operating at different power supply voltages to up-convert signals from the VDDL to the

VDDH voltage level. A well-known LS is the differential cascade voltage switch (DCVS) circuit that is typically used for converting signals between the two different above threshold voltage domains. Unfortunately, the DCVS-LS behaves as a ratioed circuit and the contention between the pull-up and pull-down networks becomes severe when input signals are in the subthreshold range, thus making the conventional sizing techniques impractical to obtain a properly functioning circuit. To address this problem, several improvements to the conventional DCVS circuit have been proposed here. The four-stage cascaded DCVS circuit described here assures robust level up-conversion from the subthreshold regime. Unfortunately, it introduces large power penalties, owing to the intermediate power supplies. Furthermore, it shows a limited speed performance. A two-stage LS was proposed. The first stage exploits a DCVS circuit with an always on diode connected nMOS transistor on the top; whereas, the second one is a conventional DCVS stage that lines, but again it is not enough to reach high speed performances.

B.VOLTAGE CONVERSION TECHNIQUE

Recently, proposed a low power LS, suitable for voltage signal up-conversion from the near/sub threshold regime, which exhibits a very low static and dynamic energy consumption. This is obtained at the expense of reduced voltage conversion range, and of relatively limited speed. In this brief, we present new LS that trade a certain amount of static power for a significantly improved operating speed and an extended voltage conversion range. Implemented with the 90-nm ST Microelectronics CMOS technology, the new design reliably converts input signals as low as 0.1 V to the 1 V nominal output voltage, with a delay of 170 ns.

2. EXISTING DESIGN

A.OVERVIEW OF LEVEL SHIFTER

The level shifter is used to convert high voltage levels to low voltage level or vice-versa. Bi-directional level shifters and translator circuit are used to interface between applications with different supply voltage and input-output voltage levels. Level shifters are the bridges that transform from low core voltage to high voltage. There are different types of level shifter such as single supply level shifter and dual supply level shifter. The single supply level shifter allows communication between modules without adding any extra supply pin, it have advantages over dual supply level shifter in terms of pin count, congestion in routing and overall cost of the system.

B.BASIC OPERATION OF LEVEL SHIFTER

The schematic of level shifter is shown below. Conventional level shifter using 10 transistors with low

IJIREEICE
ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526
INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 4, Issue 3, March 2016

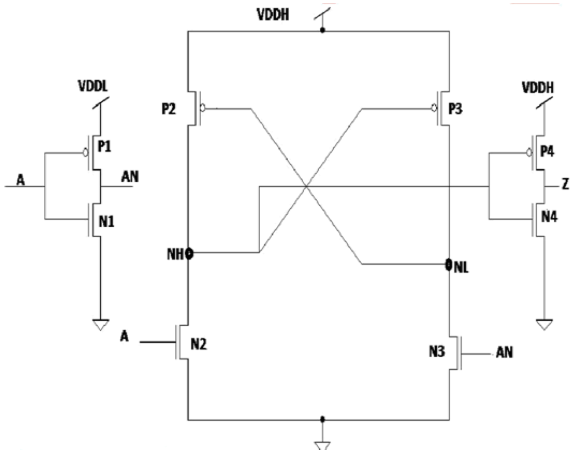
voltage supply VDDL and high voltage supply VDDH. The conventional level shifters have disadvantages of delay variation due to different current driving capabilities of transistors, large power consumption and failure at low supply core voltage VDDL.

3. PROPOSED DESIGN

The Deviation from constant field scaling due to the non-scaling parameters of the MOS transistors (thermal voltage, silicon energy band gap, and source/drain doping levels) leads to an increase in the power consumption and power density with each new technology. The increased power dissipation degrades the reliability, increase the cost of the packaging and cooling system, and lower the battery lifetime in electronic device. The multi-supply voltage domain technique, based on partitioning the design into separate voltage domains (or voltage islands) with each domain operating at a proper power supply voltage level is preferred depending on its timing requirement. Time-critical domain runs at higher power supply voltage (VDDH) to enhance the performance, whereas noncritical sections work at lower power supply voltage (VDDL) to enhance power efficiency.

A.PROPOSED LEVEL SHIFTER

The architecture of proposed level shifter. The new power gated level shifter is described in this section. Power gating uses low-leakage PMOS transistors as header switches to shut off power supplies to parts of a design in standby. Here high-Vt transistors are used for power gating. This level shifter uses a multi VTH CMOS technology in order to eliminate static dc current. There are different power gating parameters to be considered while using this technique, the most important ones being power gate size and power gate leakage. The power gate size must be selected to handle the amount of Shifting current at any given time. The gate must be bigger such that there is no measurable voltage (IR) drop due to the gate. Since power gates are made of active transistors, leakage reduction is an important consideration to maximize power savings. As shown in Figure 4.3, the circuit consists of an input inverter stage, a main voltage conversion stage and an output inverting buffer and power gating transistor. To increase the strength of the pull-down network of the main voltage conversion stage, it was also designed by using HVT transistors.



The current flowing through the nodes NH and NL at the beginning of their high to low transition could be of concern. Thus, to reduce this effect, two PMOS devices (P2 and P3) are adopted. P4 and P5 helped in weakening the pull-up networks of the main voltage conversion stage, thus reducing conflict NH and NL nodes. This choice also reduced the leakage current flowing through the pull-up networks when they are turned OFF. Finally, to achieve reliable voltage conversion, two diode-connected PMOS devices (P6 and P7) pull-up logics and the supply rail VDDH. This device limits the pull-up strength, but also reduces static power.

B. MULTI CONVERSION VOLTAGE DESIGN

This circuit provides fast differential low-voltage input signals to the main voltage conversion stage. Voltage shifting implementation has additional considerations for timing closure implementation. The following parameters need to be considered and their values carefully chosen for a successful implementation of this methodology. Power gate size must be selected to handle the amount of Shifting current at any given time. The gate must be bigger such that there is no measurable voltage (IR) drop due to the gate. As a rule of thumb, the gate size is selected to be around 3 times the Shifting capacitance.

4. RESULT ANALYSIS

INVERTER DESIGN

The low voltage inverter is designed using a pMOS and the nMOS with 45nm technology. Thus the power consumed by the inverter is reduced to 25% when compare to the 180nm inverter.

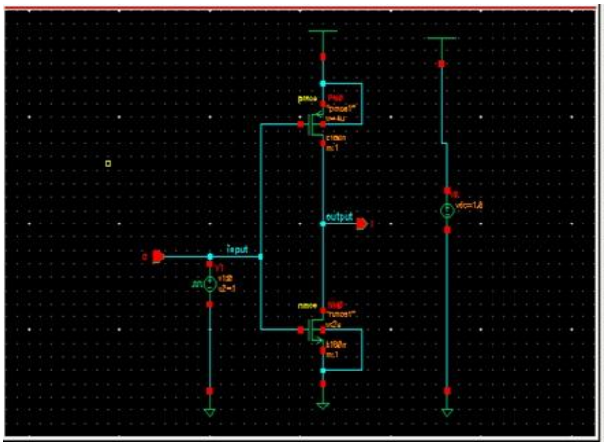


Figure1. Inverter Design

Level shifters (LSs) are required on the boundaries between the circuit subsections operating at different power supply voltages to up-convert signals from the VDDL to the VDDH voltage level. A well-known LS is the differential cascade voltage switch (DCVS) circuit that is typically used for converting signals between the two different above threshold voltage domains.

TRANSIENT ANALYSIS OF INVERTER

Time-critical domain runs at higher power supply voltage (VDDH) to enhance the performance, whereas noncritical sections work at lower power supply voltage (VDDL) to enhance power efficiency.

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 4, Issue 3, March 2016

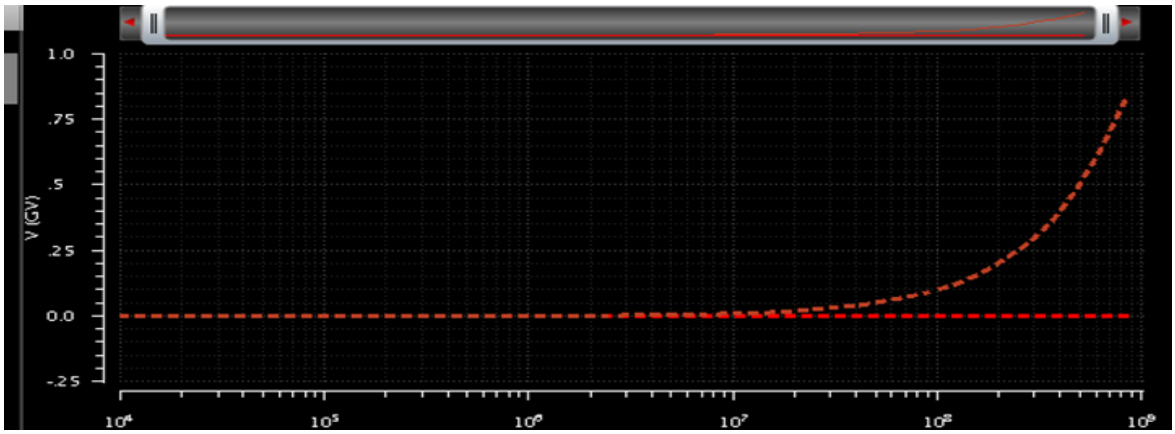


Figure 2 Transient Analysis Of Inverter.

OUTPUT WAVEFORM FOR INVERTER

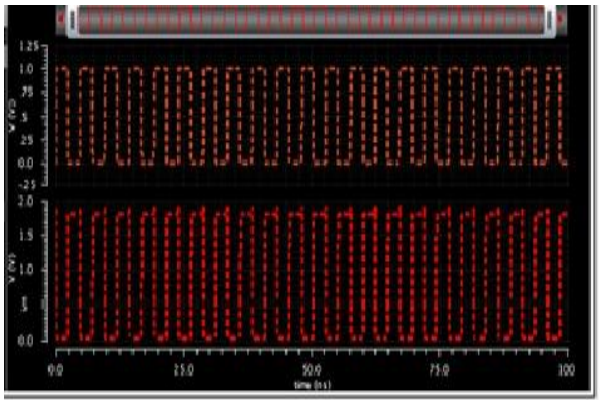


Figure3. Output Waveform for Inverter

MULTI VOLTAGE CONVERSION CIRCUIT

The multi-supply voltage domain technique, based on partitioning the design into separate voltage domains (or voltage islands) with each domain operating at a proper power supply voltage level is preferred depending on its timing requirement.

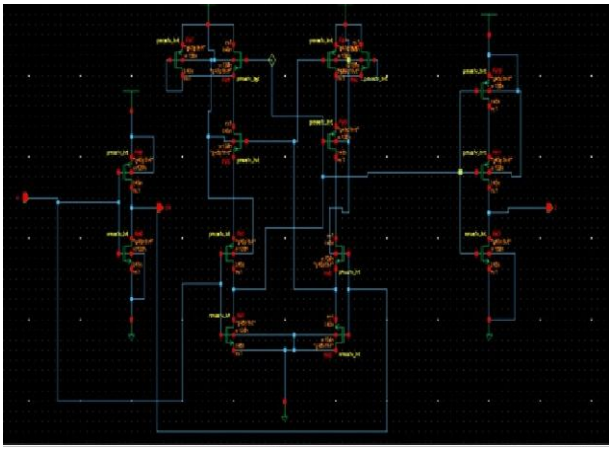


Figure4. Multi voltage Conversion circuit

A low power LS suitable for voltage signal Up conversion from the near threshold regime, which exhibits a low static and dynamic energy consumption. This is obtaining at the expense of reduced voltage conversion range.

Table1. Output Voltage for Multi voltage Conversion Circuit

Input Voltage	First Stage o/p (an)voltage	Output Voltage	TRANSIENT ANAYSIS
500mv 700mv	0.7 subthreshold voltage 0.5 subthreshold voltage	1 V 1.5V	197.1ns 197.5ns

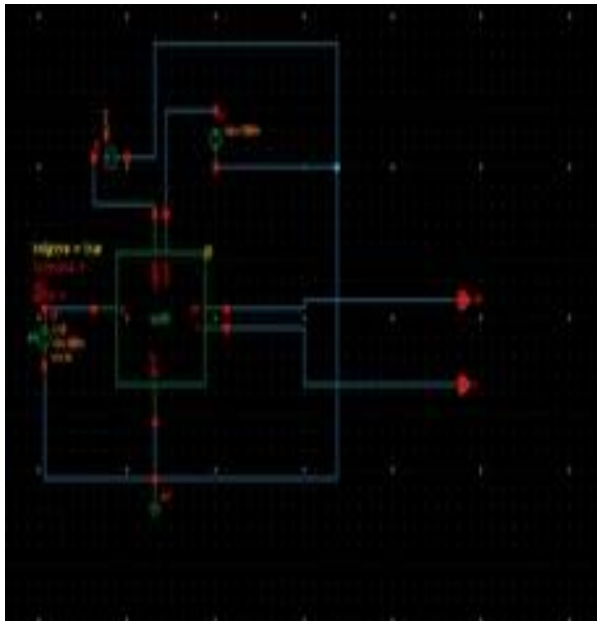


Figure5. Symbol Creation for Multi voltage Conversion

OUTPUT VOLTAGE FOR MULTIVOLTAGE CONVERTION CIRCUIT

The input inverter (MP1/MN1) is designed using low threshold voltage (lvt) transistors. This provides fast differential low-voltage input signals to the main voltage conversion stage. Higher strength of the pull, also MN2 and MN3 are lvt transistors. Then, two lvt pMOS devices (MP2 and MP3) are added to both the branches of the circuit.

DOI 10.17148/IJIREEICE.2016.4304

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 4, Issue 3, March 2016

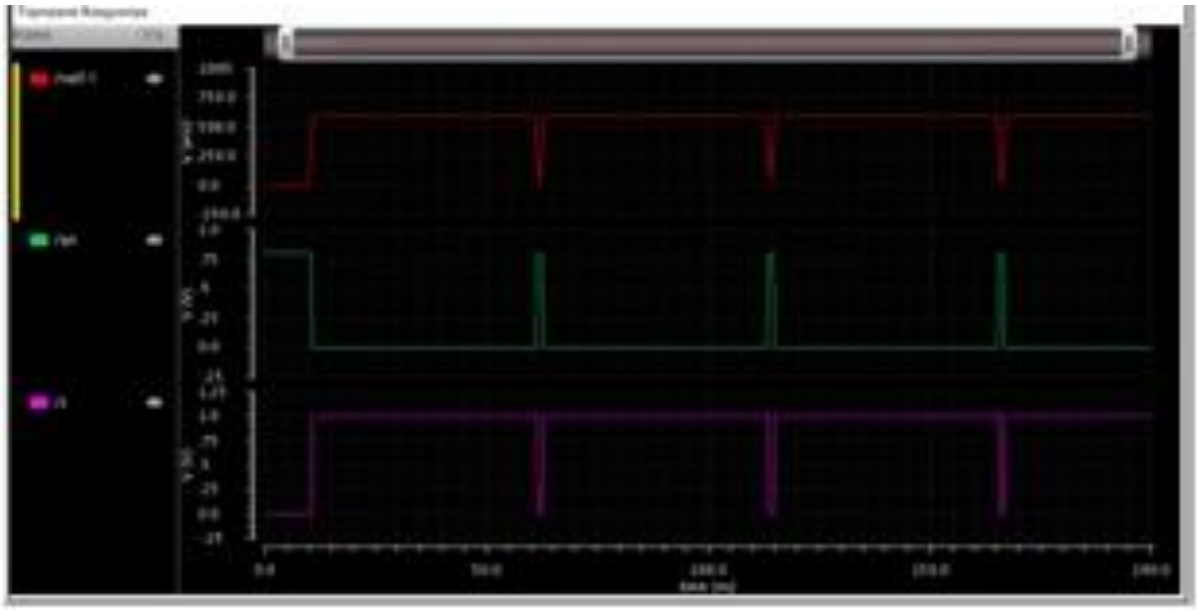


Figure6. Output Voltage for Multi voltage Conversion Circuit

TRANSIENT ANALYSIS OF MULTIVOLTAGE CONVERTION CIRCUIT

```
    start = 0 s
    outputstart = 0 s
    stop = 200 ns
    step = 200 ps
    maxstep = 4 ns
    ic = all
    useprevic = no
    skipdc = no
    reltol = 1e-03
    abstol(V) = 1 uV
    abstol(I) = 1 pA
    temp = 27 C
    tnom = 27 C
    tempeffects = all
    errpreset = moderate
    method = traponly
    lteratio = 3.5
    relref = sigglobal
    cmin = 0 F
    gmin = 1 pS

    tran: time = 6.2 ns       (3.1 %), step = 3.2 ns        (1.6 %)
    tran: time = 15.1 ns      (7.55 %), step = 1.126 ns     (563 m%)
    tran: time = 25.64 ns     (12.8 %), step = 3.988 ns     (1.99 %)
    tran: time = 37.64 ns     (18.8 %), step = 4 ns           (2 %)
    tran: time = 45.64 ns     (22.8 %), step = 4 ns           (2 %)
    tran: time = 57.64 ns     (28.8 %), step = 4 ns           (2 %)
    tran: time = 65.22 ns     (32.6 %), step = 630.2 ps     (315 m%)
    tran: time = 78.14 ns     (39.1 %), step = 4 ns           (2 %)
    tran: time = 86.14 ns     (43.1 %), step = 4 ns           (2 %)
    tran: time = 98.14 ns     (49.1 %), step = 4 ns           (2 %)
    tran: time = 106.1 ns     (53.1 %), step = 4 ns           (2 %)
    tran: time = 115 ns       (57.5 %), step = 18.44 ps    (9.22 m%)
    tran: time = 126.1 ns     (63.1 %), step = 3.043 ns     (1.52 %)
    tran: time = 138.1 ns     (69.1 %), step = 4 ns           (2 %)
    tran: time = 146.1 ns     (73.1 %), step = 4 ns           (2 %)
    tran: time = 158.1 ns     (79.1 %), step = 4 ns           (2 %)
    tran: time = 165 ns       (82.5 %), step = 2.889 ns     (1.44 %)
    tran: time = 175.1 ns     (87.5 %), step = 2.208 ns      (1.1 %)
    tran: time = 186.1 ns     (93.1 %), step = 4 ns           (2 %)
    tran: time = 197.1 ns     (98.5 %), step = 2.945 ns     (1.47 %)
Number of accepted tran steps =                404

Notice from spectre during transient analysis `tran'.
    Trapezoidal ringing is detected during tran analysis.
        Please use method=trap for better results and performance.
```

TRANSIENT TIME - 197.1 ns

5. CONCLUSION

A low-power level shifter has been proposed suitable for logic voltage shifting from near/sub-threshold to above threshold domain with reduced dynamic, static power dissipation and total energy per transition. The circuit when used for sub-threshold to above threshold voltage conversion, exhibits the lowest static power and energy consumption with respect to previous proposed LS that used similar design parameters. Moreover, even though the new designed LS is optimized for low power consumption, it also and supports a wide voltage conversion range the Proposed circuit exploits proper design strategies to increase the operating speed while maintaining very low energy consumption and large voltage conversion range when used to up convert voltage signals from the deep sub threshold. Reduce leakage current using low threshold to high threshold conversion. In 90 nm technology is parameter (temperature depended) so heat dissipation occurred in 45nm technology is independent to parameter value so heat dissipation is also low.

REFERENCES

[1] 'Analysis of Probability and Energy of nanometre CMOS circuit in present of transcations on circuit and systems Vol 58, no 9 march 2010.

[2] X. Liu, Y. Zheng, M. W. Phyu, F. N. Endru, V. Navaneethan, and B. Zhao, "An ultra- low power ECG acquisition and monitoring ASIC system for WBAN applications," IEEE J. Emerging Sel. Topics Circuits Syst., vol. 2, no. 1, pp. 60–70, Mar. 2012.

[3] D. Markovic, C. C. Wang, L. P. Alarcon, and J. M. Rabaey, "Ultralow power design in near-threshold region," Proc. IEEE, vol. 98, no. 2, pp. 237–252, Feb. 2010

[4] Y. Pu, J. P. de Gyvez, H. Corporaal, and Y. Ha, "An ultralowenergy/ frame multi-standard JPEG co-processor in 65 nm CMOS with sub/near-threshold power supply," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2009, pp. 146–14.

[5] D. Bol, R. Ambroise, D. Flandre, and J. D. Legat, "Analysis and minimization of practical energy in 45 nm subthreshold logic circuits," in Proc. IEEE Int. Conf. Comput. Design, Oct. 2008, pp.294–300.

[6] N. Verma, J. Kwong, and A. P. Chandrakasan, "Nanometer MOSFET variation in minimum energy subthreshold circuits," IEEE Trans. Electron Devices, vol. 55, no. 1, pp. 163–174, Jan.2008

[7] Asaf Kaizerman,sagi Fisher and Alexander Fish 'SubThreshold Dual Mode Logic" IEEE Trans.' Very Large Scale Integration(VLSI) System, vol. 29, no. 5, pp. 979–983, may- 2013.

[8] Jatin N.Mistry 'Active Mode Subclock power gating IEEE Trans.' VLSI SYSTEMS,journal accepted,august 20,2013.

[9] N. Mehta and B. Amrutur, 'Dynamic supply and threshold voltage scaling for CMOS digital circuits using in-situ power monitor,' IEEE Trans. Very Large Scale Syst., vol. 20, no. 5, pp. 892–901, May 2012.

[10] J. Seomun, I. Shin, and Y. Shin, 'Synthesis of active-mode power gating circuits,'IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 31, no. 3, pp. 391Mar2012.