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Temperature Effect of CNTFET under Different Dielectric Materials

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Abstract: A thorough study of the ballistic effect on the performance of the carbon nanotube field effect transistor has been explored in detail in this paper. The behavior of CNTFETs has been analyzed as a function of temperature by varying the gate dielectric constant and gate oxide thickness. Current ratio with a fixed oxide thickness and diameteris observed under different temperature for different dielectric materials and the ratio is increased while increasing the dielectric constant but the ratio degrades with the increasing temperature for all dielectric materials. On the other hand, current ratio is decreased while increasing oxide thickness for a fixed dielectric material and diameter as a function of temperature. The degradation of current ratio in lower temperature range is noticeable but for higher temperature range the slope of the degradation of current ratio is almost constant. The off state current remains same regardless of varying dielectric constant and oxide thickness and always increases while increasing the temperature. Transconductance remains almost constant as a function of temperature but increases with the increase of dielectric constant for all oxide thickness for a fixed tube diameter. Transconductance slightly decreases with the increasing oxide thickness for all dielectric materials. Effect of tube diameter for the variation of band gap is also investigated which is inverse relationship.

Keywords: Transconductance, Off-state current, Current Ratio, Chiral Indices, Chiral Angle.

I. INTRODUCTION

Carbon nanotube field effect transistors (CNTFETs) are particularly attractive because of the easy application of high dielectric constant gate insulator, novel device physics, large mean free path, unique quasi-ideal electronic as well as optical characteristics of carbon nanotube [1,2]. High dielectric constant materials are useful as gate insulators as they can provide efficient charge injection into transistor channels and reduce direct tunneling leakage currents [13]. CNTFET supplies electron from source to drain terminal for collection which is similar to MOSFET. Through experiment work Single-walled carbon nanotubes (SWCNT) was discovered by Iijima [3,4].This finding of SWCNT is significant due to the fundamental structure which has now become the basis for theoretical studies of large bodies. Mesoscopic physics analysis with higher dielectric constant gives different aspects of CNTFET and their structures for modeling a CNTFET. CNTFET is more superior to MOSFET because of its properties like higher on-state current, high channel density as well as high electric density [5-8].

While increasing the number of transistors integrated on a chip, the scaling of MOSFET increases. So, capacitance of the device is increased while decreasing the oxide thickness for MOS scaling.Gate oxide thickness maintains an inverse relationship with drain current in case of CNTFET[9]. In this paper we have observed that insulator thickness maintains an inverse relationship with Ion/Ioff current ratio for the increase of temperature. CNTFETs are mainly divided into Schottky barrier CNTFETs (SB CNTFETs)and MOSFET-like CNTFET.Here various properties of CNTFET is investigated under different Temperature as temperature plays a vital role in the performance and characteristics of CNTFET which is present in MOSFET [14].

If the channel length of CNT transistor is smaller than the carrier mean free path and larger than Coulomb blockade length, ballistic nature is then shown by the CNT transistor [16]. Carbon nanotubes are hollow seamless cylinders that can be envisioned as being formed by rolling up a finite sized piece of graphite sheet [13].Depending on the roll-up process of the graphite sheet occurs in the time of the growth process, semiconducting as well as metallic character can be shown by carbon nanotubes. The existence of metallic as well as semiconducting nanotubes points towards the fully carbon nanotubes-based electronics where metallic tubes act as interconnecting wires [13]. In this paper, the effect of variance of different dielectric materials is shown for metallic CNT. The band gap of the semiconducting tubes scales inversely with the tube diameter which is also investigated in this paper. Moreover, the variation of Ion/Ioff current ratio, off state current, transconductance considering different oxide thickness as a function of temperature are investigated under ballistic regime.

II. MATHEMATICAL ANALYSIS FOR BALLISTIC CNTFET

Conductivity of carbon nanotube changes depending on the angle of the atom arrangements along the tube. The atom arrangements are referred as chirality vector and represented as integer pair (m, n). Depending on the values of m and n sometimes carbon nanotubes act as conductor and sometimes semiconductors. The nanotube acts as metal if n=m or n-m=3i where i is an integer. Otherwise nanotube acts as semiconductor. The circumference of nanotubes can also be expressed in terms of chiral vector, $C = na_1 + ma_2$. The equation for the calculation of diameter is [18]

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$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + mn + m^2} \ldots\ldots\ldots (1)$$

Where, $a_0 = 0.142$ nm is the inter-atomic distance between each carbon atom and its neighbor. Here we have considered the diameter of nanotube $D_{CNT} = 1.02$ nm. Chiral angle ϑcan be calculated using the following equation [18]

$$\cos\theta = \frac{\frac{(n+m)}{2}}{\sqrt{n^2+mn+m^2}} \ldots\ldots\ldots \quad (2)$$

Here, the chiral angle is considered as 30°. And from the above two equation we have calculated the value of chiral vector that is m, n. we found m = 11 and n = 11. As the value of m and n is equal (m = n), theCNT is working as metallic conductor [15].

For the purpose of investigating ballistic transport in CNTFET considering the chiral angle of CNT as 30° and (11, 11) chiral indices, a simulation study is carried out using MATLAB based on FETTOY model of CNTFET. According to the ballistic CNT transport theory, the drain current caused by the transport of the non-equilibrium charge across the nanotube can be found by the Femi-Dirac statistics as follows:[17]

$$I_D = \frac{2qKT}{\pi h}\left[f_0\left(\frac{U_{SF}}{KT}\right) - f_0\left(\frac{U_{DF}}{KT}\right)\right] \ldots\ldots\ldots (3)$$

Where f_0 represents the Fermi-Dirac integral of order 0, K is Boltzmann's constant, T is the operating temperature, h is reduced Plank's constant.

III.RESULTS AND DISCUSSION

The variation of band-gap as a function of tube diameter is investigated here. It is evident from figure (1) thatthe relationship of Band gap is inversely proportional with respect to thetube diameter of CNT.

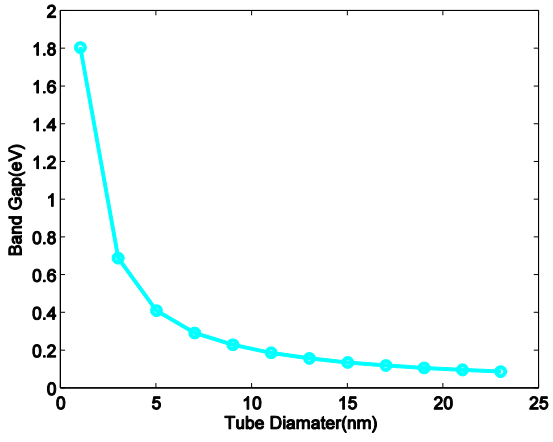

Fig1Band-gap vs tube diameter for 30° chirality representing metallic tubes

The CNTFET configuration is considered here isa (11, 11) chiral indices (m, n) which dictates metallic CNT[15] with a band gap ~1.80 eV at 1.02 nm tube diameter. Here, the simulation is being done with a gate and drain control parameters of 0.88 and 0.035 in addition with the source Fermi-level of -0.32 eV. Under different dielectric materials and different oxide thickness which separates the coaxial gate from the intrinsic part of the nanotube,thetemperature is varied from 300K to 500K to examine the influence of the temperature on the attributes of CNTFET.

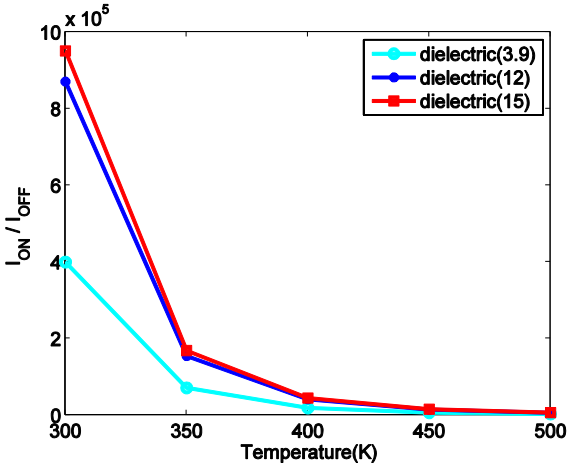

Fig 2.I_{on}/I_{off} current ratio vs Temperature for different dielectric constant with oxide thickness t_{ox}=2 nm and tube diameter (d) =1.02 nm

Figure (2) shows the effect of temperature on the current ratio for different dielectric materials. Here on current, I_{on} is measured at V_{GS}=1.00V and V_{DS}=0.00V and off current, I_{off} is measured at V_{GS}=0.00V and V_{DS} =1.00V.Figure (1) depicts that I_{on}/I_{off} current ratio is decreased while increasing the temperature. The simulation also shows the increment of current ratio as a function of temperature for higher dielectric materials. But if we increase the dielectric constant after a certain value, the increment of current ratio is not that much noticeable. For lower temperature range the increment of current ratio for initial increasing of the dielectric constantis significant but for higher temperature range, the increment rate degrades drastically.

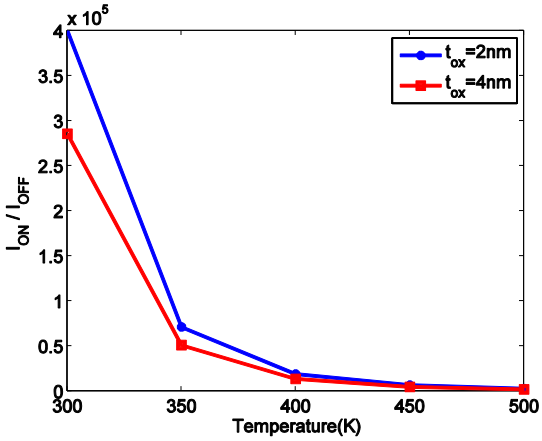

Fig. 3Temperature vs I_{on}/I_{off} for different oxide thickness with dielectric constant=3.9 and tube diameter (d) =1.02 nm

Here, on current I_{on} is measured at V_{GS} =1.00V and V_{DS} =0.00V and off current I_{off} is measured at V_{GS} =0.00V and V_{DS} =1.00V. Figure (2) shows the effect of temperature on the current ratio for different oxide thickness. Here, it is observed that oxide thickness maintains an inverse relation

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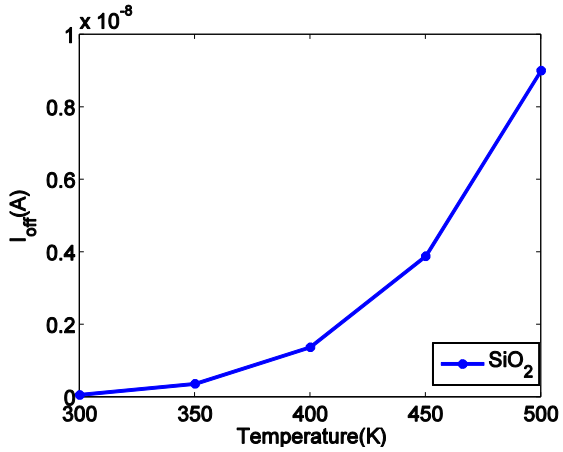
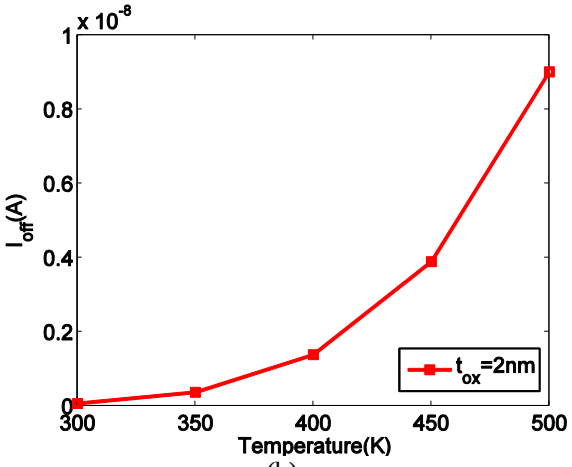
with the current ratio as a function of temperature. For all dielectric constant we have observed that, if oxide thickness is increased then I_{on}/I_{off} ratio is decreased. It is also observed that for lower temperature range the decrement of current ratio is significant but for higher temperature range the decrement rate is almost negligible.



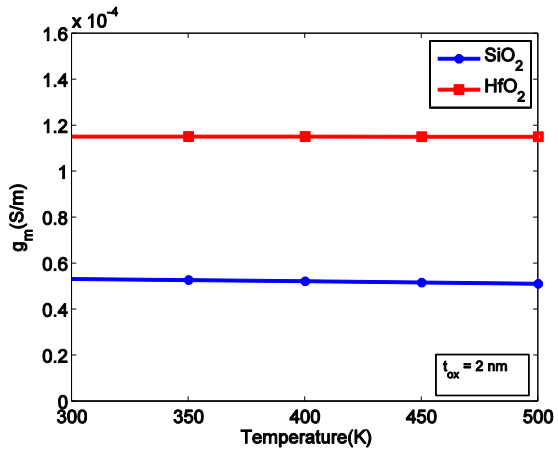
(a)



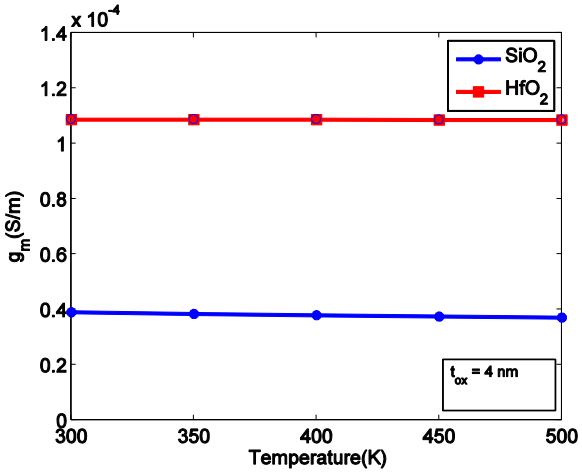
(b)

Fig. 4 I_{off} vs Temperature with d=1.02 nm (a) for different dielectric constant with t_{ox}=2 nm (b) for different oxide thickness with dielectric constant=3.9

Figure 4 (a) and (b) shows the off current with respect to the temperature. In this case gate voltage is being kept at zero and the drain voltage remains at 1.00V. The off current, I_{off} is always increasing while increasing the temperature.At first, off state current is measured for different dielectric materials by keeping a fixed oxide thickness which is shown in figure 4(a). Again, off state current is measured for different oxide thickness by keeping the dielectric constant as 3.9 which is shown in figure 4(b).We have investigated that off state current is same for any dielectric materials and any oxide thickness as a function of temperature. So, there is no effect of varying oxide thickness and dielectric materials on off state current which is always increasing with the increasing temperature. On the other hand, for smaller value of oxide thickness, the height of potential barrier becomes high and tunnelling concept becomes prominent which leads to higher thermionic emission (TE) current and hence on current is increased [12]. From figure 4(b) we have explored that off current is same for any oxide thickness as a function of temperature.This is why the current ratio gets increased for lower oxide thickness.



(a)



(b)

Fig. 5 Transconductance vs Temperature for different dielectric constant and tube diameter d=1.02 nm (a) with tox=2 nm (b) with tox=4 nm

The variation of transconductance with respect to temperature for various dielectric materials considering 2nm and 4 nm oxide thickness is observed. From figure (5) it is evident that while increasing the dielectric constant, the magnitude of the transconductance is increased for both 2 nm and 4 nm oxide thickness. The slope of the increment of the transconducatnce is almost constant. As off current is increased for any dielectric material and current ratio is increased for higher dielectric materials as a function of temperature, on current is increased for higher dielectric materials as a function of temperature. So, the transconductance is increased since the magnitude of on current is increased for higher dielectric materials [16].

Gain is largely dependent on transconductance. The higher the transconductance, the higher the gain. It has been already observed that transconductance maintains a proportional relationship with the increase dielectric constant as a function of temperature. From figure (5) it is evident that the magnitude of transconductance is slightly

higher for lower oxide thickness. The reason behind this is the on current gets bigger for lower oxide thickness as the off current is same for any oxide thickness and current ratio is higher for lower oxide thickness. From the result of figure (5) it is evident that for achieving higher gainfabrication of CNTFETs at lower oxide thickness and higher dielectric materials at room temperature is preferable.

IV. CONCLUSION

From the above exploration, it is evident that current ratio goes up for higher dielectric material and lower oxide thickness in lower temperature. Though off current is always constant for different dielectric constants and oxide thickness as a function of temperature. The on current should be higher for lower oxide thickness and temperature having higher dielectric materials. Also the transconductance is higher having obviously higher gain at lower oxide thickness and higher dielectric materials with having almost no effect of varying temperature. This means we can achieve expected gain at lower temperaturefor lower oxide thickness and higher dielectric materials. At the end of the analysis, it can be said that suitable condition for fabricating CNTFETs under ballistic condition are lower oxide thickness and higher dielectric materials in lower temperature range.

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