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Review of High Speed 32-bit Single Precision Floating Point Complex Multiplier using Vedic Mathematics

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Abstract: Multipliers are essential component of digital signal processing as they are used for determining the speed of Digital Signal Processor (DSP). The floating point complex multiplication is one of the basic functions used in digital signal processing application, microprocessors and FIR filters**.** Floating point format is a standard format used almost in all processing elements. Delay and power are main parameters used to determine the speed of multiplier. Conventional multipliers require more delay and hence consume more power for the multiplication. The Vedic mathematics technique is widely used because of its fast computational ability. This paper presents a review of 32bit single precision floating point complex multiplier using Vedic mathematics and proposes a design for high speed 32 bit single precision floating point complex multiplier using Vedic mathematic.

Keywords: Digital Signal Processor (DSP), Vedic mathematics, complex multiplier, floating point number.

I. INTRODUCTION

Multipliers are the main components of digital signal processing unit. Multiplication is an important fundamental arithmetic operation. The speed of the DSPs is mainly determined by the speed of its multiplier. Many high performance systems such as microprocessors, FIR filters and digital signal processors include the multiplier. The performance of these systems is generally determined by multiplier as it is the slowest element in the system. As the execution speed becomes most important part of any system, there is a need to design a high speed multiplier.

Multipliers can be used for multiplication of fixed point integer, floating point number and floating point complex numbers. Floating point complex number multiplication is the backbone of many digital signal processing algorithms, which mostly depend on extensive number of multiplication. Complex number multiplication is performed using four real number multiplications and two additions or subtractions. Addition and subtraction limits the overall speed of complex number multiplication. Binary floating point numbers multiplication is one of the basic functions is one of the basic functions used in digital signal processing (DSP) application [4].

Nowadays, almost every language has a floating point data type in all computers including personal computers and supercomputers. The floating point numbers are mainly used in medical field applications, image processing, motion sensing, scientific computing, audio applications, DSP applications etc. Hence, it becomes a prime need to design a floating point complex multiplier with improved computational speed. Vedic mathematics technique is a very efficient technique used for the calculation. This technique is used for the faster calculation of a floating point complex number.

Vedic mathematics is an ancient Indian system of mathematics. The word 'Vedic' is derived from the word 'Veda' which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras. It is far simpler and enjoyable than conventional mathematics and it is easier to understand as compared to modern mathematics.

Comparing to the conventional method of multiplication, Vedic multiplication method is very efficient in terms of speed. Floating point complex multiplier using Vedic multiplication is extensively used in DSP applications. Hence developing floating point complex multiplier using Vedic multiplier is a necessary choice.

We propose Vedic multiplier based on the "Urdhva Tiryagbhyam" sutra. The multiplication in Urdhva Tiryagbhyam sutra is done in vertically and crosswise manner.

II. RELATED WORK

Mohamed Asan Basiri M et.al [1] have proposed a MAC Design in Digital Filters with Complex Numbers. They designed a novel fixed point complex number multiply accumulate circuit, which is used in real time digital signal processing applications. \

The architecture consists of multiplier-cum-accumulator which can be used as multiplier as well as MAC (multiplication-cum-accumulation).

In the proposed architecture, the accumulation can be done along with multiplication (multiplication-cum-accumulation).In conventional radix-2 pipelined architectures the previous MAC result is added with the first carry save stage of the multiplier-cum-accumulator.

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So 2 stage pipeline only is possible. But in this proposed MAC Design, the previous MAC result is added with the last carry save stage of the multiplier-cum accumulator.

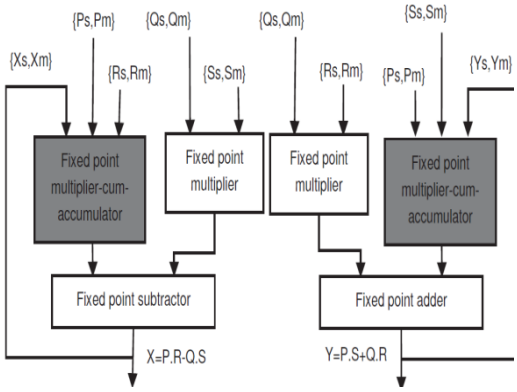

Figure 1: Fixed point complex number multiplier-cum-accumulator [1]

And hence n stage pipeline is possible which tends to increase the operating frequency. In MAC complex multiplier the real and imaginary parts are computed by sending the previous MAC result as one of the partial product to the present multiplication. So the separate accumulator circuit is avoided.

Sangho Yun et.al. [2] designed a low complexity floating-point complex multiplier. The design uses a three-term dot-product unit that reduces the overlapped unit that reduces the overlapped portion. The dot product unit mainly consists of fused multiply-add unit. A floating-point fused dot-product (FDP) unit perform a arithmetic operation. The FDP produces more accurate results because only the final result is rounded. The complex multiplier with two terms can be implemented by combining two equations into one unit to reduce the hardware complexity.

Prabir Saha et.al [3] presents report on a novel complex number multiplier design based on the formulas of the ancient Indian Vedic Mathematics, highly suitable for high speed complex arithmetic circuits. They designed complex multiplier by using parallel adders and sub-tractors. In this architecture, complex multiplier is designed at transistor level. For the multiplication purpose they used *Urdhva-Triyakbyham* sutra. This is the most efficient sutra that gives minimum delay for multiplication of small or large types of numbers. The advantage of this novel architecture encounters the stages ad partial product reduction. Following figure 2 shows the implemented block diagram of complex multiplier.

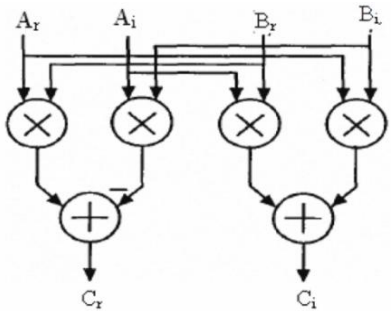

Figure 2: Implementation method of complex multiplier [3]

Laxman P. Thakare et.al [4] designed complex number multiplier using Urdhva Tiryakbhyam sutra which has been implemented using VHDL. The complete code is synthesized using Xilinx synthesis tool (XST).In this design architecture array multiplication and Booth's algorithm are used for multiplication. Also 8 bit adder and sub-tractor are used for calculating imaginary and real part respectively. The computational time in case of array multipliers are comparatively less since the partial results are calculated in parallel.

Ankush Nikam et.al.[5] designed 32 bit Complex Multiplier using the techniques of Ancient Indian Vedic Mathematics. The system was designed using VHDL and Verilog and is implemented through Xilinx ISE 14.2 navigator and modelsim v6.3 software's. Following figure 3 shows the block diagram of 32x32 complex number multiplier. It requires four 32x32bit Vedic multiplier modules and adders/sub-tractors.

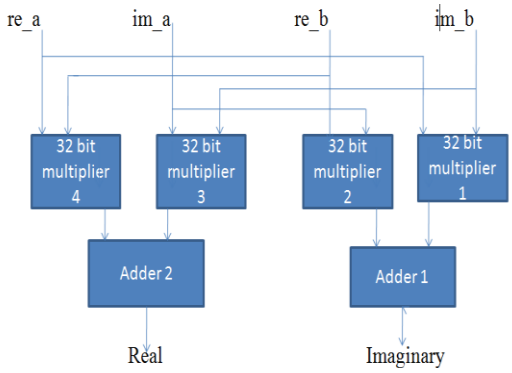

Figure 3: Block Diagram of 32 bit complex multiplier [5]

Pratiksha Rai et.al.[6] designed 32 bit Floating Point Multiplier Using Vedic Aphorisms as been implemented. For the design of multiplier VHDL Xilinx ISE tool was used. And for the simulation Model sim 10.2a was used. Any floating point number consists of mantissa, exponent and sign parts. For the mantissa multiplication the Urdhva-triyakbhyam sutra was used. The hardware requirement for the designed of 32 bit Floating Point Multiplier Using Vedic Aphorisms is less.

III. OVERALL ANALYSIS OF RELATED WORK

The overall analysis of related work in terms of delay and power parameters is shown in below table.

TABLE I

Ref. No.	Parameters	
	Delay(ns)	Power(mw)
[1]	9	2.9
[2]	-	12.217
[3]	4	6.5
[4]	40.250	-
[5]	29.84	62
[6]	4.788	-

IV. PROPOSED MULTIPLIER

From overall analysis of related work, it is observed that number of researchers have designed multiplier to reduce delay and power. The proposed work is to design a high

speed 32-bit single precision Floating Point Complex Multiplier using Vedic Mathematics. Many authors have designed a multiplier only for a floating point number calculation. But, floating point number calculation technique is not sufficient for the large electronic system. Therefore, a high speed technique is needed for the floating point multiplication. Hence, a high speed 32-bit single precision Floating Point Complex Multiplier using Vedic Mathematics is proposed in this paper. In this technique the partial products and their sum is calculated in parallel due to which floating point compilers will operate at less clock frequencies and thus the power consumption is also reduced. Another major advantage is that the Vedic Multiplier has the regular structure and it can be easily layout on a chip.

The diagram for the proposed implementation of 32 bit floating point complex multiplier is given below.

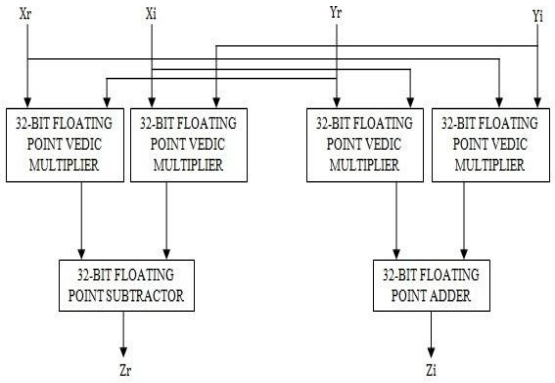

Figure 4: Proposed Block Diagram of 32 Bit Floating Point Complex Multiplier.

The proposed complex multiplier is composed of four real multipliers, one adder and one sub-tractor. Each 32 bit floating point complex multiplier takes two terms one is real and another is imaginary for the complex multiplication.

V. CONCLUSION

Most of the researchers presented design methodology for the multiplication of only integer numbers. Some of the authors used conventional algorithms for the fixed point complex number multiplication. From overall analysis of the literature it is observed that the delay and power for various multipliers are more which can be minimized with the proposed technique.

The proposed 32 bit single precision floating point complex multiplier using Vedic mathematics technique shall give faster computational speed.

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