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Review on Design of HDLC Protocol using HDL

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Abstract: Protocols are needed for efficient data communication over network. They are specified for each layer of the OSI or TCP/IP reference model by standards engineering organization. HDLC i.e. High level data link control protocol is one of the protocols defined by International Organization for Standardization (ISO) for data link layer of OSI reference model. HDLC is bit oriented protocol and it is most widely used in the network. There are different methods of designing and implementing the protocol. This paper presents different approaches of designing the HDLC protocol using hardware description language and its implementation using software tools.

Keywords: HDLC, VHDL, FCS, FPGA, Verilog HDL, Xilinx.

I. INTRODUCTION

HDLC stands for High level data link control protocol. It is a bit orientated protocol and sends information as a sequence of bits. HDLC protocol is specified for data link layer of OSI reference model. HDLC protocol is a common protocol in networking. SDLC protocol was adopted by IEEE and defined as HDLC. This protocol is used to send data over communication channel.

It was developed by the International Organization for Standardization (ISO). It falls under the ISO standards ISO 3309 and ISO 4335. It sends the data in the form of frames. The frame has to follow a predefined format called as frame structure. Every frame starts and ends with flag sequence field. Then address field holds the address of the receiving station. Control field holds the control code. Data field is the information to be transferred. Frame Check Sequence FCS adopts the CRC as calculating polynomial. The control field varies depending on the mode of operation. A frame contains error checking information which allows data to be sent reliably from a sender to a receiver

There are three modes of operations: Normal Response Mode (NRM), Asynchronous Response Mode (ARM), Asynchronous Balanced Mode (ABM). HDLC specifies the following three types of stations for data link control: 1.Primary Station, Secondary Station, Combined Station. HDLC also defines three types' ofconfigurations for the three types of stations: Unbalanced Configuration Balanced Configuration, Symmetrical Configuration.

It specifies a packetization standard for serial links. It has found itself being used throughout the world. It has been so widely implemented because it supports both half-duplex and full-duplex communication lines, point-to-point and multi-point networks, and switched or non-switched channels. Other benefits of HDLC are that the control information is always in the same position, and specific bit patterns used for control differ from those in representing data, which reduces the chance of errors. If errorsoccurs, it is detected at the receiver side. It has also led to many subsets. Two subsets widely in use are Synchronous Data Link Control (SDLC) and Link Access Procedure-Balanced (LAP-B).

Thus this paper describes the review work on design of HDLC protocol using hardware description language and its implementation by using the different software tools.

II. LITERATURE REVIEW

The research papers on the design of HDLC protocols are published in various journals and presented in many conferences. Here the paper selected describes the design of protocol using VHDL or Verilog language which includes the design of transmitter and receiver. Some of the papers present the design of protocol for particular application. They have designed the protocol according to the requirements of application.The clock requirement; synchronization requirement for every design is different. The CRC polynomial selected can be 16-bit or 32-bit.Mostly CRC-16 has been used.Most papers have used FSMs to design the transmitter and receiver of their controller.

Syed Manzoor Qasim and Shuja A. Abbasi [1] presented the design of single channel HDLC protocol. They designed the transmitter, coded in VHDL and implemented in Xilinx Virtex FPGA. The HDLC Transmitter consists of the following main blocks as shown in figure 1:-Transmitter Controller Transmit Register, Address Insertion, Frame Check Sequence (FCS) generation, Bit Stuffer, Flag/Abort Generation.

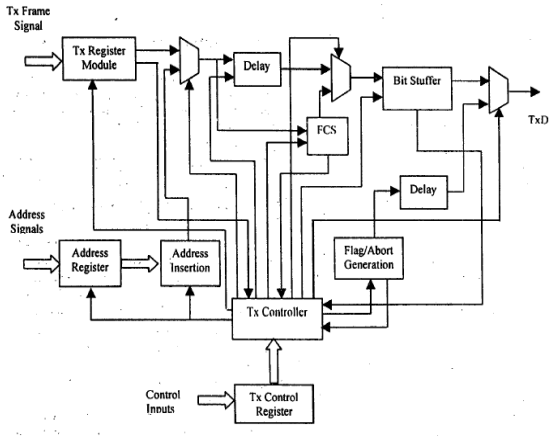

Fig.1 Block diagram of transmitter

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They achieved frequency of 59.2 MHz with a total equivalent gate count 574. It is suitable for Frame Relay switches, Video conferencing on ISDN, ISDN B-channel, SONET Termination, X.25 layer-2 protocol, Cable Modem, Private packet data networks & switches.

S. Hamed Javadi and Ali Peiravi [2] designed the HDLC transceiver and implemented in Xilinx VirtexII FPGA. The maximum bit rate of 85 MHz achieved. The signals of controller are compatible with MT8952 produced by Zarlink which are used in industry and also compatible with ST bus format. The designed HDLC controller uses the available resources of the target technology efficiently, so it is possible to integrate it with other systems. This HDLC controller is based on a modified MT8952B controller as shown in figure 2.

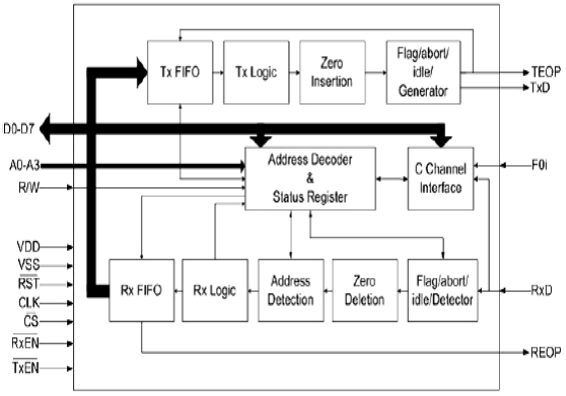

Fig. 2HDLC controller

This transceiver is useful in packet switchingand ISDN for its D-channel. K. Sakthidasan, Mohammed Mahommed [3] presented the design of transceiver in VHDL and implemented in Xilinx virtex FPGA. The codes were simulated by Modelsim. It can be used in MODEMS where error detection part is performed by this HDLC controller. It also support ISDN frame format and thus the flexibility in this controller is very high. The block diagram of controller designed is shown in figure 3.

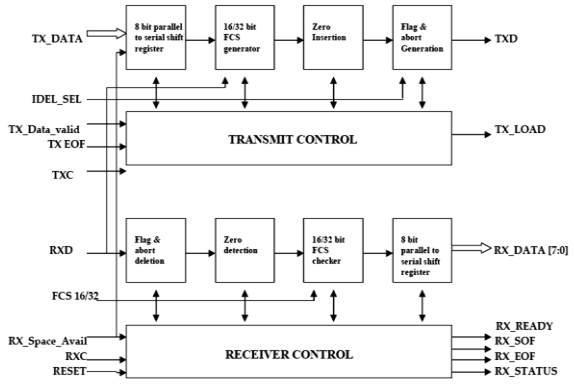

Fig. 3 Block diagram of controller

The multichannel HDLC transceiver [4] operates at frequency of 70.64 Mbps. The design was coded in Verilog HDL and synthesized with Xilinx Virtex FPGA as target device. Its functional simulation was carried out using Modelsim simulator. The HDLC protocol transceiver consists of the following main blocks:-Control unit and Registers, Transmitter, Receiver, Dual port RAMS and RAM management unit, Interrupt Controller. Figure 4 shows the block diagram of HDLC transceiver.

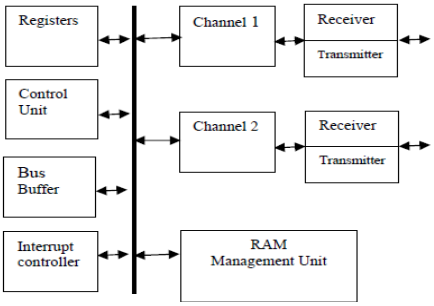

Fig. 4 Multichannel HDLC transceiver

The transceiver is designed for the full duplex communication. The authors of paper [5] presented the design of HDLC transceiver in Verilog HDL language. They implemented the design in VCS synpsys simulation tool.The proposed HDLC transmitter has 3 components, which are- FIFO, zero stuffing and transmission. Figure 5 shows the block diagram of the transmitter.

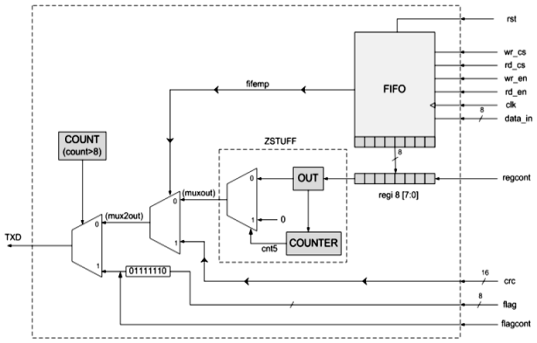

Fig. 5 HDLC transmitter

The architecture for the HDLC receiver is shown in figure 6:-

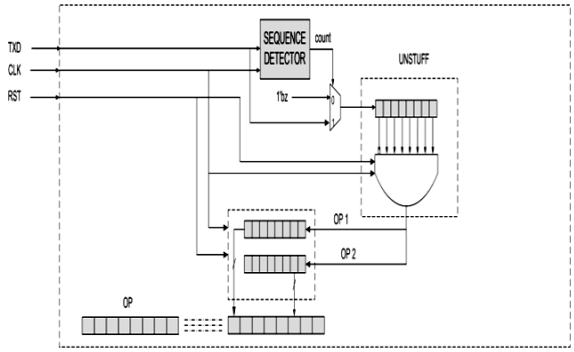

Fig. 6 HDLC receiver

Gaurav Chandil, Priyanka Mishra [6] presented design of HDLC controller. The coding done in VHDL and implemented by using FPGA Spartan 3 device. It offers highest frequency of 155.52 Mbps.The signals of thiscontroller are compatible with ITU q.921.X.25 level 2 recommendation.The block diagram of transceiver is shown below:-

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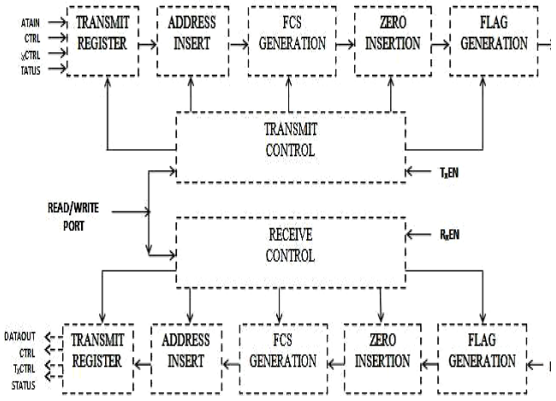

Fig. 7 HDLC transceiver

HDLC controller design supports full Duplex and half duplex mode of operations.It is CCITT X.25 compatible.
Jai Karan Singh1, Mukesh Tiwari, Mohd Firoz Warsi proposed a broadband radar system communication [7] in which control computer gives instruction and also receives the results from radar signal processor ,HDLC controller exchange the data between radar signal processor and control computer. Figure 8 shows the block diagram of the system. HDLC controller is designed according to communication requirements of baud rate less than 4 Mb/s,the communication distance does not exceed 10 meters, the error rate less than 10-6. The designed HDLC controller has the following features: receiving and sending module programming control, query/interrupt working mode, 8-bit station address freely set, data overflow/CRC error detection, DDR-SRAM memory.

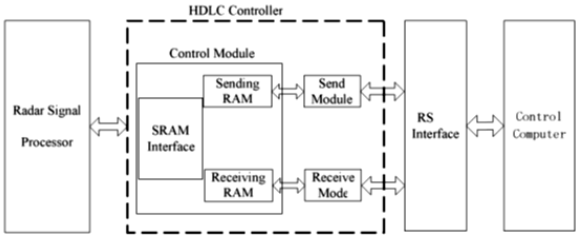

Fig. 8 Block diagram of Radar communication system

HDLC controller designed in Verilog with ISE 12.1 and simulated in Modelsim 6.3. Shubham Fadnavis [8] designed HDLC protocol for error detection and correction. This is application based paper which presents high efficient combined error detection and correction technique based on horizontal-vertical diagonal parity check in HDLC. This method has been experimentally implemented and simulated using field programmable gate array. Simulation results show that the proposed technique detects 99.99% of the errors and corrects as predicted up to three bits of errors in the received impaired n-bit code. The design was implemented in Xilinx 8.1 using Modelsim SE-EE for simulation.

The authors [9] designed the HDLC protocol for data communication. In designed communication system, data is first compressed, transmitted by using HDLC frame and received by the receiver. To select the 32 Channels information, multiplexer is used. The system has 32 bit multiplexer, channel counter, FIFO (first in first out), RLE Compressor and HDLC Framing at the transmission end. A 32 bit de-multiplexer, FIFO (first in first out), RLE Decompressor and a HDLC De-framing at the receiving end. The architecture of system is shown in figure 9.

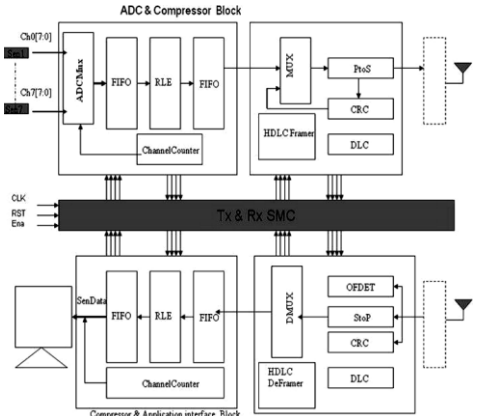

Fig. 9 Block diagram

All the modules are coded in VHDL and implemented in Xilinx Spartan-3 device.

III. COMPARISON TABLE

Ref. paper No	Bit rate	Features	Software tool used
[1]	59.2 Mbps	1.Transmitter is designed	Xilinx Virtex FPGA, Modelsim
[2]	85 Mbps	Compatible with ST bus format, MT8952 ZARLINK HDLC Controller, Transceiver designed.	Xilinx VirtexII FPGA, Modelsim
[3]	-	Transceiver designed	Xilinx Virtex FPGA, Modelsim
[4]	70.64 Mbps	Multichannel transceiver is designed	Xilinx Virtex FPGA, Modelsim
[5]	-	Transceiver designed by Verilog hdl.	VCS Synopsys
[6]	155.52 Mbps	Transceiver designed.	FPGA Spartan 3 device., Modelsim
[7]	4 Mbps	1. HDLC controller is designed for radar communication	XILINX ISE 12.1, Modelsim 6.3.
[8]	-	1. This technique detects 99.99% of the errors 2. It corrects as predicted up to three bits of errors	Xilinx 8.1, Modelsim SE-EE 5.4A
[9]	-	1. They designed the system in which data is compressed ,then transmitted and received using HDLC	Xilinx Spartan-3

IV. CONCLUSION

The study of papers shows different approaches of designing the HDLC protocol using hardware description language. It has been found that HDLC controller for transmitter and receiver is designed in VHDL or Verilog language and then implemented using various software tools. The authors designed protocol at the different bit rate and highest bit rate of 155.52 Mbps is achieved. It is also observed that the HDLC protocol is designed according to the requirements of particular application. Thus this review gives brief idea that by designing the HDLC protocol in hardware description language, the protocol can be made more efficient and its speed can be increased. Hence it can be used in more application, making it more flexible and upgradable.

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