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A Comparative Study of SRAM Cells

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Abstract: This paper discusses seven variants of SRAM Cells that are most commonly used in present electronic circuits. A comparison with respect to number of transistors, average delay, average rise/fall time, peak power and average power is drawn at the end of this paper.

Keywords: SRAM, Low Power VLSI, 6T SRAM, SRAM Working, Memory.

I. INTRODUCTION

Memory is one of the most crucial things of any computing or storage device. It occupies a significant amount of space inside the device and accounts for a considerable fraction of the total power consumed by the device. With the advent of mobile technology accompanied an immense need to minimize the power consumption of electronic devices. A number of driving forces behind this like increased demand for portable computers, high performance systems, and environmental concernsare listed in [1]. Out of these the most prominent one is the need to reduce the size of the device while making it last longer on a single charge. Owing to Moore's law [2] and rapid innovation in the manufacturing sector, electronic circuits today are scaling at a much rapid rate than ever before with no signs of slowing down. This means that the circuits are becoming smaller with every passing day but consuming more power. Batteries on the other hand cannot be scaled to the same extent. These factors further stress on the need to design and construct low power circuits. As a result of its ubiquity in electronic devices and high packing density, memory (particularly SRAM) plays a very important role in reducing power consumption. This paper presents a comparative study of the most commonly used SRAM cells with respect to power consumption, delay, rise/fall times and area. The results are based on computer simulations done using Cadence software using spectre simulator at 45nm technology.

II. 6T SRAM

Figure 1 shows the structure of a 6T SRAM cell which is most commonly used in many circuits. The read and write operations of this cell is explained. During the write operation, BL and BLB are set to the value that has to be written and its complement respectively and WL is asserted. That is, to write 1 into the cell, BL is set to HIGH while BLB is set to LOW. When WL is made HIGH, access transistors NM2 and NM3 pass these values into the cell. Setting Q to 1 turns ON NM1 setting QB to LOW. Similarly,setting QB to 0 turns ON PM0 setting Q to HIGH. Since PM1 and NM0 are turned OFF, there is ideally zero current flowing through the circuit. Writing 0 into the cell follows similar set of operations. In this case PM1 and NM0 are turned ON while PM0 and NM1 are turned OFF. This makes Q become 0 and QB 1.

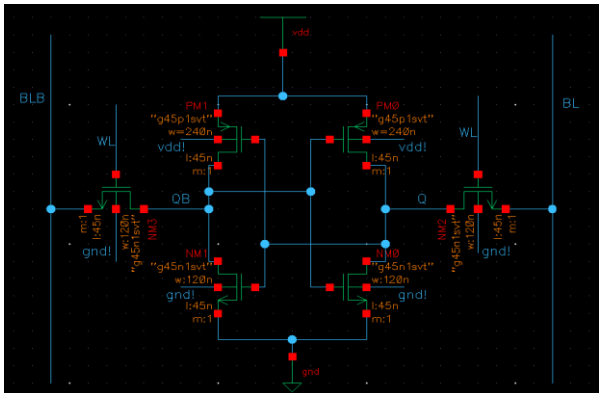

Fig.1. Circuit of 6T SRAM Cell

III.7T SRAM

In circuit of figure 2, we can further prevent leakage current by including a pass transistor NM7 to control the path to ground [3]. NM7 is turned ON when the cell is operational and it turned OFF during the standby state. This prevents any leakage current from flowing to the ground. This design is especially useful in memories that spend a significant fraction of their time in standby state.

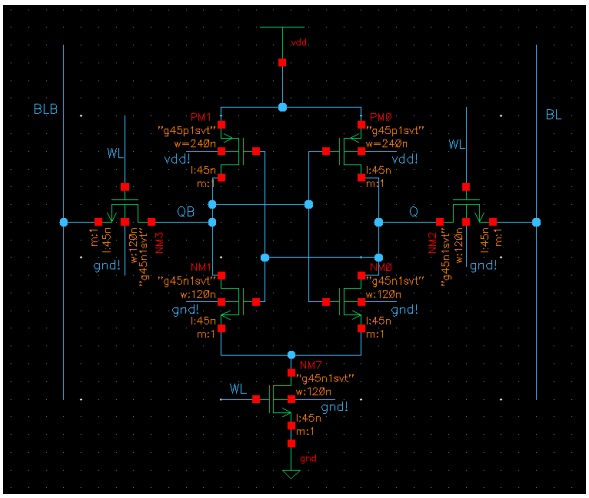

Fig2. Circuit of 7T SRAM Cell

IV.8T SRAM

P N Vamsi Kiran et al also propose in [3] another design

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of the SRAM cell that uses 8 transistors. In this design two additional sources are used to write into the cell. This reduces the voltage swing on the bit lines BL and BLB.

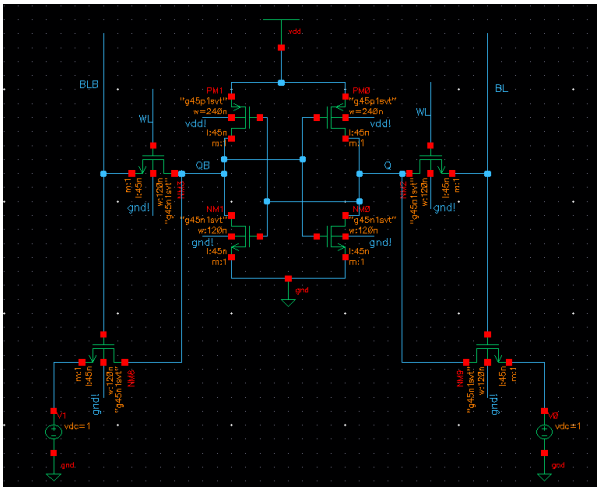

Fig.3. Circuit of 8T SRAM Cell

V. 9T SRAM(1)

One of the main disadvantages of 6T SRAM is that when WL is HIGH and a new value is written into the cell, for a brief instant of time both NMOS and PMOS transistors will be turned ON. This causes short circuit current to flow from VDD to GND. For instance, when we change the value stored in the cell from 0 to 1, Q raises from LOW to HIGH while QB falls from HIGH to LOW. During this process, when Q and QB is approximately VDD/2, NM0, NM1, PM0 and PM1 will be ON. This results in a current flow from VDD to GND. To prevent this, we add a pass transistor NM4 and turn it OFF during the write operation.

This prevents this short circuit current from dissipating excess power. But, adding this comes at a cost of additional voltage drop across the transistor. To compensate for it, we replace the pass transistors NM2 and NM3 with transmission gates. Since, transmission gates propagate both strong 1 and strong 0, the voltage drop is reduced. This circuit is proposed in [4] and is depicted in figure 4.

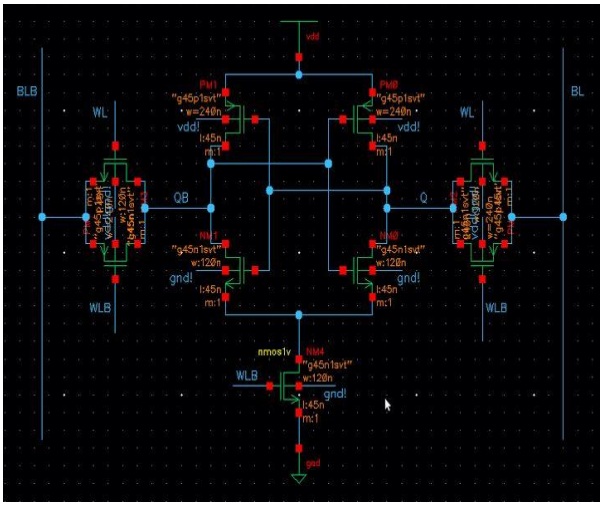

Fig.4. Circuit of 9T SRAM (1) Cell

VI. 9T SRAM(2)

A variation of the above circuit is discussed in [5]. In this circuit, instead of the NMOS pass transistor used to cut off a path to GND, a PMOS pass transistor is used to cut off the supply form VDD when not required.

This provides additional advantage as it prevents even the intermediate nodes from charging and discharging when not needed. This is shown in figure 5.

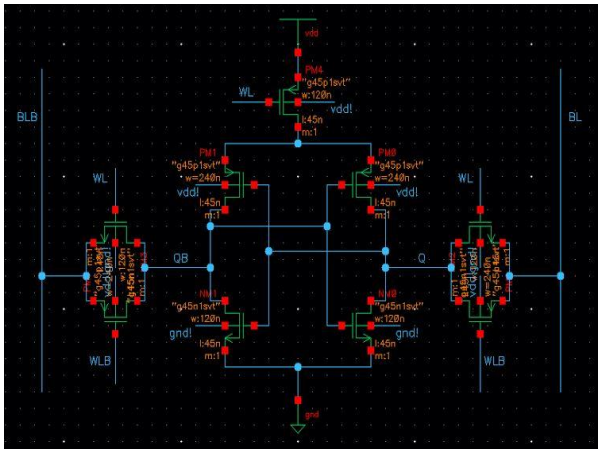

Fig.5. Circuit of 9T SRAM (2)

VII. 9T RAM(3)

Yet another variation of a 9T SRAM is shown below. This design is mentioned in [3] and is depicted in figure 6. This is very similar to the one in figure 2 except for the two pass transistors that is connected to GND through NM7.

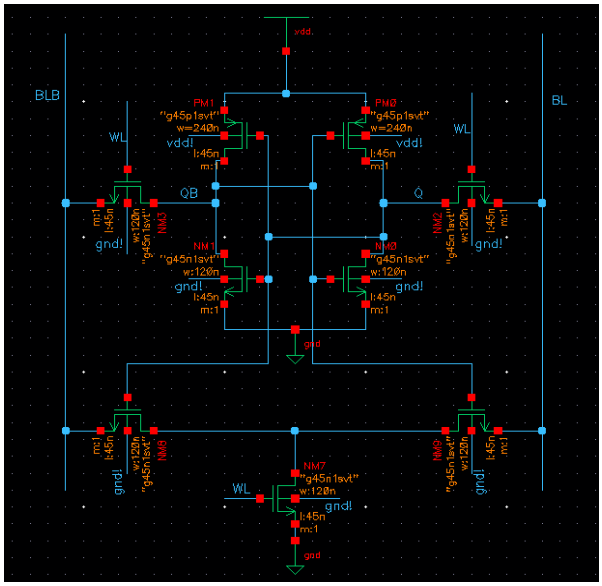

Fig.6. Circuit of 9T SRAM (3)

VIII. 10T SRAM

Figure 7 shows a 10T SRAM cell as mentioned in [5]. This is a combination of designs in figure 4 and figure 5. While it achieves lower power dissipation than either circuit, it occupies more area owing to the presence of an extra transistor. Also, the rise time and fall time of the circuit worsens.

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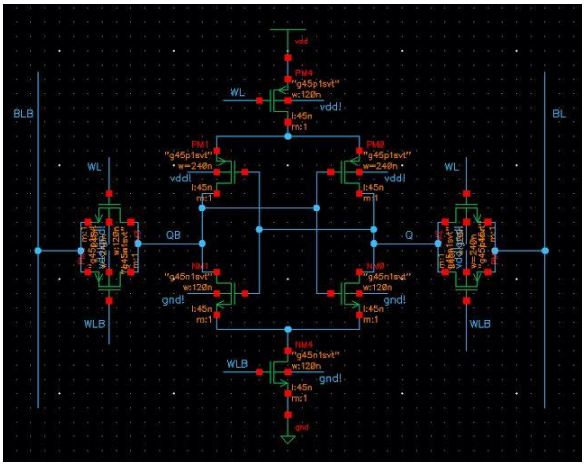

Fig.7. 10T SRAM Cell

IX. RESULTS

All of the above circuits were simulated using spectre simulator in Cadence software at 45nm technology. Power analysis has been carried out to determine the average power and peak power dissipated in the circuits as per procedure established in [6].

The output waveform of 6T SRAM cell is shown in figure 8 and its power dissipation is depicted in figure 9. The waveforms of other designs are similar and hence are not provided. Table 1 provides the results obtained for each SRAM Cell.

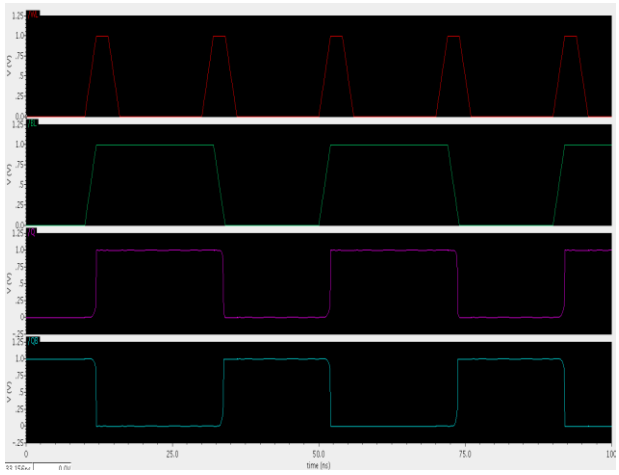

Fig.8. Output Waveform

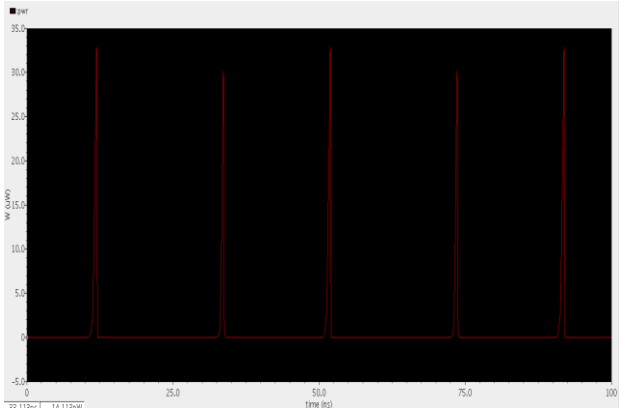

Fig.9. Power Dissipation

	TRANS. COUNT	AVG. DELAY (PS)	AVG (RISE / FALL) TIME (PS)	PEAK POWER (µW)	AVG. POWER (µW)
6T SRAM	6	835.0	72.565	32.93	0.6437
7T SRAM	7	630.2	78.65	25.4	0.3696
8T SRAM	8	787.5	96.65	32.03	0.6494
9T SRAM(1)	9	340.3	362.0	14.52	0.3135
9T SRAM(2)	9	262.2	650.0	5.671	0.1357
9T SRAM(3)	9	855.5	72.675	46.3	0.9137
10T SRAM	10	259.3	817.5	4.817	0.095

X. CONCLUSION

From the above table it can be concluded that there is a tradeoff between various parameters as we go from one SRAM cell to another. 10T SRAM consumes the least amount of power of all circuits and has the smallest delay. But it occupies largest area due to more number of transistors. The average rise time and fall time of it is also the largest among all cells which limits its usage in practical circuits. 6T SRAM has the least number of transistors and occupies least area on a chip. It also has the least average rise and fall times. But, it has one of the highest power values and delay which renders it less efficient. 8T SRAM and 9T SRAM cells fall in between these two extremities and provide moderate power consumption, delay, average rise and fall time values.

The choice of SRAM is left to the user and is highly dependent on the application. The parameters mentioned in Table 1 have to be carefully studied before making a decision about it.

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