ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 3, Issue 5, May 2015

Non-Conventional Multi-level Inverter with Reduced Number of Voltage Sources and Switches

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Abstract: Multilevel inverters have got high quality output when compared with two-level inverters so for high power purposes the usage of Multi-level inverter applications has grow more ubiquitous in industries. In this paper, foremost a new topology for sub-multi level inverters is proposed and then the series connection of sub-multilevel inverters is put forth as a generalized multilevel inverter. This proposed multi level inverter has reduced number of switching devices. The optimal structure concerning the criteria such as standard voltage on the switches, number of switches and number of dc voltage sources etc is succeed by paying a special attention. Asymmetric condition is verified for proposed multilevel inverter by using MATLAB SIMULINK software.

Keywords: Multilevel inverter, Optimal Structure, Sub-Multilevel inverter, Asymmetric condition, MATLABSIMULINK software.

I. INTRODUCTION

Nowadays, for high power and high voltage applications, Multi-level inverters are used because of their advantages like its output voltage has got lower electromagnetic interference, reduced harmonic distortion, high efficiency. Multi-level inverters includes power semiconductors devices and dc voltage sources, the output is generated with voltages of stepped waveform. In Multi-level inverters, required ac output voltage waveform can be obtained by various combinations of multiple dc voltage sources. As the number of voltage sources increased, the quality of output voltage is much improved. However, a larger number of levels increase the number of devices that must be controlled and the control complexity [9].

There are three well-known types of Multi-level inverters [10],[11]: the neutral point clamped (NPC) or diode clamped multilevel inverter, the flying capacitor (FC) multilevel inverter, and the cascaded H-bridge (CHB) multilevel inverter. All those three conventional single phase inverters for three level output are shown in Fig(1).

The NPC Multi-level inverter has got the drawback of the unequal voltage distribution between the series connected capacitors, which causes the dc-link capacitor unbalancing and require large number of clamping diodes for a large number of voltage levels [2]. The FC multilevel inverter uses flying capacitors as the clamping devices and this type topology has got several advantages when compared to NPC Multilevel Inverters, also with the advantage of having redundant phase leg states which allows the equal distribution of switching stress among the semiconductor devices [7] and [8] and also the transformer less operation.

The topologies of CHB have got good modularity and simplicity of control and so they are suitable for high-voltage applications. But, the drawback of this topology is it requires large number of separated voltage sources to supply each conversion cell. To overcome this drawback for high voltage applications, new configurations have been developed [3-6]. Multi-level inverters also got some particular disadvantages like, they require large number of power semiconductor devices, which leads to increase in the cost and complexity in controlling and tend to reduce the efficiency and overall reliability.

Among all those three Multi-level inverters, cascaded inverters got many advantageous and are preferred mostly. Based on the voltage balancing of inverter topologies, inverters can also determine as symmetrical [1-4] and asymmetrical inverters [5-6].

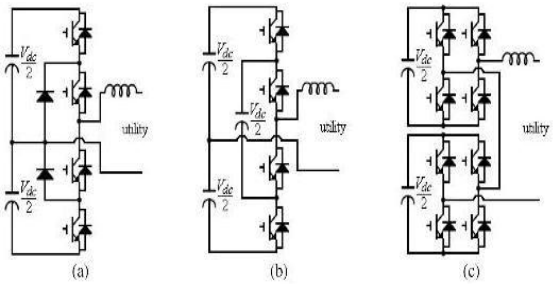

Fig 1. (a) Diode Clamped Multilevel Inverter (b) Capacitor Clamped Multilevel Inverter (c) Cascaded H–Bridge Multilevel Inverter.

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In past years, lot of configurations and topologies are presented in order to reduce the total number of devices. Some among them are proposed in the literature [3-6]. This paper present a new multilevel inverter topology using series connection of sub-multilevel inverter which requires less number of power electronic devices as compared to conventional inverters.

II. CONVENTIONAL SEVEN – LEVEL INVERTERS

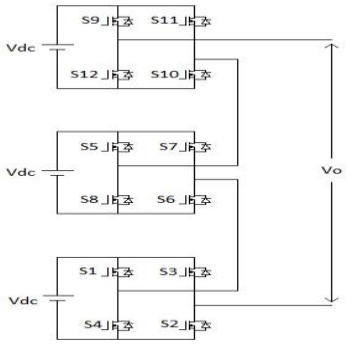

Fig 2. Seven – level Cascaded H–Bridge Multilevel Inverter

A cascaded H – bridges Multi-level inverter is a series connection of multiple H – bridge inverters. Each H – bridge inverter has the same configuration as a typical single phase full-bridge inverter. The circuit configuration of seven – level cascaded H – Bridge inverter is shown in Fig(2). It requires 12 IGBT switches and 3 DC sources for a seven – level inverter.

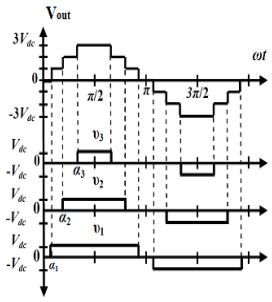

Fig 3 : Output Voltage of cascaded H-bridge seven level inverter

Each H-bridge inverter is connected to its own DC source Vdc. It introduces the idea of using Separate DC Sources (SDCSs) to produce AC voltage. By cascading AC outputs of each H-bridge inverter, AC voltage waveform is obtained. Lot of topologies are developed in recent year, with this idea.The proposed topology in this paper is also based on the same working principle.

III. PROPOSED TOPOLOGY

Configuration circuit shown in Fig(4) is of a seven – level inverter. It comprises of two constant DC voltage sources V1 and V2 and eight switches (S1, S2, S3,S4, T1, T2, T3 and T4), among those four switches(S1, S2 ,S3 ,S4) are used at voltage sources for voltage level control and output obtained from these switches is similar to the output obtained from a full wave rectifier. And then the remaining four switches are used as CHB inverter. This CHB is used for maintaining positive and negative parts of output voltage waveform. At the output terminals of CHB

Mode	S1	S2	S3	S4	T1 T2	T3 T4	Vo
1	OFF	ON	OFF	ON	ON	OFF	3Vdc
2	ON	OFF	OFF	ON	ON	OFF	2Vdc
3	OFF	ON	ON	OFF	ON	OFF	Vdc
4	ON	OFF	ON	OFF	ON	OFF	0
5	ON	OFF	ON	OFF	OFF	ON	0
6	OFF	ON	ON	OFF	OFF	ON	-Vdc
7	ON	OFF	OFF	ON	OFF	ON	-2Vdc
8	OFF	ON	OFF	ON	OFF	ON	-3Vdc

inverter the load is connected. Therefore, by using CHB inverter at the end, all the generated positive half – cycles will be converted into positive and negative half – cycles.

A, Operation Principle

The seven – level inverter operation can be divided into eight modes. Modes 1 – 4 are for the positive half – cycle and modes 5 – 8 are for the negative half – cycle. As shown in Fig(2), the power electronic switches in CHB inverter are switched synchronously with the utility voltage to convert the DC power into AC power for commutating and in low frequency.

As the DC constant voltage sources are unequal, the magnitude of DC constant voltage sources V1 and V2 can be shown as follows,

$$V1 = Vdc,$$
$$V2 = 2Vdc$$

Switches T1 and T2 are turned ON for positive half-cycle and at this time switches T3 and T4 are turned off. Now switches T3 and T4 are turned ON for negative half-cycle and at this time T1 and T2 are turned OFF.

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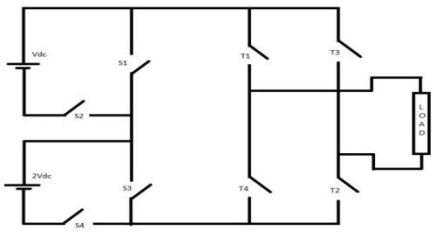

Fig 4 : Seven – Level Proposed Topology

The switching modes and output voltages of seven – level inverter are shown in table(1).

The operating modes of proposed seven – level inverter are as follows,

Mode1**:** In this mode, the output voltage is 3Vdc (V1+V2) as shown in Table(1). In this, switches S2 and S4 are turned ON and switches S1and S3 are turned OFF. The load current path will be through S2 – T1 – Load – T2 – S4.

Mode2**:** In this mode, the output voltage is 2Vdc (V2) as shown in Table(1). In this, switches S4 and S1 are turned ON and switches S2 and S3 are turned OFF. The load current path will be through S1 – T1 – Load – T2 – S4.

*Mode3***:**In this mode, the output voltage is Vdc (V1)as shown in Table(1). In this, switches S3 and S2 are turned ON and switches S1 and S4 are turned OFF. The load current path will be through S2 – T1 – Load – T2 – S3.

*Mode4***:**In this mode, the output voltage is '0'. In this, switches S3 and S1 are turned ON and switches S2 and S4 are turned OFF. The load current path will be through S1 – T1 – Load – T2 – S

Table (1) Switching Table of Seven – level Inverter

Similarly the principles of working of modes 5,6,7 and 8 are similar to modes 4,3,2 and 1 respectively. But the modes from 5 – 8 are for negative half – cycle, so,switches T1 and T2 turned OFF and switches T3 andT4 are turned ON. The output voltage obtained from modes 5 – 8 are 0, -Vdc, -2Vdc and -3Vdc respectively. Therefore, total seven output levels of proposed topology are as follows +3Vdc, +2Vdc, +Vdc, 0, -Vdc, -2Vdc and -3Vdc.

IV. SIMULATION RESULTS

MATLAB SIMULINK based simulation tool is used to validate the results of proposed topology. 7 – level output voltages are as shown in Figure. Fig(7) shows the final output voltage of 7 – level inverter, and Fig(6) shows the half wave output voltage .

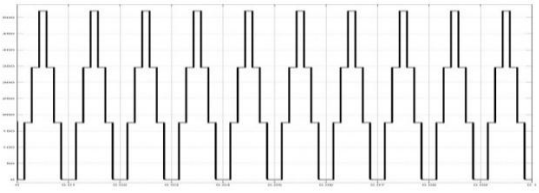

Fig 6. Generated positive half - cycles

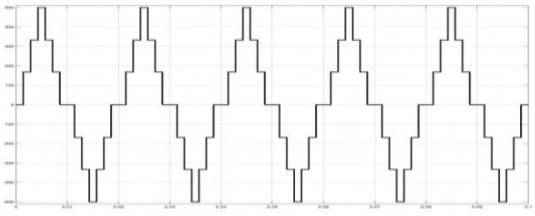

Fig 7. Seven – level output voltage

All the output voltages are obtained for resistive load of "100Ω". Hence, the current waveforms are also similar to voltage waveforms, but the difference is in magnitude only.

V. CONCLUSION

In this paper, a new topology has been introduced for Cascaded Multi-level inverters. The proposed topology results in reduction of cost and installation area as the number of voltage sources and switches are minimised. This configuration extends possibilities to optimize it for various objectives and the design flexibility. The simulation results for proposed multilevel inverter topology demonstrate that the proposed configuration has prominent feature compared to other Cascaded Multi-level inverters.

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Vol. 3, Issue 5, May 2015

BIOGRAPHY

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