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A Survey Approach - Multiprocessing on FPGA using Light Weight Processor

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Abstract: These Multiprocessors have been widely used in modern high performance embedded system to meet the computational needs of smart, real time applications spread across multiple domains. While custom IPs (InteUectual Property) on FPGA based systems are commonly used, multiprocessing on FPGAs have not been explored enough due to concerns about meeting a right trade-off between area usage, achievable performance, and the required design time. Multiprocessor embedded systems (MESes) are a very promising approach for high performance yet relatively low-cost computing. This paper presents an implementation of a multiprocessing system on FPGA using multiple light weight soft processors (LWP) that work in conjunction with a custom hardware to achieve balanced performance to resource ratio. As an example we have implemented a TDEA (Triple Data Encryption Algorithm).simulation is done by using Xilinx and implementation is done by using FPGA.

Keywords: Multiprocessing, TDEA, Field Programmable Gate Array (FPGA), MicroBlaze

I. INTRODUCTION

The increase in capacity of Field Programmable Gate Arrays (FPGAs) made it possible to include many microprocessors within a System On Chip (SOC). Multiprocessing systems are systems with more than one processing element which can execute several processes simultaneously. As technology advanced, it began to be possible to integrate in a chip a complete multiprocessing system. In this respect, FPGA's (Field Programmable Gate Array) emerge as a new and promising platform to implement multiprocessing systems. FPGAs enable fast prototyping and research of new architectures without ASIC (Application Specific Integrated Circuit) related problems.

Open source processors do not have these limitations, but aspects like design quality, support and documentation can become a bottleneck. A good solution to the bottlenecks of such ad-hoc designs is also given in Combinational and sequential elements are explicitly separated to clarify time dependencies between processes. The algorithm is completely determined by the Combinational process.

Computer networks play an important role in computer science as well as in today's life. They allow communicating easily on large distances. In recent years the computer networks have been growing at a very high rate and the data throughput has grown dramatically. The data in the networks are usually sent in a form of packets. The packets are transmitted from a source to a destination by network appliances like switches or routers. Network processors are a class of processors which are targeted on the network appliances. These devices manipulate the frames of data flowing in the computer networks.

Majority of FPGA-based multiprocessing that has been previously explored make use of commercially available soft processors from vendors like Altera and Xilinx. While multiprocessing on FPGA has been feasible, not many solutions have been explored due to existing tradeoff between a processor based solution and a custom design solution.

Several techniques are applied to solve hazards. For data hazards forwarding is applied to reduce the number of stalls to a minimum. The structural hazard which occurs when the same register is read and written concurrently is also solved using operand forwarding. When the result of a load instruction is immediately used, these techniques cannot be applied and a stall will be inserted in the pipeline. Finally, control hazards are solved using a pipeline flush. Custom designs are always high in performance but they come at the expense of chip area and power. Processor based solutions are efficient in terms of area but low in performance.

In addition, specific processor architecture is not suited to different application domains. For example, a DSP architecture that is suited for low-to-moderate performance image, video, or wireless processing, is not efficient for wired networking applications such as switching/routing. FPGA vendors provide their own soft processor solutions that can be configured to suit a designer's requirement. These are general purpose soft processors widely used in multiple applications. The multiprocessor abstraction retains the advantage of software programmability and provides an easy way to deploy applications from an existing code base. FPGAs also allow the designer to customize the multiprocessor for a target application. Designers can iteratively explore other configurations or offload critical functions into co-processors on the fabric to improve performance.

II.LITERATURE SURVEY

A paper "Multiprocessor system in an FPGA" International Conference on Reconfigurable Computing and FPGA's" [1] concluded with the main objective which consisted in the design and implementation of a

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multiprocessor system in a FPGA. The main contributions involving in the paper can be summarized as Design of a homogeneous multiprocessor system with distributed memory and streaming communication. Development and comparison of two different communication architectures, a crossbar switch based architecture and NoC based with mesh topology architecture. Evaluation of scalability and performance of the Crossbar Switch based architecture. Acceleration of a matrix multiplication test application through mapping on a multiprocessor system with increasing number of cores. Implementation of a four cores multiprocessing demonstration system in a Spartan-3E device and concluded that being able to broadcast data is extremely important in parallel applications, because it reduces significantly the communication delay.

A paper “An FPGA-based Soft Multi-processor System for IPv4 Packet Forwarding," [2] concluded on soft processing architecture obtains the effectiveness of FPGA-based soft-multiprocessors for high performance applications. And designed a soft multiprocessor for the data plane of the IPv4 packet forwarding application and achieved a throughput of 1.8 Gbps. The paper also developed a design space exploration framework for soft multiprocessor micro-architectures. Using this framework designed a more efficient multiprocessor that achieved a 1.9 Gbps throughput surpassing the performance of hand-tuned design. From the study of paper [3], soft multiprocessors on FPGAs only lose a 2.6X factor in performance normalized to area compared to a network processor implementation for the IPv4packet forwarding application. If a high-performance programmable platform already exists for an application niche, then it is a cost-effective implementation medium.

A paper “Definition and SIMD implementation of a multi-processing architecture approach on FPGA" [4] described work is a promising solution to implement the new generation of computation intensive signal or image processing systems. Compared to classical FPGA implementations, not only it allows to dramatically reduce development and evolution costs but it also gives access to sophisticated data dependent algorithms such as the ones required to make systems more intelligent. In fact, seen from industries dealing with long lifecycle, it gives access to similar features as the ones offered by emerging technologies such as massively parallel processing or reconfigurable computing but provides a much more secure way to guarantee long term availability. Moreover the platform approach with an API as suggested for probably a way to allow a smooth transition toward those emerging technologies when they are mature.

A paper "iDEA: A DSP Block Based FPGA Soft Processor", [5] introduced DSP Extension Architecture (iDEA), an instruction set-based, soft-processor built with a DSP48E1 primitive as the execution core and harness the strengths of the DSP48E1 primitive by manipulating its functionality to suit the architecture of a load-store processor. The DSP48E1 primitive is designed for signal processing implementations, but showed that it is capable of supporting all the required arithmetic functionality for a basic processor. As iDEA is designed to occupy minimal area, the logic is kept as simple as possible. By limiting the addition of hardware modules such as branch prediction able to minimise control complexity. The processor has a basic, yet comprehensive enough, instruction set for general purpose applications. Using three C applications – Fibonacci, FIR and Median filter, showed that it is on-par with a minimised Micro-Blaze soft processor. It occupies about half as many slice LUTs and registers as Micro-Blaze while achieving about twice the frequency. paper aim to focus now on reducing the need for NOP fillers. These cause significant latency overhead and decrease code density, for what is otherwise an efficient, high speed processor. It worked on developing a compiler that will allow some of these limitations to be overcome at compilation. They have presented a DSP48E1-based processor that is minimal, yet comprehensive enough to be able to run general purpose processing tasks, rather than being tailored to specific application areas. The processor can be implemented across the next generation of Xilinx FPGAs, achieving comparable performance in all cases.

CONCLUSION

In this paper, we have shown how multiprocessing on FPGA is implemented using different processors. So implementation of light weight, high performance processors can deliver, highly competitive solutions compared to those using standard processors from existing vendors or writing custom IP. We showed the design of a 5 -stage pipelined light weight processor that makes use of DSP48E l block and minimal BRAM on Xilinx Kintex-7 device. This processor is then used as a building block of our multiprocessing system.

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