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Interphase ac-ac Converter Topology for DVR to Mitigate Voltage Sags

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Abstract: The most common and serious power quality problem is voltage sag and causes more economic losses. The definite solution for voltage related power quality problems is DVR. The conventional topologies operate with a dc link which imposes limits on the compensation capability of the DVR. This paper analyzes the characteristics of voltage dips in power systems with special emphasis on symmetrical components analysis and unbalanced dips with an ac-ac converter topology to mitigate voltage sags. These topologies require instantaneous voltages at the point of common coupling. A generalized dip model is built for all unbalanced dips, taking into account the fault types and load connections. Detailed simulations to support the same have been carried out in MATLAB, and the results are presented.

Index Terms: Dynamic voltage restorer (DVR), voltage dips, power quality, instantaneous symmetrical components.

I. INTRODUCTION

Power quality describes the quality of voltage and current a facility has, and is one of the most important considerations in industrial and commercial applications today. It is essential that processes, in particular, in industrial plants, operate uninterrupted where high productivity levels are an important factor. Power quality problems commonly faced by industrial operations include transients, sags, swells, surges, outages, harmonics, and impulses that vary in quantity or magnitude of the voltage [1]. Of these, voltage sags and extended under-voltages have the largest negative impact on industrial productivity, and could be the most important type of power quality variation for many industrial and commercial customers [1]–[3].

Voltage sags are momentary voltage variations, usually caused by a short circuit or fault somewhere in a power distribution system. Voltage magnitude is one of the major factors that determine the quality of electrical power. Computers, adjustable speed drives, and automated manufacturing processes are very susceptible to voltage sags and brief outages. The quality of power should be improved before it is used to energize any load. Voltage sag is known to produce the most devastating impact on the loads, 63% of the disturbances were single line-to-ground (SLG) faults and11% were line-to-line (LL) faults [5]. Though symmetrical faults (Symm) were 6%, deep symmetrical three-phase voltage sags were very rare [4]. Most of the three-phase symmetrical faults create symmetrical sag depth less than 50%.Voltage sags are characterized by sag depth, phase jump, and duration of sag.

Voltage sags in an electrical grid are almost impossible to avoid, because of the finite clearing time of the faults that cause the voltage sags and the propagation of sags from the transmission and distribution system to the low-voltage loads.

Dynamic Voltage Restorer (DVR) is a custom power device (CPD) that is connected in series with the network to improve voltage disturbance in the electrical system. The different sag types do affect the basic DVR design, but the prim-ary issues that influence the DVR rating for the different system topologies are the duration and depth of the voltage sags. To restore the load supply voltages the DVR injects voltage in to the line. It consists of a voltage source inverter (VSI) to inject voltage in series with the line, injection transformer, and a dc link, where the energy is stored using dc capacitors or battery energy storage.

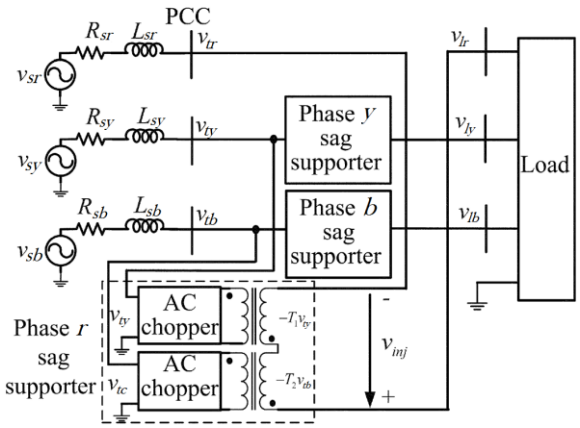

Fig 1: Interphase ac-ac converter topology

This type of DVR is not adequate for compensating deep and long-duration voltage sags. Contradictory to this, as per the sensitive load concern, deep and long-duration sags are more vulnerable than shallow and short-duration sags. The magnitude and ride-through capability of the compensator depend on the size and capacity of the storage device. Poor reliability of the storage devices and variation in the dc bus voltage may compromise the sag compensation performance. A system-wide addition of DVRs is hindered because of high cost, in particular, due to the expensive energy storage devices. Use of batteries has raised many environmental concerns. Further, the voltage regulation of the dc link demands the use of a separate ac–dc converter, which requires one more stage

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of power conversion. Thus, the compensator size, cost, control complexity, and power losses will increase. New series power conditioners are proposed based on direct ac–ac z-source, boost, buck–boost, and matrix converter topology [6]-[7]. These topologies directly convert ac voltage to regulated ac voltage without any intermediate converters.

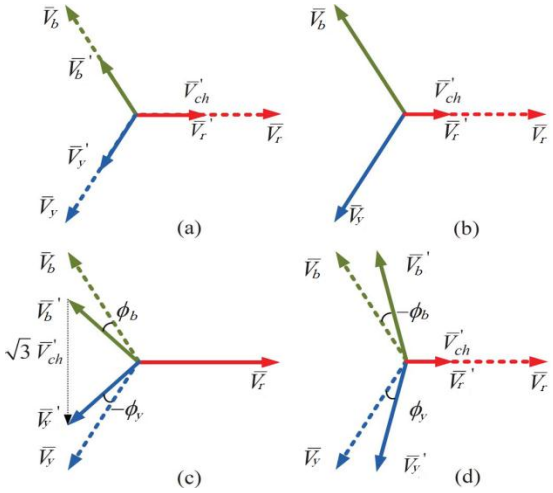

Fig 2: phasor voltages of sag types: (a) type I, (b) type II, (c) type III and (d) type IV

II. AC VOLTAGE–VOLTAGE CONVERTER MODEL

The ac voltage-voltage converter model is based on a buck converter configuration, with a step-up injection transformer used at its output. The converter incorporates fast-switching insulated gate bipolar transistor (IGBT) technology, and controls involving pulse width modulation (PWM) techniques. The model block diagram is shown in Fig. 1.

The CBEMA and ITIC curves provide the voltage tolerance requirements for computing equipments. A half cycle undervoltage is considerable for most of the devices. Although the definition of sag also states that it is a decrease in voltage for minimum of half cycle duration. The sag flag can be set when the undervoltages are less than half cycle. All the potential sags thus detected by the algorithm is characterized and the data is sent to the compensation scheme. As the algorithm uses half cycle window length, the undervoltage longer than half cycle duration i.e. sag, have the $\bar{V}_{a1}$ settled at half cycle from the sag detection. Therefore, undervoltage for less than half cycle can be identified from the slope of the $\bar{V}_{a1}$ waveform, as it moves towards 1 p.u immediately after the half cycle.

When an undervoltage is detected by the algorithm i.e., when $\bar{V}_{a1}$ crosses 0.9667 p.u, the counter C is initialized and is incremented until the voltage recovers. Once the counter value equals the duration for half a cycle as in (1), it is checked for a potential sag.

$$C\ f_s = 0.5\ T \qquad (1)$$

where, *fs* is the sampling frequency and *T* is the time period of the input voltage. If a potential sag is detected, sag flag is raised and characterized data is to be sent to the compensation scheme. Otherwise, the sag flag and counter are cleared. Fig. 3 shows the working of the proposed algorithm for the characterization of voltage sags.

The two parameters quantifying the dip are the characteristic voltage $\bar{V}'_{ch}$ and the called PN factor F, both complex numbers. The phase voltages as a function of these two parameters are, for a type III_r dip

$$\begin{aligned} V_r &= F\ ; \\ V_y &= -\frac{1}{2}F - \frac{1}{2}\bar{V}'ch\sqrt{3}\ ; \\ V_b &= -\frac{1}{2}F + \frac{1}{2}\bar{V}'ch\sqrt{3} \end{aligned} \qquad (2)$$

and for a type IV_a dip

$$\begin{aligned} V_r &= \bar{V}'_{ch}\ ; \\ V_y &= -\frac{1}{2}\bar{V}'ch - \frac{1}{2}F\sqrt{3}\ ; \\ V_b &= -\frac{1}{2}\bar{V}'ch + \frac{1}{2}F\sqrt{3} \end{aligned} \qquad (3)$$

The aim of the algorithms to be discussed below is to obtain the dip type according to Fig. 2, the characteristic voltage $\bar{V}'_{ch,}$ and the PN factor F, from the complex phase voltages V_r, V_y, and V_b. The latter obtained from the measured voltage waveforms. Both characteristic voltage $\bar{V}_{ch}$ and PN factor F are complex numbers. The absolute value and the argument of the characteristic voltage are referred to as "magnitude" and "phase-angle jump" of the voltage dip, respectively. The magnitude (absolute value of the characteristic voltage) is a generalization for three-phase events of the retained voltage defined in IEC 61 000-4-30.

The algorithm proposed in [8] determines the dip type from the positive-sequence and negative-sequence voltages. From (2), (3), and similar expressions for the other dip types in Fig. 3, it can be concluded that the positive-sequence voltage (with reference to -phase prefault voltage) is the same for all dip types

$$V_1 = \frac{1}{2}(F + V) \qquad (4)$$

The negative-sequence voltage is the same in magnitude but different in argument:

$$\begin{aligned} V_2 &= \frac{1}{2}(F - V) && \text{type } III_r\ ; \\ V_2 &= \frac{1}{2}a(F - V) && \text{type } III_y\ ; \\ V_2 &= \frac{1}{2}a^2(F - V) && \text{type } III_b\ ; \\ V_2 &= -\frac{1}{2}(F - V) && \text{type } IV_r\ ; \\ V_2 &= -\frac{1}{2}a(F - V)\ t && \text{type } IV_y\ ; \\ V_2 &= -\frac{1}{2}a^2(F - V) && \text{type } IV_b\ ; \end{aligned} \qquad (5)$$

where a constitutes a rotation over 120 . If we assume that F = 1, the angle between the drop in positive-sequence and negative-sequence voltage is an integer multiple of 60. The angle obtained from a measurement can be used to obtain the dip type

$$T = \frac{1}{60}\ arg\left\{\frac{V_2}{1-V_1}\right\} \qquad (6)$$

where T is rounded to the nearest integer as shown in Table1. Knowing the dip type, the other characteristics can be obtained [e.g., from the sum and difference of positive and negative-sequence voltage according to (4) and (5)].

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A Characteristic voltage

The three-phase voltage sag is defined by the characteristic voltage ($\bar{V}'_{ch}$). The characteristic voltage by a phase-to-phase fault for sag-type-III is along the affected line voltage ($\bar{V}'_{ry}$) and for other sag-types (sag-type-I, II, IV have the affected phase voltage as $\bar{V}'_{r}$). The voltage of the phase affected is the characteristic voltage as shown in the Fig. 2. With the help of sag-type indicator and sequence components, the characteristic voltage is calculated from (7),

$$\bar{V}'_{ch} = \bar{V}'_{r1} - b^{(6-T_y)}\,\bar{V}'_{r2} + a^{(6-T_y)}\bar{V}'_{r0} \qquad (7)$$

where a= $1\angle 120^0$; b= $-a^2 = 1\angle 60^0$; and $\bar{V}'_{r1}$, $\bar{V}'_{r2}$, and $\bar{V}'_{r0}$ are the complex positive-, negative-, and zero-sequence components of r-phase, respectively. These components are extracted using (3) where the moving-average technique is employed for better dynamic response. By using the above equation the phase voltages (as a function of the presage voltage and characteristic voltage) can be found for other sub types. The phase voltage of four basic types [9] are given (2), (3).

A sag flag (SF) is set by the algorithm when it detects the sag inception. The sag inception point is defined as the instant when V_{rms} of at least one phase goes below the threshold point, that is, 0.9 p.u. The injection transformer is bypassed when the SF is not set. This brings the DVR into operation only when it is required.

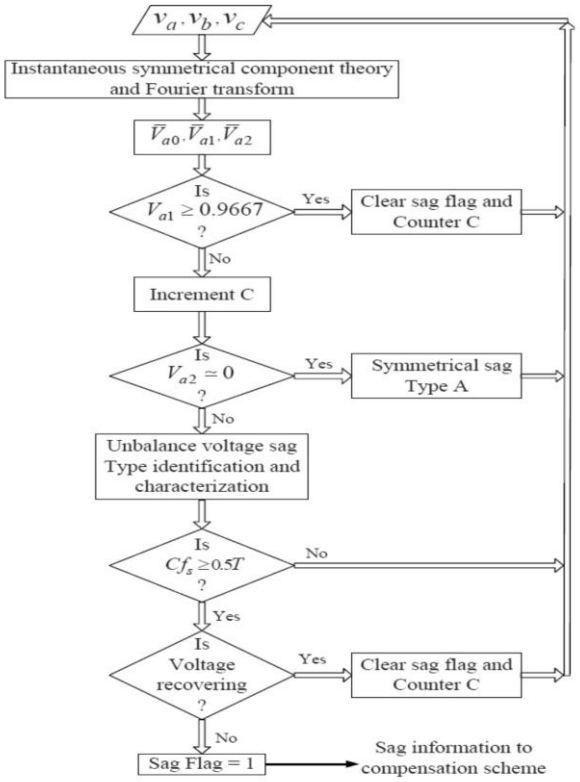

Fig 3: Algorithm flowchart

The algorithm tracks the magnitude of characteristic voltage time to time to detect whether sag is present in the system or not. SF is set when $\bar{V}'_{ch}$ goes below 0.9 p.u. $\bar{V}'_{ch}$ is the worst affected phase voltage for all sag types except for sag type-III.Since the characteristic voltage for sag type-III is along the line effected, involving the characteristic voltage and characteristic phase angle ($\emptyset$) (i.e. the angle of $\bar{V}'_{ch}$ as shown in Fig. 2.) the phase voltages are calculated using triangle properties. Using the cosine rule, the magnitudes of phase voltages are calculated as follows:

$$(V'_y)^2 = 0.25\,V^2 + 0.75\,(V'_{ch})^2 - 0.867\,VV'_{ch}\,\sin(\emptyset) \quad (8)$$
$$(V'_b)^2 = 0.25\,V^2 + 0.75\,(V'_{ch})^2 + 0.867\,VV'_{ch}\,\sin(\emptyset) \quad (9)$$

Using the sine rule, the phase jump information is derived from (10) and (11)

$$\emptyset_y = -60 + \sin^{-1}\left(\frac{\sqrt{3}\,V'_{ch}}{2V'_y}\right)\cos(\emptyset) \qquad (10)$$

$$\emptyset_b = -60 + \sin^{-1}\left(\frac{\sqrt{3}\,V'_{ch}}{2V'_b}\right)\cos(\emptyset) \qquad (11)$$

The phase voltage is used to detect the sag type. Which is found either by applying Fourier transform on the instantaneous phase voltages or by using (8) and (9) in terms of characteristic voltage.

To detect a sag, algorithm takes, at most, half-a-cycle. However, the detection time varies with sag depth, that is, deeper sag can be detected even before half-a-cycle. This delay is acceptable according to CBEMA and ITIC curves that provide voltage tolerance requirements for computing equipment [13]. The Fourier transform implemented with half-a-cycle window length causes a delay in the algorithm

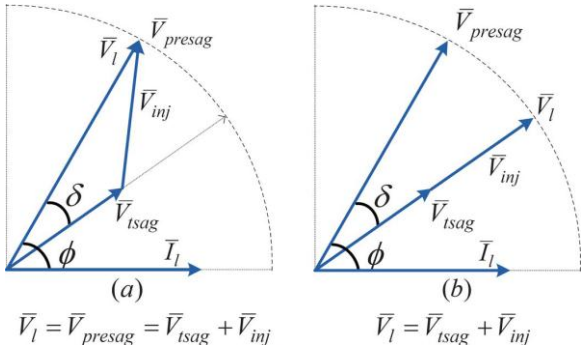

Fig 4: compensation scheme.(a) presage compensation. (b) inphase compensation

B Injected Voltage Generation

The injected voltage at the affected phase is derived from the characteristic voltage. Two compensation schemes are used to generate injected voltage, they are presage compensation and in-phase compensation. The phasor diagrams are shown in Fig. 4. The phase voltages before and during sag ($\bar{V}_{presag}$ and $\bar{V}_{tsag}$ respectively) at the PCC are shown in the phasor diagrams. The load current and terminal voltage during sag are $\bar{I}_l$ *and* $\bar{V}_l$; the load power factor angle ϕ ; and the phase jump δ. Both phase jump and voltage are compensated back to the presage condition (i.e., $\bar{V}_l = \bar{V}_{presag}$) in presage compensation. Only the magnitude of the sag (i.e., $|\bar{V}_l| = |\bar{V}_{presag}|$) is compensated in inphase compensation [12].

For sag types except type-III, the characteristic voltage is the phase voltage and, therefore, the injected voltage is

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Vol. 3, Issue 7, July 2015

calculated for presag compensation as follows:

$$\bar{V}_{inj} = \bar{V}_{presag} - \bar{V}_{ch}^{'} \quad (12)$$

For the inphase compensation, the injected voltage is inphase with the characteristic voltage, and so only the magnitude is derived by

$$|\bar{V}_{inj}| = |\bar{V}_{presag}| - |\bar{V}_{ch}^{'}| \quad (13)$$

For sag type-III, since characteristic voltage is along the line voltage, the injected voltage is calculated by using

$$\bar{V}_{inj} = \frac{\sqrt{3}}{2}(\bar{V}_{ch} - \bar{V}_{ch}^{'}) \quad (14)$$

where $\bar{V}_{ch}$ is the characteristic voltage before sag. The injected voltage for the inphase compensation is derived similarly.

The sag supporter generates the approximate voltage with respect to the reference voltage to be injected. Here, an interphase ac–ac converter topology [11] is used for the study, since it accounts for phase-jump correction also. The switching scheme for the topology based on the characterization is discussed in the next section.

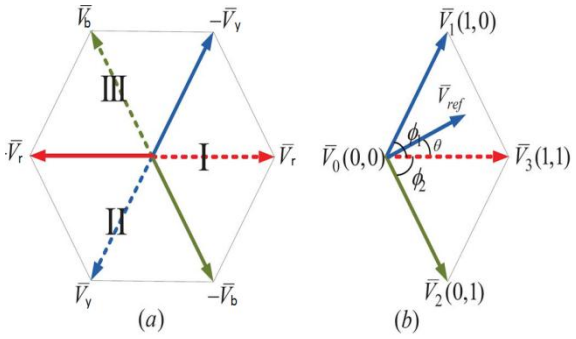


Fig 5: Switching Sequence (a) sectors of operation (b) sector I

III. GENERATION OF DUTY CYCLES

The energy from the other phases is taken and calculated the duty cycles required to compensate the voltage dip in the affected phase. Fig. 5(a) represents three sectors I, II, and III, each comprised of two inverted phase voltages, and they represent phase-r, y and b sag supporters, respectively.

The phase-r sag supporter (sector I) with injected voltage and active vectors is shown in Fig. 5(b). The active vector $\bar{V}_1(1,0)$ can be realized by switching OFF the phase-b chopper and ON the phase-y chopper; while vector $\bar{V}_2$ (0,1) can be realized by switching ON the phase-b chopper and OFF the phase-y chopper. If both the choppers are ON, the resulting vector lies over the active vector $\bar{V}_3$ (1,1). The fourth vector, zero vector $\bar{V}_0$ (0,0) , is placed at the origin and is obtained by withdrawing the switching pulses from both choppers.

Under normal condition the active vectors $\bar{V}_1$, $\bar{V}_2$, and $\bar{V}_3$ are 60^o apart as in Fig. 5(b). These angles may alter due to phase jump in the phase voltages. For sag type B, only one phase is affected. Therefore, phase angles $\emptyset_1$and $\emptyset_2$ of the active vectors with respect to $\bar{V}_3$ remain as 60^o each. Since the phase voltages are affected for most of the other sag types, the angles $\emptyset_1$and $\emptyset_2$ are not 60^o, rather it is $60^o \pm$ phase jump. For example, sag type IV_r has angles $\emptyset_1$and $\emptyset_2$, as (60^o + S_b), and (60^o – S_c), respectively, where S_b and S_c are the phase jumps associated with the phases-b and c, respectively.

The sag supporter to be activated for compensation is identified from the sag-type indicator (T_y). Over the sector, the injected voltage ($\bar{V}_{inj}$) is searched, and it is generated by weighted average, over a cycle, of the other two phase voltages as

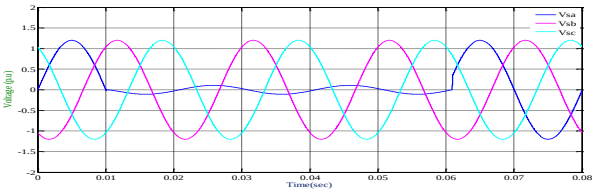
$$d_1 \bar{V}_1 + d_2 \bar{V}_2 = \bar{V}_{ref} \quad (15)$$

where d_1 and d_2 are duty cycles of the choppers corresponding to the active vectors $\bar{V}_1$ and $\bar{V}_2$. The duty cycles are calculated as in (16) and (17), by resolving (15) in rectangular coordinates

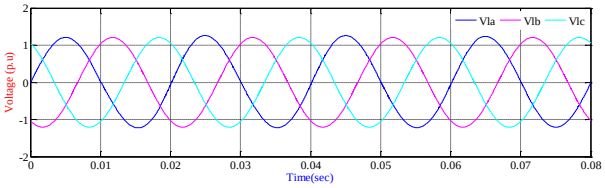
$$d_1 = \frac{|\bar{V}_{ref}|}{|\bar{V}_1|} \frac{\sin(\emptyset_2+\theta)}{\sin(\emptyset_1+\emptyset_2)} \quad (16)$$

TABLE II: Parameters (in p.u.) Estimated from simulatin studies

	II_r : 0.1∠-60^o	III_y :0.6∠-30^o	I : 0.5∠-60^o
$\bar{V}_r$	0.1∠-60^o	0.51∠1.91^o	0.5∠-60^o
$\bar{V}_y$	1∠-120^o	1∠-120^o	0.5∠180^o
$\bar{V}_b$	1∠120^o	0.88∠90.64^o	0.5∠60^o
V_{r1}	0.68	0.77	0.5
V_{r2}	0.32	0.283	0
V_{r0}	0.32	0	0
T_y	3	2	7
$\bar{V}_{ch}$	0.1∠-60^o	0.6∠-30^o	0.5∠-60^o
$\bar{V}_{inj}$	0.95∠5.2^o	phase-b: 0.49∠60^o phase-r: 0.49∠1.98^o	For all phases: 0.5∠-60^o
d_1	1	phase-b: 0.92 phase-r: 0.92	1
d_2	0.9	phase-b: 0 phase-r:0.96	1



(a) Phase voltage at the PCC with sag



(b) Load voltage

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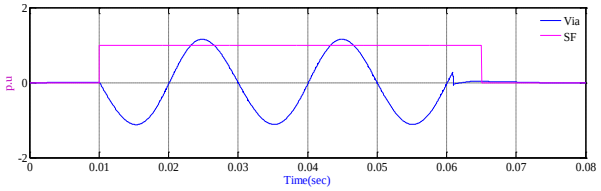
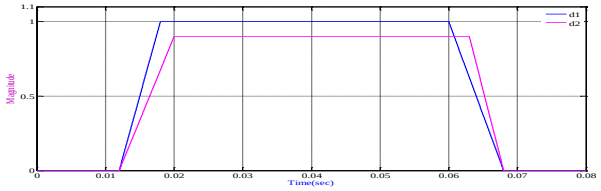


(c) Injected voltages with the sag flag (SF)



(d) Duty cycle of the choppers in phase- sag supporter

Fig. 6: Compensation of a sag type II

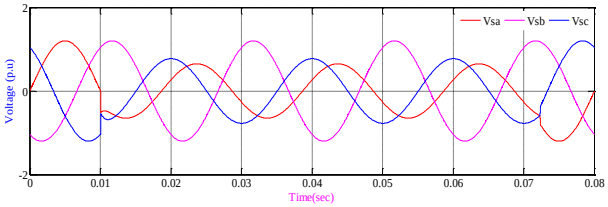
$$d_2 = \frac{|\bar{V}_{ref}|}{|\bar{V}_2|} \frac{\sin(\emptyset_1 - \theta)}{\sin(\emptyset_1 + \emptyset_2)} \qquad (17)$$

where θ is phase angle of the injected voltage, and $\emptyset_1$and $\emptyset_2$ are phase angles of the active vectors with respect to the active vector $\bar{V}_3$.

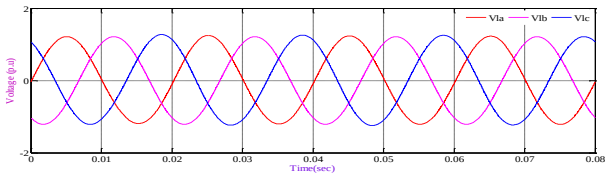
Since, a buck ac–ac chopper is employed to realize the injected voltage, a limit is imposed on d_1 and d_2 as given by

$$0 \leq d_1 \leq 1 \; and \; 0 \leq d_2 \leq 1 \qquad (18)$$

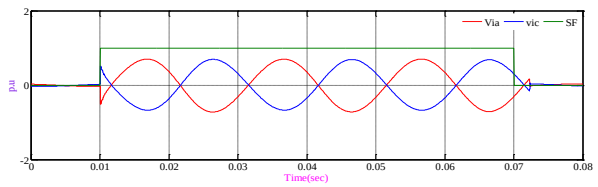
The calculated duty cycles d_1 and d_2 are given to series switches of the choppers across the phase voltages corresponding to the active vectors $\bar{V}_1$ and $\bar{V}_2$, that is, phase-b and c voltages, for a phase-a sag supporter. The complement of the switching signals d_1 and d_2 are $\bar{d}_1$and $\bar{d}_2$, respectively, and are given to the corresponding load current.



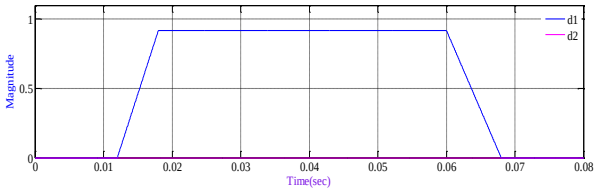
(a) Phase voltage at the PCC with sag



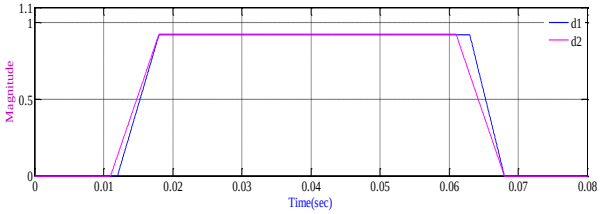
(b) Load voltage at the PCC



(c) Injected voltages with the SF



(d) The duty cycle of voltages in phase-c Sag supporter



(e) The duty cycle of choppers in phase-a sag supporter

Fig.7: Compensation of a sag type III_y

IV. SIMULATION STUDIES

The sags are generated in MATLAB with the three phase fault using the relations between the distance from PCC, phase angle jump and the magnitude. The three phase model of the system is shown in Fig. 1. and the results are shown in Figs. 6-8. The duty cycles required for the circuit are also shown in

TABLE III: System and ac chopper parameters for experimental studies

Parameters	Values	
Rated voltage and frequency	50 V, 50 Hz	
Load	50 Ω	
Injection transformer	1 : 1, 140 V, 700 VA	
AC chopper	Switching frequency f_s	5 kHz
	Input capacitance C_s	50 µF
	Filter inductance L_f	0.25 mH
	Filter capacitance C_f	180 µF

the same. For theaffected phase for three sag types are estimated by the magnitude of the symmetrical components ($\bar{V}_{a1}, \bar{V}_{a2}, and \; \bar{V}_{a3}$), characteristic voltage $(\overline{V_{ch}})$, sag-type indicator (T_y) and the injected voltage (V_{inj}) and their corresponding per-unit values are listed in Table II.

The presence of the zero component (V_{r0}) and the calculated T_y value suggests that it is III_r type sag for single-phase sag as simulated in Fig. 6(a). The phase-r sag supporter is activated when sag is occured in phase-r. Fig. 6(b) and (c) are compensated and injected voltage (v_{ir}), which is accompanied when a SF is set. The DVR is made to operate when the SF is high. To set the SF, the algorithm takes 1/8th of a power cycle to detect the sag. Fig 6(d) shows the duty cycles d_1 and d_2 of the ac-choppers across phase-y and phase-b, respectively. The sag is compensated with in a period of half-a-cycle. A III_y type sag with a characteristic voltage of $0.6\angle\text{-}\,30^o$ is

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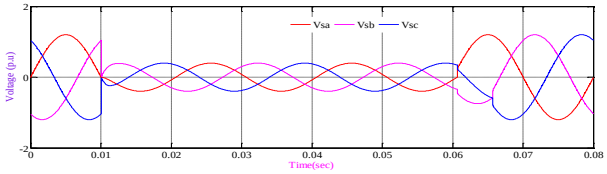
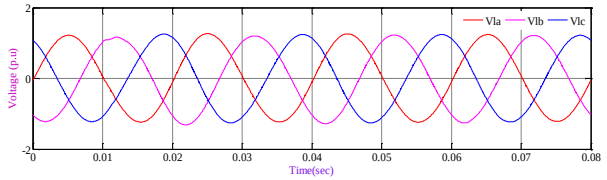
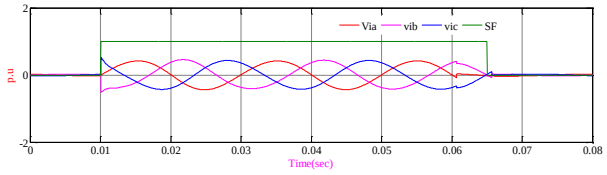
considered. Both phase-b and -r sag supporters are activated since phases-b and phase-r are affected from (14) both the characteristic voltage and the corresponding injected voltages are calculated. Fig. 7(b) shows compensated voltages at the PCC (i.e, prior to pre-sag condition of phase-b), eliminating the -29^{o} phase jump. The injected voltages(V_{ib} and V_{ir}) with SF, which is set in 1/4th of a power cycle for the sag type III_r is shown in Fig. 7(c). Fig. 7(d) and (e) shows the duty cycles of the choppers in sag supporters-b and sag supporter-r, respectively.Fig. 8(a) shows symmetrical sag exceeding the pre-sag compensation limit, with 50% sag magnitude and -60^{o} phase jump. Here, the algorithm operates in an inphase compensation scheme, and the corresponding injected voltages are calculated. Since it is a symmetrical sag all sag supporters in the three phases are activated. Fig. 8(b)–(d) shows the compensated voltages at the PCC, injected voltages, and the duty cycles of the choppers,



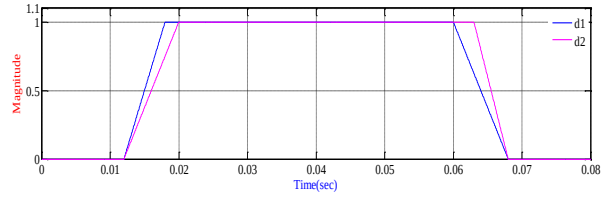
(a) Phase voltage at the PCC with sag



(b) Load voltage at the PCC



(c) Injected voltages with the SF



(d) The duty cycle of choppers in all sag supporters.

Fig. 8: Compensation of a sag type I

respectively. The transgression of limits as given in (18) is checked by the algorithm to switch between the compensation schemes. The compensation can be for a longer duration, but sag duration of 2.5 cycles is compensated in the simulations.

When the characteristic voltage at the PCC is within the compensation capability of the topology [13], the duration of compensation by the topology is limited only by the power available at the PCC

V. CONCLUSION

In this thesis, a control scheme based on the characterization of voltage sag is proposed. It is tested on inter-phase ac–ac converter topology and it is found that the scheme besides compensation gives insight on the limits on compensation imposed by various sag types. Therefore, it aids in the flexible compensation by switching between pre-sag and in-phase compensation. The scheme provides 100% compensation for type sag, and for all other types, compensation up to 50% sag magnitude with phase jumps ranging from 60^{o} to 60^{o} for interphase ac-ac topology. The algorithm takes; at most, half a cycle to compensate and it works in the presence of harmonics and unbalance, since the Fourier transform is employed to extract the fundamental component from 60^{0} to 60^{0} for inter phase ac–ac topology. The algorithm takes; at most, half a cycle.

REFERENCES

[1]. P. B. Steciuk and J. R. Redmon, "*Voltage sag analysis peaks customer service*," IEEE Comput. Appl. Power, vol. 9, pp. 48–51, Oct. 1996.

[2]. C. Becker et al., "*Proposed Chapter 9 for predicting voltage sags (dips) in revision to IEEE Std. 493, the Gold Book*," IEEE Trans. Ind. Applicat., vol. 30, pp. 805–821, May/June 1994.

[3]. M. F. McGranaghan, D. R. Mueller, and M. J. Samotyj, "*Voltage sags in industrial systems*," IEEE Trans. Ind. Applicat., vol. 29, pp. 397–403, Mar./Apr. 1993.

[4]. EPRI, "*Distribution system power quality assessment: Phase II—Voltage sag and interruption analysis*," Electr. Power Res. Inst. (EPRI), Palo Alto, CA, Tech. Rep. 1001678, 2003.

[5]. A. Prasai and D. M. Divan, "*Zero-energy sag correctors-optimizing dynamic voltage restorers for industrial applications*," IEEE Trans. Ind. Appl., vol. 44, no. 6, pp. 1777–1784, Nov./Dec. 2008.

[6]. Y. Tang, S. Xie, and C. Zhang, "*Z-source ac–ac converters solving commutation problem*," IEEE Trans. Power Electron., vol. 22, no. 6, pp. 2146–2154, Nov. 2007.

[7]. M. Kazerani, "*A direct AC/AC converter based on current-source converter modules*," IEEE Trans. Power Electron., vol. 18, no. 5, pp. 1168–1175, Sep. 2003.

[8]. L. D. Zhang and M. H. J. Bollen, "*Characteristic of voltage dips (sags) inpower systems*," IEEE Trans. Power Delivery, vol. 15, pp. 827–832, Apr. 2000.

[9]. M. H. J. Bollen, Understanding Power Quality Problems. Piscataway, NJ, USA: IEEE, 2000.

[10]. IEEE Recommended Practice for Emergency and Standby Power Systems for Industrial and Commercial Applications, IEEE Standard 446- 1995, Jul. 3, 1996

[11]. S. Subramanian and M. K. Mishra, "*Interphase AC-AC topology for voltage sag supporter*," IEEE Trans. Power Electron., vol. 25, no. 2 pp. 514–518, Feb. 2010

[12]. D.M. Vilathgamuwa, A. A. D. R. Perera, and S. S. Choi, "*Voltage sag compensation with energy optimized dynamic voltage restorer*," IEEE Trans. Power Del., vol. 18, no. 3, pp. 928–936, Jul. 2003.

[13]. J. Suma and M. K. Mishra, "*Instantaneous symmetrical component theory based algorithm for characterization of three phase distorted and unbalanced voltage sags*," in Proc. IEEE Int. Conf. Ind. Technol., Feb. 2013, pp. 845-850

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