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Comparative study on a low drop-out voltage regulator

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Abstract: Today's LDO (low drop-out voltage regulator) must meet the requirements of various future demands of the portable electronics. To get a new approach towards a design of low drop-out voltage regulator that provides a modern system on chip (SoC) solution and fulfils the present commercial requirements as well as the projected demands of the future, it becomes necessary to study the literature work. The various performance matrices such as minimization of drop-out voltage, low power, low operating voltages, low quiescent currents, fast transient response, high PSR and high packing density have a vital importance in designing of LDO regulator. Furthermore, capacitor less LDO architecture, overcomes the typical load transient and ac stability issues. The designing can be possible with Digital implementation and programmability can be added to become suitable for more applications. Considering the advancement of future technology, regulator can be proposed with the selection of lower order of nm technology. This paper presents the comparative study of literature work that contributes to the research of LDO using CMOS technology and provides different architectures and techniques to make LDO better.

Keywords*:* Low Drop-Out Voltage Regulator, Low Power, Low quiescent current, PSR.

I. INTRODUCTION

The demand for low-voltage, low drop-out (LDO) regulators are increasing because of the increasing demand for portable electronics. The low drop-out nature of the regulator makes it appropriate for use in many applications as automotive, portable, industrial, and medical applications. The automotive industry requires low drop-out (LDO) regulators to power up digital circuits, especially during cold-crank conditions where the battery voltage can be below 6 V. The increasing demand, however, is especially essential in mobile battery operated devices, such as cellular phones, pagers, camera recorders, and laptops. Low quiescent current flow is important in portable products where the total current drain determines battery life.(1) Each performance metric such as drop-out voltage, power, operating voltages, quiescent currents, transient response, PSR(power supply rejection),packing density and regulation issues has its own consequence to make regulator better. Also it is very much essential to reduce the number of battery cells, so that minimization of cost and size is possible.

For efficient power management in power management systems, an important building block is the low drop-out (LDO) linear regulator which often follows a DC-DC switching converter. It is used to regulate the supplies ripples to provide a clean voltage source for the noise-sensitive analog/RF blocks. Designing a stable LDO for a wide range of load conditions, while achieving high power-supply rejection (PSR), low drop-out voltage, and low quiescent current, is the main target using CMOS technologies. Recently, there has been an increasing demand to integrate the whole power management system into a single system-on-chip (SoC) solution.

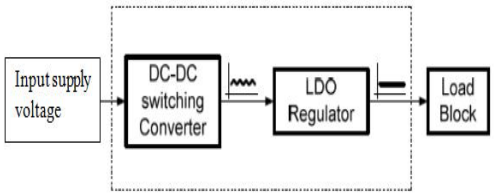

Fig. 1: Block diagram of typical power management system

Hence the proposed paper focuses the review of certain published literature that contributes to research of low drop-out (LDO) voltage regulator by identifying patterns and trends in the literature. This study will help us to find new approaches towards power management and fulfil the need of LDO regulators in various sectors. It is observed that many researchers have designed different models of low drop-out regulator by applying different methodologies and each of these models contribute to further research

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II. SYSTEM ARCHITECTURE OF CONVENTIONAL LDO REGULATOR

Low-drop out regulators is one of the most conventional applications of operational amplifiers. Figure 2 shows the basic topology. A voltage reference is used with the op-amp to generate a regulated voltage, Vreg (Vout). If the voltage reference is stable with temperature, the fact that the Vreg is a function of a ratio of resistors (so process or temperature changes in the resistance value don't affect the ratio) and the variation in the op-amp's open loop gain is desensitized using feedback makes the regulated voltage stable with process and temperature changes.

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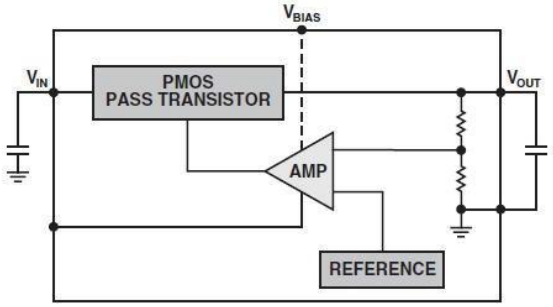

Fig. 2: Conventional LDO

III. KEY PARAMETERS OF LDO REGULATOR

Some of the key parameter of low drop-out regulator is discussed where-

Ii, Vi–Input current and input voltage

Io, Vo –Output current and output voltage

A. Dropout Voltage

Dropout voltage is the input-to-output differential voltage at which the circuit ceases to regulate against further reductions in input voltage; this point occurs when the input voltage approaches the output voltage.

B. Quiescent Current or Ground Current

Quiescent current, or ground current, is the difference between input and output currents. Minimum quiescent current is necessary for maximum current efficiency. Quiescent current is defined by-

$$I_q = Ii - Io$$

Quiescent current consists of bias current (such as band-gap reference, sampling resistor and error amplifier) and drive current of the series pass element, which do not contribute to output power. The value of quiescent current is mostly determined by the series pass element, topologies, ambient temperature, etc.

C. Efficiency

The efficiency of a LDO regulator is limited by the quiescent current and input/output voltage as follows:

$$\text{Efficiency} = [I_o V_o / (I_o + Iq)\, Vi] \times 100$$

To have a high efficiency LDO regulator, drop out voltage and quiescent current must be minimized. In addition, the voltage difference between input and of LDO regulators accounts for the efficiency. The input/output voltage difference is an intrinsic factor in determining the efficiency regardless of the load condition.

D. Load Regulation

Load regulation is a measure of the circuit's ability to maintain the specified output voltage under varying load conditions. Load regulation is defined as-

$$\text{Load Regulation} = \Delta Vo / \Delta Io$$

E. Line Regulation

Line regulation is a measure of the circuit's ability to maintain the specified output voltage with varying input voltage. Line regulation is defined as-

$$\text{Line regulation} = \Delta Vo / \Delta Vi$$

F. Transient Response

The transient response is an important specification, which is the maximum allowable output voltage variation for a load current step change. The transient response is a function of the output capacitor value (Co), the equivalent series resistance (ESR) of the output capacitor, the buy pass capacitor (Cb), and the maximum load current.

IV. DIFFERENT CIRCUIT TOPOLOGIES USED TO DESIGN LDO'S.

In the year 1998,Gabriel A. Rincon-Mora, Phillip E. Allen in their paper named " A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator'' discussed some techniques that enable the practical realizations of low quiescent current LDO's at low voltages and in existing technologies. The proposed circuit exploits the frequency response dependence on load-current to minimize quiescent current flow. Moreover, the output current capabilities of MOS power transistors are enhanced and drop-out voltages are decreased for a given device size. A drop-out voltage also need to be minimized to maximize dynamic range within a given power supply voltage. In this paper, two significant contributions namely current efficient buffer and current boosted pass device, make the low-voltage design viable for battery powered circuits. Both these techniques take advantage of the availability of a sense element that provides a linearly load dependent current. This is intrinsic for low quiescent current flow during low load-current conditions. The resulting circuit takes maximum advantage of the transistors utilized to yield low component count and low overall ground current. Furthermore, the current boosting technique can be readily implemented in applications requiring low switch-on resistors, i.e., dc-dc converters.

In the year 2007, Robert J. Milliken, Jose Silva-Martínez, and Edgar Sánchez-Sinencio, in their paper named, "Full on-chip CMOS low-dropout voltage regulator" proposed a solution to the present bulky external capacitor low-dropout (LDO) voltage regulators with an external capacitor less LDO architecture. The large external capacitor used in typical LDOs is removed allowing for greater power system integration for system-on-chip (SoC) applications. The compensation scheme is presented that provides both a fast transient response and full range alternating current (ac) stability from 0 to 50-mA load current even if the output load is as high as 100 pF. This paper poses to remove the large external capacitor, while guaranteeing stability under all operating conditions using 0.35µm CMOS technology. Removing the large off-chip output capacitor also reduces the board real estate and the overall cost of the design and makes it suitable for SoC designs. There are the following two major design considerations 1) small over/under shoots during transients and 2) the regulator's stability. To solve these issues, a compensating left-hand plane (LHP) zero is introduced in the proposed design. Not only does the proposed regulator consume low power, but it provides a low dropout voltage and fast settling time. SoC designs would benefit from the reduced board real estate, pin count, and cost achievable with the proposed off-chip capacitor less full CMOS LDO regulator.

In year 2010, Ka Nang Leung, Yuan Yen Mai, and Philip K. T. Mok in their paper, "A Chip-Area Efficient

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Voltage Regulator for VLSI Systems'' presented an error amplifier structure to improve load regulation of low-voltage low-dropout regulators using AMS 0.35µm CMOS technology. Compactness is a major concern of this work. The key requirements of the error amplifier are wide output swing to maximize the gate to source voltage of the power transistor and simple frequency response to ease frequency compensation of the LDO. A current-mirror amplifier proves good choice for this purpose .A single-sided gain-retained method to extend the high gain region of the error amplifier and retain the voltage gain at large load current is proposed in this paper. Experimental results show that the required power transistor size is reduced by 25% to achieve similar performance in load regulation. Moreover, extra power consumption and increase of silicon area are not significant. The design of the output stage of the error amplifier has a substantial impact on the required size of the power transistor for the improvement of load regulation, especially when the supply voltage of the VLSI systems is low. The idea can be extended to the analog-driver design for maximizing the output capability.

In March 2010, Mohamed El-Nozahi, Ahmed Amer, Joselyn Torres, Kamran Entesari and Edgar Sánchez-Sinencio, in their paper named " High PSR Low Drop-Out Regulator With Feed-Forward Ripple Cancellation Technique'' presented a low drop-out (LDO) regulator with a feed-forward ripple cancellation (FFRC) technique that achieves a high power-supply rejection (PSR) over a wide frequency range. Kelvin connection is also used to increase the gain–bandwidth of the LDO that allows for faster transient performance. The LDO was implemented in 0.13µm CMOS technology and achieves a PSR better than 56 dB. This is the first LDO that achieves such a high PSR up to 10 MHz In addition; it enables the design for high supply currents and low quiescent current consumption. The proposed topology provided a robust design when the process, temperature and bonding inductance variations are considered. The FFRC can be extended to any existing LDO architecture to yield a high PSR for a wide range of frequencies. In addition, it was shown that Kelvin connection at the output helps to increase the GBW of the LDO without affecting the stability at heavy loads.

In year 2010,Amit P. Patel and Gabriel A. Rincon-Mora in their paper, "High Power-Supply-Rejection (PSR) Current-Mode Low-Dropout (LDO) Regulator," presented a 5-mA 1.5-μm bipolar current-mode LDO regulator that, with a higher bandwidth current loop, suppresses higher frequency noise by 49 dB (i.e., power supply rejection) up to 10 MHz with only 68 nF at the output, which is 20 dB better than its voltage-mode counterpart. Modern system-on-a-chip (SoC) solutions suffer from limited on-chip capacitance, which means that the switching events of functionally dense ICs induce considerable noise in the supplies. This ripple worsens the accuracy of sensitive analog electronics. Without dropping a substantial voltage, point-of-load (PoL) low-dropout (LDO) regulators reduce (filter) this noise but only as much as their loop gains and bandwidths allow. The prototyped 1.5-μm bipolar LDO achieved this performance by increasing the impedance to the supply with a current-sampling feedback loop. The loop essentially samples the output current with a mirroring sense transistor and mixes it into the main (voltage) loop through a frequency shaping (*RC*-degenerated) differential pair. Further suppressing the supply ripple (by 6×) in this way prevents switching converter noise from rendering sensitive analog functions ineffectual.

Many techniques have been proposed for designing LDO regulators with a programmable output voltage [9]-[11]. In January 2012,Jia-Hui Wang, Chien-Hung Tsai and Sheng-Wen Lai in their paper, "A Low-Dropout regulator with tail current control for DPWM clock correction'' presented a low-dropout (LDO) regulator with tail current control (TCC) that consists of a dual differential pair, a 5-bit current digital-to-analog converter, and a current summation circuit using 0.18µm CMOS technology. The TCC adjusts the tail current ratio of the dual differential pair of the LDO regulator to achieve a programmable output voltage using 5-bit digital signals. The power supply rejection over a wide frequency range is improved with addition of supply-ripple isolation mechanism. The proposed LDO regulator with TCC provides a supply voltage to a DPWM (digital pulse width modulation) to achieve a 32-level oscillator frequency. The DPWM is a voltage-controlled oscillator (VCO), and low-dropout (LDO) regulators which are used for the supply voltage of VCOs because they have advantage of reduced supply noise, allowing a steady oscillator frequency in a SoC chip. In addition, the PSR performance improved by about 20 dB over a wide frequency range due to an isolation mechanism. Therefore, the proposed LDO regulator is suitable for correcting the oscillator frequency of DPWMs. On the other hand, the TCC technology needs accurately to adjust tail current to achieve the 32-level output voltage of the LDO regulator; therefore, the transistors size of the TCC circuit is so large that the proposed LDO occupies more area than previous LDO regulators. This brief proposes an LDO regulator with a programmable output voltage, which adjusts the clock of a DPWM and provides it with a clean supply voltage.

In the year 2013, Yen-Chia Chu and Le-Ren Chang-Chien introduced a digitally controlled low-dropout voltage regulator (LDO) in their paper entitled, " Digitally Controlled Low-Dropout Regulator with Fast-Transient and Auto tuning Algorithms'' that can perform fast-transient and auto tuned voltage. As there are still several arguments regarding the digital implementation on the LDOs, advantages and disadvantages of the digital control are first discussed in this paper to illustrate its opportunity in the LDO applications. This paper brings new concept to digitize LDO's using 0.18µm CMOS technology. Following that, the architecture and configuration of the digital scheme are demonstrated. Under the new design concept, several drawbacks of the digital implementation would be minor. This paper presents a D-LDO with various features that did not appear in the counterpart of the analog one. Different from the analog approach, a digital compensation scheme is demonstrated to solve the

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ESR zero problem when a small output capacitor is employed. It is noted that the proposed digital scheme allows more types of compensation to be implemented in the design flow. In addition, to ensure the transient performance, several operating uncertainties should be taken care of by an autonomous manner. Therefore, two auto tuning methods to handle the uncertainty problem were discussed. The first auto tuning method is to adjust the charge-balance current by controlling the driving voltage of the power MOSFET during the transient time. The second auto tuning function is to automatically assign proper initial values for the compensator for avoiding ringing at output voltage. Also the D-LDO is robust when it is operating under the conditions of low supply voltage and wide supply voltage variation. One of the drawbacks in the digital control is the power consumption issue as power consumption of the digital controller is higher than that of the analog controller.

In 2014, Chung-Hsun Huang, Ying-Ting Ma and Wei-Chen Liao in their paper entitled "Design of a Low-Voltage Low-Dropout Regulator," presented a low-voltage low-dropout (LDO) regulator that converts an input of 1 V to an output of 0.85–0.5 V, with 90-nm CMOS technology. A simple symmetric operational trans-conductance amplifier is used as the error amplifier (EA), with a current splitting technique was adopted to boost the gain. This also enhances the closed-loop bandwidth of the LDO regulator. In the rail-to-rail output stage of the EA, a power noise cancellation mechanism is formed, minimizing the size of the power MOS transistor. Furthermore, a fast responding transient accelerator is designed through the reuse of parts of the EA. These advantages allow the proposed LDO regulator to operate over a wide range of operating conditions while achieving 99.94% current efficiency, a 28-mV output variation for a 0–100 mA load transient, and a power supply rejection of roughly 50 dB over 0–100 kHz. This paper proposed an LDO regulator using a simple OTA-type EA plus an adaptive transient accelerator, which can achieve operation below 1 V, fast transient response, low *IQ*, and high PSR under a wide range of operating conditions.

V. RESULT AND DISCUSSION

From review of published literature, it is observed that many researchers have designed different models of low drop-out regulator by applying different methodologies. Also many phenomena have been undertaken to enhance the transient response of the LDO regulators and to combat with stability issues and power management problems. Efficiency obtained with mentioned proposed LDO architectures is about 98%.The LDO architectures in [1] and [5] provide current efficiency of 99.94% and 99.95% respectively whereas [4] &[5] gives PSR of about 57dB at $100KH_z$.It is seen that nm technology proves better in achieving required performance specifications.

The large external capacitor used in typical LDOs can be removed allowing for greater power system integration for system-on-chip (SoC) applications that require a sound compensation scheme for both the transient response and the alternating current (ac) stability. Presently, in some applications, the external capacitor used is quite large (10 μF), but capacitor less architectures [4] have been proposed and form a significant part of current CMOS LDO design literature. The proposed circuit will be able to exploit the frequency response dependence on load-current to minimize quiescent current flow so that current efficient buffer and current boosted pass device can be made the low-voltage design viable for battery powered circuits. The advanced power management unit (PMU) concept inside the SoC scheme inspires the digital control potential for the design of a novel D-LDO regulator that is capable to perform fast transient and performing the DVS function can be used to propose LDO with digital implementation responsible to increase area of applications [2]. An error amplifier structure to improve load regulation of low-voltage, low-dropout regulators can be employed. The TCC adjusts the tail current ratio of the dual differential pair of the LDO regulator to achieve a programmable output voltage using 5-bit digital signals.
In [9]–[11], external control signals open or short the switch transistors to change the feedback resistor divider ratio to achieve a programmable output voltage. However, extra resistors and switch transistors are needed for additional output voltages. The FFRC technique can be extended to any existing LDO architecture to yield a high PSR for a wide range of frequencies [4]. A LDO regulator using a simple OTA-type EA plus an adaptive transient accelerator achieve fast transient response, low *IQ*, and high PSR under a wide range of operating conditions. If in the rail-to-rail output stage of the EA, a power noise cancellation mechanism is formed, the size of the power MOS transistor can be minimized [1].

VI. CONCLUSION

By comparing circuit topologies for designing LDO regulator, it is seen that in general, all LDO specifications constrain each other. It is difficult to improve all of them simultaneously. As the various performance matrices such as minimization of drop-out voltage, low power, low operating voltages, low quiescent currents, fast transient response, high PSR and high packing density have a vital importance in designing of LDO regulator, future LDO should beware of all these matrices. The capacitor less LDO architecture sounds good in overcoming the typical load transient and ac stability issues. Furthermore, the designing can be possible with digital implementation and programmability can be added to become suitable for more applications. Also future nm technology offers more advantages in achieving most of the performance specifications so considering the advancement of future technology, regulator can be proposed with the selection of lower order of nm technology to fulfil targeted demands.

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