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Design of low power Flip-Flop with signal feed through scheme for Counter Design Applications: A Review

Haritha Vijayan[1], Praveen J[2], Raghavendra Rao A[3]

M.Tech Student, Dept. of ECE, Alva's Institute of Engg & Technology, Mijar, Moodbidri, Karnataka, India[1]

Sr. Associate professor, Dept. of ECE, Alva's Institute of Engg &Tech, Mijar, Moodbidri, Karnataka, India[2,3]

Abstract*:* A low-power flip-flop (FF) design featuring an explicit type pulse-triggered structure and a modified true single phase clock latch based on a signal feed-through scheme is presented. The proposed design successfully solves the long discharging path problem in conventional explicit type pulse-triggered FF (P-FF) designs and achieves better speed and power performance. Based on post-layout simulation results using cadence virtuoso CMOS 180-nm technology, the proposed design outperforms the conventional P-FF design. The proposed design features the best power-delay-product performance in both implicit and explicit type flip flops under comparison. Counters can be designed using such flip flop. As a result power consumption is reduced compared to conventional methods. In this paper, a low power explicit pulse triggered flip flop is discussed as a proper choice of low power applications and comparison with other flip flop architectures.

Keywords*:* Flip-flop (FF), low power, pulse-triggered, signal feed through scheme.

I . INTRODUCTION

The increasing significance of portable systems and the need to limit power consumption (and hence, heat dissipation) in very-high density Very Large Scale Integration (VLSI) chips have led to rapid and innovative developments in low-power design during the recent years. Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in first out. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power. FFs thus contribute a significant portion of the chip area and power consumption to the overall system design .

Pulse-triggered FF (P-FF), because of its single-latch structure, is more popular than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. A P-FF consists of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are sufficiently narrow, the latch acts like an edge-triggered FF. Since only one latch, as opposed to two in the conventional master–slave configuration, is needed, a P-FF is simpler in circuit complexity. This leads to a higher toggle rate for high-speed operations. P-FFs also allow time borrowing across clock cycle boundaries and characteristic a zero or even negative setup time.

Depending on the method of pulse generation, P-FF designs can be classified as implicit and explicit .In an implicit-type P-FF, the pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated. In an explicit-type P-FF, the designs of pulse generator and latch are separate.

II. LITERATURE SURVEY

Mr.Hamid Mahmoodi et.al proposed a paper[10], A low power clocking schemes for low-power design. The proposed flip-flops operate with a single-phase sinusoidal clock, which can be generated with high efficiency. In the TSMC 0.25- m CMOS technology. Implementation of 1024 proposed energy recovery clocked flip-flops through an H-tree clock network driven by a resonant clock-generator to generate a sinusoidal clock. Simulation results show a power reduction of 90% on the clock-tree and total power savings of up to 83% as compared to the same implementation using the conventional square-wave clocking scheme and flip-flops. Using a sinusoidal clock signal for energy recovery prevents application of existing clock gating solutions. In this paper, we also propose clock gating solutions for energy recovery clocking. Applying clock gating to the energy recovery clocked flip-flops reduces their power by more than 1000x in the idle mode with negligible power and delay overhead in the active mode. Finally, a test chip containing two pipelined multipliers one designed with conventional square wave clocked flip-flops and the other one with the proposed energy recovery clocked flip-flops is fabricated and measured. Based on measurement results, the energy recovery clocking scheme and flip-flops shows a power reduction of 71% on the clock-tree and 39% on flip-flops, resulting in an overall power savings of 25% for the multiplier chip.

In this paper, energy recovery techniques are applied to the clock network since the clock signal is typically the most capacitive signal in a chip. The proposed energy recovery clocking scheme recycles the energy from this capacitance in each cycle of the clock. For an efficient clock generation, we use a sinusoidal clock signal. The rest of the system is implemented using standard circuit

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styles with a constant supply voltage. However, for this technique to work effectively there is a need for energy recovery clocked flip-flops that can efficiently operate with a sinusoidal clock.

In this paper, clock gating solutions for the energy recover clock is proposed. We modify the design of the existing energy recovery clocked flip-flops to incorporate a power saving feature that eliminates any energy loss on the internal clock and other nodes of the flip-flops. Applying the proposed clock gating technique to the flip-flops reduces their power by a substantial amount (1000x) during the sleep mode. Moreover, the added feature has negligible power and delay overhead when flip-flops are in the active mode. The results demonstrate the feasibility and effectiveness of the energy recovery clocking scheme in reducing total power consumption.

Ms. Tania Gupta et.al in [6]. Has presented an explicit pulsed double edge triggered sense amplifier flip-flop for the low power and low delay in the paper. The redundant transitions are eliminated by using the conditional technique named conditional discharge technique. By using the fast improved version of the nickolic latch along with the sense amplifier approach for the latching and the sensing stage the delay factor of the circuit is improved. Simulation using TSPICE and a 0.18µm CMOS technology shows that the proposed design has low power dissipation and small delay as compared to the existing design which use a conditional precharge technique in the design for removing the redundant transitions. Comparing with the previous work of the dual edge triggered flip-flops, the proposed one saved power upto 20.7%. The delay factor is improved by the factor of the 26.5% as compared to the existing design of the flip-flop.

The paper presents dual edge triggered flip-flop for low power and high performance flip-flop. The proposed dual edge triggered flip-flop achieves a low power by implementing dual edge triggering and conditional discharging technique. Dual edge triggering reducing the power dissipation by half while paying virtually no penalty in the throughput. It also minimizes the latency factor by utilizing the improved fast symmetrical latch. The power factor of the proposed flip-flop design is improved by the factor 20.77%. The delay factor is also improved by the factor of 26.5% by using the TSPICE simulation with 0.18µmCMOS technology.

Mr. G.Venkadeshkumar et.al in [1]. Has designed a low power pulse triggered flipflop (P-FF) design. The design is done by the pulse generation control logic, an AND function, is removed from the critical path to facilitate a faster discharge operation. A simple two-transistor AND gate design is used to reduce the circuit complexity. A conditional pulse enhancement technique is devised to speed up the discharge along the critical path only when needed. As a result, transistor sizes in delay inverter and pulse generation circuit can be reduced for power saving. Various post layout simulation results based on UMC CMOS 90-nm technology reveal that the enhanced pulse triggered FF design features the best power-delay-product performance in seven FF designs under comparison. Its maximum power saving against rival designs is up to 38.4%. Compared with the conventional transmission gate based flip flop design. The average leakage power consumption is also reduced by a factor of 3.52.

The enhanced pulse triggered low-power FF (EPTFF) design by employing two new design measures. The first one successfully reduces the number of transistors stacked along the discharging path by incorporating a PTL-based AND logic. The second one supports conditional enhancement to the height and width of the discharging pulse so that the size of the transistors in the pulse generation circuit can be kept minimum. Simulation results indicate that the proposed design excels rival designs in performance indexes such as power, D to Q delay, and PDP. Coupled with these design merits is a longer hold-time requirement inherent in pulse triggered FF designs. However, hold-time violations are much easier to fix in circuit design compared with the failures in speed or power.

Mr.Peiyi Zhao et.al in [4] presented a new technique for implementing low-energy double-edge triggered flip-flops is introduced. The new technique employs a clock branch-sharing scheme to reduce the number of clocked transistors in the design. The newly proposed design also employs conditional discharge and split-path techniques to further reduce switching activity and short-circuit currents, respectively. As compared to the other state of the art double-edge triggered flip-flop designs, the newly proposed CBS_ip design has an improvement of up to 20% and 12.4% in view of power consumption and PDP, respectively.

The paper surveyed the double-edge clocking flip-flops and classified them into three groups. Conventional DEFF duplicate the latching component, hence duplicating the area and increasing the input loads. The explicit DE pulsed flip-flops have an external pulse generator, so they have higher power consumption. The newly proposed flip flop uses a clock branch sharing scheme to sample the clock transitions, which efficiently reduces the number of clocked transistors and results in lower power while maintaining a competitive speed. It employs the conditional discharge technique and the split path technique to reduce the redundant switching activity and short circuit current, respectively. The flip flop has the least number of clocked transistors and lowest power; hence, it is suitable for use in high-performance and low-power environments.

Mr.Michael Wieckowski et.al.in [9].Has designed the first evaluation of a soft-edge flip-flop as an alternative to useful-skew and latch-based designs for variation compensation in a 16-bit 8-tap FIR filter in 0.13µm CMOS. An 11.2% performance improvement was achieved over a standard hard edge data flip-flop (9.2% when post-silicon useful-skew is applied).

Soft edge clocking based on latch transparency windows is a well-understood technique that has been shown in this work to provide significant gains in performance for modern process technologies plagued by random sources of variation. Since high performance pulsed techniques are intolerant to variation, and hence unsuitable for variation compensation, we have demonstrated a simple soft edge flip-flop technique as a viable alternative. We have demonstrated in silicon that this SFF can achieve gains in performance over 10% compared to traditional designs even under harsh low-voltage conditions. These gains come at minimal area and power penalties and can readily be incorporated into a standard design flow.

Mr.Peiyi Zhao et.al in [11] proposed a new model of conditional discharge flip flop by analyzing conditional precharge and conditional capture flip flop technologies. In this paper, high-performance flip-flops are analyzed and classified into two categories: the conditional precharge and the conditional capture technologies. This classification is based on how to prevent or reduce the redundant internal switching activities. A new flip-flop is introduced: the conditional discharge flip-flop (CDFF). It is based on a new technology, known as the conditional discharge technology. This CDFF not only reduces the internal switching activities, but also generates less glitches at the output, while maintaining the negative setup time and small -to- delay characteristics. With a data-switching activity of 37.5%, the proposed flip-flop can save up to 39% of the energy with the same speed as that for the fastest pulsed flip-flops.

A.Jagadeeswaran et.al in [12] has presented power optimization techniques for sequential elements using pulse triggered flip-flops with svl logic. The concept of this paper is to reduce the power consumption and to increase the speed and functionality of the chip. This project moves around in replacing conventional master-slave based flip flop to a pulse triggered flip flop which acts as a tribute alternate for low power applications. Initially in the critical path the pulse generation controls logic along with SVL function. A simple transistor SVL design is used to reduce the circuit complexity. In this scheme transistor sizes and pulse generation circuit can be further reduce for power saving. Here UMC CMOS 180nm technology is use in SPICE tool to design the proposed structure. This would bring up the result in power saving approximately to 38.4%.

III.CONCLUSION

This paper analyses various methods for designing low power edge triggered and pulse triggered flip flops. The paper discusses about major issues associated while designing flip flops. In the proposed design a new pulse triggered FF with an explicit pulse generator will be designed using modified TSPC latch structure incorporating a mixed design style consisting of pass transistor and pseudo-nMOS logic.

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