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FPGA Implementation of FIR Filter Using Bit Serial Arithmetic Technique

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Abstract: Implementing hardware design in Field Programmable Gate Arrays (FPGAs) is a formidable task. There is more than one way to implement the dsp design for digital FIR filter. The traditional approach is based on application of general purpose multipliers. However, multipliers implemented in FPGA architectures do not allow constructing economic Digital Filters. For this reason, multipliers are replaced by Lookup Tables and Adder Subs tractor, which use Bit-Serial Arithmetic.

Keywords: Digital filter, FIR filter, Look up table

I. INTRODUCTION

A Digital Filter is a Linear Time Invariant (LTI) system which performs numerical calculations on sampled values of the signal. The analog input signal must first be sampled and digitized using an Analog to Digital Converter (ADC). The resulting binary numbers, representing successive sampled values of the input signal, are transferred to the filter, which carries out numerical calculations on them. These calculations typically involve multiplying the input values by constants and adding the products together. If necessary, the results of these calculations which now represent sampled values of the filtered signal, are output through a Digital to Analog Converter (DAC) to convert the signal back to analog form. In the last years digital filters have been recognized as primary digital signal processing (DSP) operation.

There are two basic types of digital filters, Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters. FIR and IIR filters are used in many digital signal processing systems to per- form a variety of signal filtering and conditioning functions. An IIR filter is capable of emulating the transfer functions of analog continuous-time filters, such as low-pass, band-pass, high-pass, and all- pass (phase-shifting) types of filtering IIR filters exhibit similar phase characteristics as their analog counterparts. For arbitrary transfer functions with linear-phase response, FIR filters are utilized and have no equivalent in the analog domain.

On the other hand, the advances in Field Programmable Gate Arrays (FPGA) technology have enabled these devices to be applied to a variety of applications traditionally reserved for Application Specific Integrated Circuits (ASICs). The advantages of the FPGA approach to digital filter implementation include: higher samples rates than those that are available from traditional DSP chips lower costs than an ASIC for Moderate volume applications, and are more flexible than the alternate approaches.

A filtering function is usually carried out by a number of multiplication operations, which are expensive in terms of time and space. Therefore, several techniques are used to minimize the hard- ware needed to implement a filter. A technique widely used is to replace Bit- Parallel by Bit-Serial structures.

Bit-Parallel structures process all the bits of input data simultaneously at a significant hardware cost. Bit-Serial, by comparison, process the input one bit at a time The advantage of the last one is that all the bits pass through the same logic, in a huge reduction in the required hard- ware. Typically, the Bit-Serial approach 1/n of the hardware required for the n-bit parallel design. The price of the logic reduction is that serial hardware takes n clock cycles to execute in one clock cycle. Since for certain classes of applications, FPGA utilization is high, performance goals are achieved while using economically attractive FPGA devices. For applications that require high speed performance, Bit-Parallel structures yield the highest performance.

II. PROBLEM STATEMENT

An Approach to overcome the drawback of using general purpose multiplier used in the FIR filter design. An efficient design methodology which makes use of bit serial arithmetic technique to design economic filters.

III. PROPOSED WORK

This paper is organized as follows

- The bit Serial arithmetic technique
- Structure of FIR Filter
- Experimental results

IV. METHODOLOGY

A. Bit Serial Arithmetic Technique

Bit parallel designs process all of the bits of an input simultaneously at a significant hardware cost. In contrast, a bit serial structure processes the input one bit at a time,

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generally using the results of the operations on the first bits to influence the processing of subsequent bits. The advantage enjoyed by the bit serial design is that all of the bits pass through the same logic, resulting in a huge reduction in the required hardware. Typically, the bit serial approach requires $1/n^{th}$ of the hardware required for the equivalent n-bit parallel design. The price of this logic reduction is that the serial hardware takes n clock cycles to execute, while the equivalent parallel structure executes in one. The time-hardware product, however, for the serial structure is often smaller than for equivalent parallel designs because the logic delays between registers are generally significantly smaller. This means that the serial machine can operate at a higher Clock frequency In the case of FPGAs; signal routing contributes significant propagation delays and often uses up logic cells.

The serial structures tend to have very localized routing, often to only one destination. In contrast, the parallel machines usually need signals extended across the width of the processing element. The limited and slow routing resources in FPGAs make the serial processing elements even more attractive. In some cases, the overall throughput for a serial design implemented in an FPGA can actually exceed of an equivalent parallel design in the same device.

B. FIR Filter Design

In a FIR-Digital Filter the output depends only of present and previous input samples, which are multiplied by a set of coefficients and then added together to produce the output. The filter behaviour is determined by the filter coefficients. A general FIR-filter is characterized by the following equation

$$y^n=a_0x^n+a_1x^{n-1}+\ldots\ldots\ldots+a_qx^{n-p}$$

where p is the filter order, the a_p are the filter coefficients, x^n is the input signal at the time step n, and y^n is the output signal at the step n.

The major disadvantage of these filters is that usually a large number of coefficients are required to control adequately their frequency response. Practical FIR-Filters typically need between 10 and 150 coefficients.

This makes them slower in operation than most IIR-filter design. Expanding the above equation

$$y^n=\Sigma 2^j f(x^n_j,x^{n-1},\ldots,x^{n-p})-f(x_0{}^n,x^{n-1}{}_0,..,x^{n-p}{}_0)$$

Fig below shows the architecture to compute the filter equation

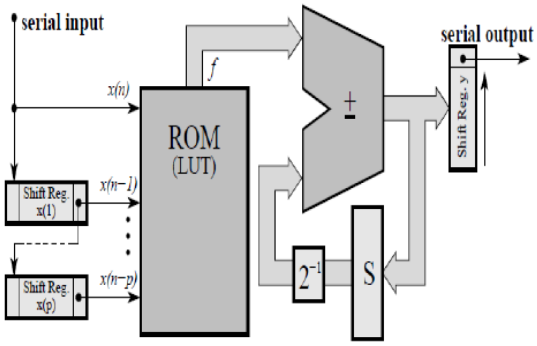

Fig. 1: FIR Filter Using Bit Serial Arithmetic

As we know FIR filters have no feedback coefficients. Due to this, a After *l*+1 cycles, the adder-Subtracter output is only stored into y(n) register.

C. Experimental Results

The filter implementation consist o f 8 bit input samples and there coefficients have 12 bit precision. The FPGA selected was Spartan 3AN kit.

Project File:	bit_serial.ise	Current State:	Synthesized
Module Name:	bitserial_main	• Errors:	No Errors
Target Device:	xc3s50an-4tqg144	• Warnings:	18 Warnings
Product Version:	ISE 10.1 - Foundation	• Routing Results:	
Design Goal:	Balanced	• Timing Constraints:	
Design Strategy:	Xilinx Default (unlocked)	• Final Timing Score:	

bit_serial Partition Summary

No partition information was found.

Device Utilization Summary [estimated values]

Logic Utilization	Used	Available	Utilization
Number of Slices	35	704	4%
Number of Slice Flip Flops	39	1408	2%
Number of 4 input LUTs	56	1408	3%
Number of bonded IOBs	11	108	10%
Number of GCLKs	1	24	4%

Table.1: Design Summary of FIR filter bit serial arithmetic technique

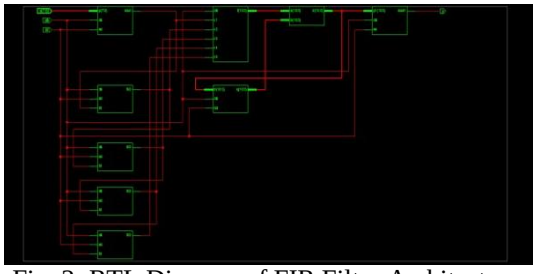

Fig. 2: RTL Diagram of FIR Filter Architecture

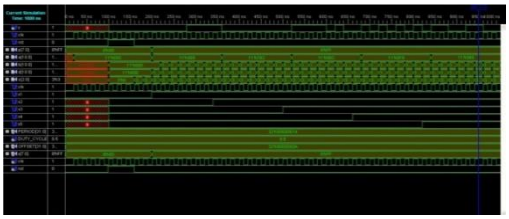

Fig.3: Simulation Waveform of 8 Bit FIR filter Architecture

V. CONCLUSION

The presented paper results allows us to construct the higher order economic FIR filters and using interconnection techniques without the of use huge look up tables. The result produced by these techniques can be straight forward translated from their schematic representation into VERILOG code and then synthesize it on an FPGA SPARTAN 3AN.

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BIOGRAPHY

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