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Low-Power Architectures and Self-Calibration Techniques of DAC for SAR-ADC implementation

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Abstract: SAR-ADC is best suited for low power applications where power has a trade-off with speed. Use of redundant circuitry reduces the on chip area making it cost effective. DAC is one of the components of SAR-ADC that introduces error voltage due to mismatch and consumes large power other than comparator. Low power DAC architectures have been studied and analysed. To account for capacitor mismatch issues self-calibration techniques have been discussed and analysed for 14-bit DAC implementation. All the architectures have been analysed for 100KS/s with 1.6MHz clock speed in 180nm technology with supply voltage of 1.8V. EDA tool used for design analysis is Cadence® Spectre®.

Keywords: Successive Approximation Register Analog-to-Digital Converter (SAR-ADC), Digital-to-Analog Converter (DAC), Electronic Design Automation (EDA), Least Significant Bit (LSB), Calibration.

I. INTRODUCTION

For the most biomedical applications stringent low power design with comparable resolution is preferred. Among the various ADC architectures SAR-ADC fits the most as because of its redundant circuitry use at relative low clock rates reduces power dissipation effectively [1]. All though resolution is not as good as of Sigma-Delta ADC architecture but its oversampling rate introduces countable power dissipation. DAC in SAR-ADC architecture consumes noticeable power and is counted for introducing errors due to mismatch and thermal noise. Instead of resistive DAC the capacitive DAC architectures are preferred as it reduces extra need of sampling circuitry; consume less power and saves on chip area. Beside this other issues comes into picture like capacitor mismatch, thermal noise limitations, parasitic influence, etc. But the pros overcome the cons of using capacitive architecture. There are many calibration techniques that reduce error voltage due to capacitive mismatches like foreground and background calibration techniques. Here in this paper foreground calibration techniques specifically Self-calibration technique is analysed and discussed.

II. DAC ARCHITECTURES

For SAR-ADC implementation capacitive DAC architectures are commonly used for low power designs these day's because of their enormous advantages over other DAC architectures.

A. Charge Scaling DAC

Charge scaling DAC is preferred over the other architectures because of ease of design and the three operations being performed on the same structure *i.e.* (1) Sampling (2) Subtraction node, and (3) DAC operation. Charge scaling DAC works on the principle of charge storage and charge redistribution. During the sampling phase the charge is stored in the capacitors corresponding to the voltage difference (VIN-Vbias) across its plate's *i.e.*

$$Q = C * \Delta V$$
$$\Delta V = VIN - Vbias$$

During the conversion time the charge is distributed across all the capacitors. All the capacitors used are binary weighted with respect to unit capacitance C (in fF) as shown in Fig. 1.

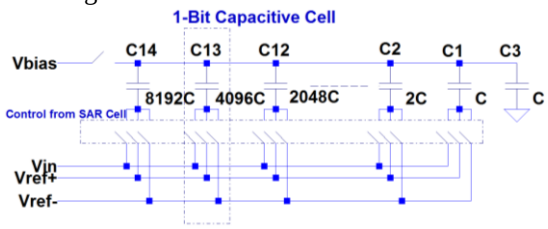

Fig. 1 Capacitive Charge scaling DAC

Impact of thermal noise and quantization noise is taken into consideration for calculation on unit capacitance limit and their sum should be limited to the half of DAC-LSB.

$$\sqrt{\frac{kT}{C_{Total}} + \frac{LSB^2}{12}} \leq \frac{LSB}{2} \quad ..(1)$$

Where, $LSB = \frac{1.8}{2^{14}} = 0.109mV$

$$\therefore C_{Total} \geq 2.0589\,pF \text{ for T} = 300^0\text{K} \quad ..(2)$$

Also, C_{Total} for the given architecture can be calculated as:

$$C_{Total} = 16384C\,, where\ C = unit\ capacitance \quad ..(3)$$

From eqns. (2) and (3)

$$C \geq 0.12567fF$$

The imposed limitation for the minimum capacitance in 180nm technology is 1.2 fF. At this minimum value a little capacitance mismatch can introduce large (more than 1LSB) error voltage at output node. Thus for the analysis 15fF of unit capacitor is used.

For higher resolution DAC's (*i.e.* ≥ 10-bit) total capacitance of DAC increases exponentially thus an

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exponential rise in total power dissipation is estimated as [2]:

P= Power consumed during sampling + During Conversion

$$P = f_s * \frac{1}{2} * C_{Total} * \left(\frac{V_{Range}}{2}\right)^2 + 0.5 * f_s * C_{Total} * {V_{Ref}}^2 \quad ..(4)$$

From eqn. (4), C_{Total} has a direct influence on power consumption which is very large for high resolution DAC. Here, for C_{Total} is equal to 245.76pF for 14-bit DAC. Other issue is the large settling time of the MSB capacitor node voltage as the RC-time constant is very large and can be greater than the clock period for high resolution DAC. Thus it imposes a restriction on the clock period and slows down the operation. Also, the large capacitor increases on-chip area and hence the fabrication cost.

B. Split-Capacitor DAC

For the design of high resolution DAC, split-capacitor DAC architecture is used, as it can significantly reduces the capacitor size and thus the power dissipation. The MSB capacitor value reduces from $2^{N-1}C$ to $2^{\frac{N}{2}-1}C$ with the use of single split capacitor. Limitation imposed on using Split capacitor is that only even resolution bits can be implemented. Also, with the use of split-capacitor the output node becomes sensitive to parasitic capacitance. Parasitic capacitances P_1 and P_2 as shown in Fig. 2 has the charge difference at the beginning and at the end of the conversion depending on the value of VIN thus making input dependent fluctuations and introducing non-linearity[3].

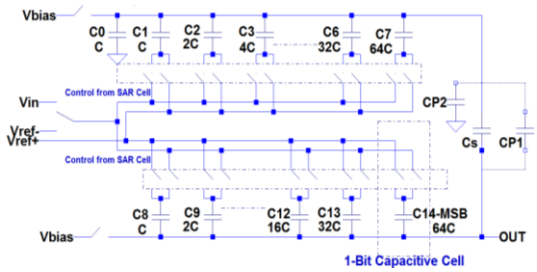

Fig. 2 Split Capacitor DAC

The value of unit capacitance is calculated using the eqn. (1) but C_{Total} here follow different relation to unit capacitance *i.e.*

$$C_{Total} = \left[2^{N\backslash 2} + \left(2^{N\backslash 2} - 1\right)\right]C \quad ..(5)$$

Using eqns. (1) and (5) unit capacitor can be calculated; whose value is almost the same as previous. Hence, again a unit capacitor of 15fF has been chosen. Value of split capacitor can be calculated as:

$$C_S = \frac{Left\ hand\ side\ cpacitances}{Right\ hand\ side\ capacitan\ ces} = \frac{2^M}{2^M - 1} = \left(1 + \frac{1}{127}\right)C$$

Value of unit capacitance C is 15fF and M is equal to N/2 = 7 that means 15.11811fF is the exact value of C_S which is very difficult to obtain precisely because of the process variations during fabrications will lead to mismatch and will add non-linearity. Also, the switches cause charge injection problem and the parasitic capacitances, the drain to body capacitance C_{db} for nmos and source to body capacitance C_{sb} of pmos adds to the output node capacitance which is very significant for a very low LSB DAC designs. For low LSB-DAC designs, stack transistor transmission gate as shown in Fig. 3 is used as switch to reduce settling error voltage during sampling stage which should be less than 0.5LSB and also leakage current is reduced for small input voltages [4]. The total power dissipated by the Split-capacitor DAC to convert a sample corresponding to full input swing *i.e.* 1.8V is found to be 12.537nW.

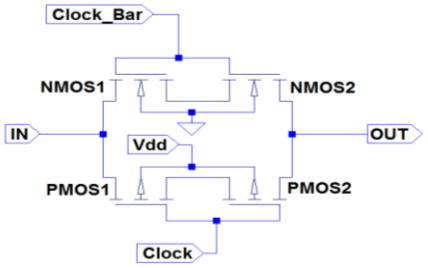

Fig. 3 Stacked Transistor TG as a switch

C. Unit Split-Capacitor DAC

Unit capacitor is used as a split capacitor i.e. $C_S = C$ and the last dummy capacitor C0 is removed as shown in Figure 4. Function of C0 was only to make circuit operate at 1LSB less to full swing and Unit spilt causes a gain error that is well within 1LSB margin and can be neglected. In case of unit split capacitor, total power dissipated for the same sample of full input swing is 12.587 nW.

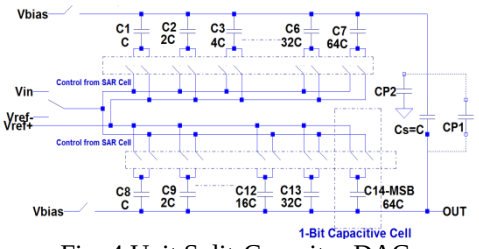

Fig. 4 Unit Split-Capacitor DAC

D. Top Plate Sampling DAC

Another architecture that can be used is top plate sampling DAC. Operation of this DAC is similar to charge scaling DAC except sampling is done on the top plate of capacitors instead of the bottom plates. In bottom plate sampling when full input swing is sampled DAC output may go beyond the rail. So, to avoid either input swing can be decreased with reduction in SNR or to use top plate sampling [4]. In top plate sampling DAC, during the sampling the MSB is preset and on the next pulse the comparator of SAR-ADC checks weather to force high or low. If low is desired, then it is forced in the next consecutive pulse by SAR logic.

III. CALIBRATION TECHNIQUES

Calibration is done to reduce the impact of the process variations and component non-linearity. There are two domains of calibration - foreground and background. In foreground calibration, chip is calibrated for mismatch or non-linearity before its normal operation and in background calibration mismatches are calibrated instantaneously on each bit during the operation [5]. However, background calibration requires an overhead circuitry and therefore some power.

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Foreground calibration technique introduces less overhead circuitry as compared to background calibration where memory functions are commonly employed to store the mismatches. Self-calibration is used to account for capacitor mismatches in DAC due process variations.

A. Split-Capacitor Mismatch Calibration

In this calibration technique, the value of split capacitor is kept slightly larger than the ideal fractional value and a tuneable capacitor C_C is placed on the top side of the split DAC to compensate for mismatches as shown in Fig. 5. Calibration is done in three modes (1) Pre-charge (2) Charge Redistribution and (3) Mismatch calibration.

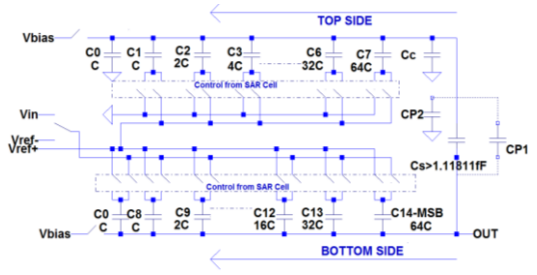

Fig. 5 Split-Capacitor DAC with mismatch calibration

During calibration all the bottom side capacitors in Fig. 5 are grounded except the lowest bit. Pre-charging is done by connecting top plates of both top and bottom side capacitors to Vbias and bottom plate of capacitor, C0 of bottom side is set to '0'. Bottom plate of all top side capacitors are connected to '11111111' where logic '1' corresponds to Vref+. During charge redistribution phase Vbias is disconnected from top plates of top and bottom side capacitors and charge previously stored is redistributed. Simultaneously, the voltage at the bottom plates of both top and bottom side capacitors are swapped. Due to mismatch (if Cc is small) OUT voltage becomes less than Vbias and this counts to capacitor mismatch. Mismatch calibration is done by increasing the value of C_C with successive clock pulses. C_C can be implements as shown in Fig. 6 [6]. Minimum value of mismatch which can be calibrated is 0.5C and maximum mismatch which can be calibrated is 8C, C is the unit capacitor.

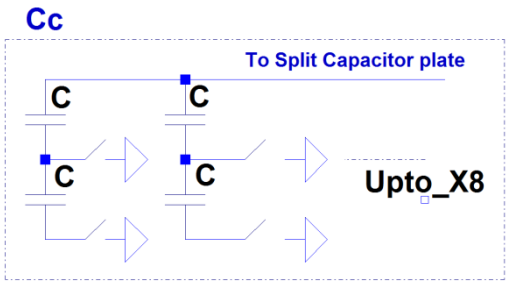

Fig. 6 Implementation of Cc

This calibration technique can effectively improve the linearity performance and reduce the gain error as well. Once the DAC is switched on, this calibration occurs every time for first few clock pulses.

B. Unit Split-Capacitor Mismatch Calibration

As in previous technique, here also sampling is done on the bottom side bits only thus reducing the input capacitance of the main DAC (MDAC) for the sampled input. Here, calibration of the unit split DAC architecture is done in same manner as discussed in the previous section-A. But the implementation is different as shown in Fig. 7. Instead of a tuneable capacitor, another DAC called as CDAC, has been used to calibrate the mismatch. Dummy capacitor is connected at the bottom side and is used for calibration only.

Aim of the calibration here is to match the value of C_{C1} with C_{C2} that counts for the major mismatch of the MDAC *i.e.*

$$C_{C1} = C_{C2} = \sum_{i=D,1\ldots}^{NS-1} C_i \quad where\ NS = 0,1 \ldots (M-1)$$

M = N/2 and N is number of bits of MDAC.

Here, in case MSB of the bottom side (CC1) is matched with the remaining bottom side bits (CC2). During the first two stages or clock pulses, bottom plates of all the other capacitors are grounded. During pre-charging top plates of both bottom side and top side are kept at Vbias. MSB is kept at '0' and other bits of bottom side at '1111111', where logic '0' corresponds to Vref- and logic '1' corresponds to Vref+. On next pulse charge redistribution is done by disconnecting the Vbias and swapping the voltages of bottom plates of the C_{C1} and C_{C2}. Thus, at the OUT node a significant change in voltage can be measured which counts for the capacitor mismatch. On the next subsequent pulse, mismatch calibration is done by adding the capacitances through the CDAC which operates on the same SAR logic as MDAC operates on. The bottom plates of CDAC are either kept at Vref+ or Vref- [7].

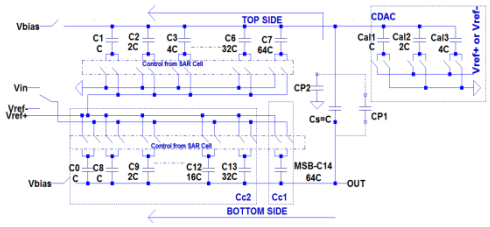

Fig. 7 Unit Split-Capacitor DAC with mismatch calibration

IV. CONCLUSION

Various design issues in DAC architectures have been discussed and analyzed. Capacitive DAC implementation reduces need of extra circuitry and split-capacitor DAC reduces the overall power dissipation making it suitable for the low power applications. Use of unit split capacitor reduces the fabrication efforts as compared to non-integer split capacitor with compromise on gain error. Calibration techniques have been discussed which are used to reduce the capacitor mismatch, improve the linearity of DAC and reduce the gain error.

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BIOGRAPHIES

Atul Thakur received the B.Tech. degree in Electronics and Communication Engineering with distinction from Punjab Technical University, Jalandhar, Punjab , India in 2010. He is currently pursuing the M.Tech. degree from Thapar University (TU), Patiala, Punjab, India. His research interest includes low power analog-to-digital convertors, smart data convertor design for bio-medical applications.

Alpana Agarwal received the M.Sc. and M.Tech. Degrees from IIT-Delhi, India in 1986 and 1988 respectively, and the Ph.D. degree from Thapar University Patiala, India. She worked as a Scientist at IC Design Group in CEERI-Pilani, Rajasthan, India from 1988 to 1996. In 1996, she joined Thapar University as a faculty in ECED Department where she is currently working as an Associate Professor. Her research interests include VLSI Circuit and System Design-Synthesis, Design Automation and ASIC Design.