ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 2, Issue 7, July 2014

Multilevel Inverter Topology And Modulation Techniques: A Review

Arpita[1], Tali Nagwani[2]

P.G. Scholar, Department of Electrical Engineering, OIST, Bhopal India[1]

Assistant Professor, Department of Electrical Engineering, OIST, Bhopal[2]

Abstract: The requirement of high-voltage, high-power converters capable of producing high-quality waveforms forced the development of power switching and reduced switching frequency devices and equipments. Multilevel inverters proved itself as a vital utility with regard to semiconductor power switch voltage limit barriers. Presently research is ongoing to improve their capabilities further through optimized control techniques, and to minimize both component count and manufacturing cost. Owing to voltage limits power switches are typically cascaded in series and configured as multilevel structures. The outputs thus obtained are superior in quality resulting in reduced filter and overall system size requirement. Switching losses are greatly reduced, with lower switching frequency operation while mentaining high-power quality**.**

Keywords: Cascaded H-bridge, cascaded neutral-point, capacitor clamped inverter, five-level inverter, multicarrier phase-shifted pulse-width modulation (MCPS-PWM), multilevel inverter (MLI), transistor-clamped inverter

I. INTRODUCTION

The multilevel inverter has been implemented in various applications ranging from medium to high-power levels, such as motor drives, power conditioning devices also conventional or renewable energy generation and distribution[1]–[8]. There are several basic configurations for multi-level inverters, and each of them has its advantages and disadvantages w.r.t. others. Output voltages is produced by adding or subtracting several distinct DC voltages to/from others.

II. DIODE CLAMPED MULTILEVEL INVERTER

The inverter utilises diodes to provide multiple voltage levels through the different phases to the capacitor banks which are in series as shown in Figure 1. A diode transfers a limited amount of voltage, thereby reducing the stress on other electrical devices. The maximum output voltage is half of the input DC voltage.

TABLE I
DIODE CLAMPED CONVERTER COMPONENT COUNT

Component	Number
Levels	m
Switches & Parallel diodes	2(m-1)
Capacitors	m-1
Clamp diodes	(m-1)(m-2)

The main advantages of diode clamped inverters are Back-to-back topology is possible and used for high-voltage back-to-back inter-connection or an adjustable speed drive, The capacitors can be pre-charged as a group, Efficiency is high for fundamental frequency switching[9]. While the limitation is that Real power flow is difficult for a single inverter and the number of clamping diodes required is related to the number of levels. Table 1 shows the component count for a diode clamped converter.

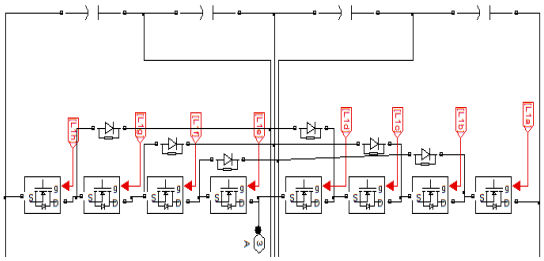

Figure 1: Diode clamped multi-level inverter phase limb

III. FLYING CAPACITORS MULTILEVEL INVERTER

The main concept of this inverter is to use series connection of capacitor clamped switching cells. The capacitors transfer the limited amount of voltage to electrical devices.

The operating principle is similar to that of the diode-clamped converter and can be extended to higher numbers of output levels and clamping diodes are not required in this type of multilevel inverters.

The major merits of this type are; huge amount of storage capacitors provide additional ride through capabilities during power rage, Switch combination redundancy is provided for balancing different voltage levels and Control of both the real and reactive power flow can be done [10].

While the prominent drawbacks include; A huge amount of storage capacitors is required which are expensive, the switching frequency and switching losses will are high for real power transmission and the converter control gets very complicated.

Table 2 shows the component count for a diode clamped converter.

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 2, Issue 7, July 2014

TABLE II
FLYING CAPACITOR CONVERTER COMPONENT COUNT

Component	Number
Levels	m
Switches & Parallel diodes	2(m-1)
Capacitors	m-1
Clamp diodes	(m-1)(m-1/2)

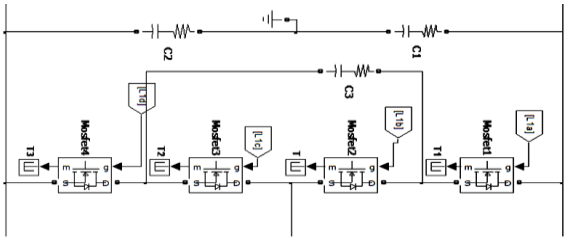

Figure 2: Flying capacitor multi-level inverter limb per phase

IV. CASCADED H- BRIDGE MULTILEVEL INVERTER

The cascaded H-bride multi level inverter requires less number of components in each level. This topology [11] consists of series of power conversion cells called an H-bridge and gives separate input DC voltage for each H-bridge. Each cell can provide three different voltages like zero, positive DC and negative DC voltages. The advantages of this topology are : Has the least number of components among all multilevel converters to obtain same number of voltage levels, Modularized circuit packaging is possible as each level has the same structure, Soft switching can be used. While they suffer from a major drawback as they require separate dc sources for real power conversions, and therefore its application is limited. The number of components required for a diode clamped converter is shown in Table 3.

TABLE III
CASCADED H-BRIDHE COMPONENT COUNT

Component	Number
Levels	M
Switches & Parallel diodes	2(m-1)
Clamp diodes	(m-1/2)

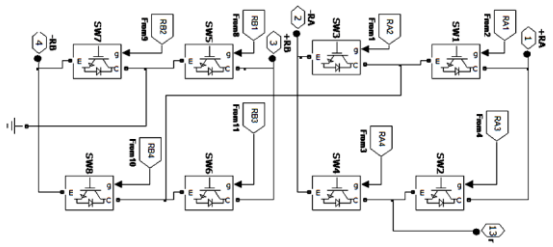

Figure 3: Cascaded H-bridge multi-level inverter limb per phase

V. MODULATION STRATEGIES

In order to obtain output of desired pattern a definite modulation strategy is used. This strategy describes the characteristic of a device. Modularity also permits the cascaded multilevel inverter to be stacked easily for high-power and high-voltage applications. Modulation strategies applied to multilevel inverters are

- selective harmonics elimination [12]
- carrier-based PWM[13]
- space vector modulation (SVM) [15]
- fundamental frequency modulation [16]

Generally, among the three topologies, the cascaded multilevel inverter has the potential to be the most reliable and achieve the best fault tolerance owing to its modularity; a feature that enables the inverter to continue operating at lower power levels after cell failure.

The cascaded multilevel inverter typically comprises several identical single phase H-bridge cells cascaded in series at its output side. This configuration is commonly referred to as a cascaded H-bridge (CHB), which can be classified as symmetrical if the dc bus voltages are equal in all the series power cells, or as asymmetrical if otherwise. In an asymmetrical CHB, dc voltages are varied to produce more output levels [2]. Consequently, inverter design becomes more complicated as each power cell has to be sized accordingly to the different power levels, including isolated dc sources. This makes symmetrical CHB modularity advantageous over asymmetrical with regard to maintenance and cost. For the symmetrical cascaded inverter, voltage level increase is possible without varying dc voltage with the same number of power cells[18], a three-phase cascaded multilevel inverter that uses five-level transistor-clamped H-bridge power cells using Multicarrier phase-shifted pulse-width modulation method fundamental is shown in Figure 5(b), to achieve balanced power distribution among the power cells.

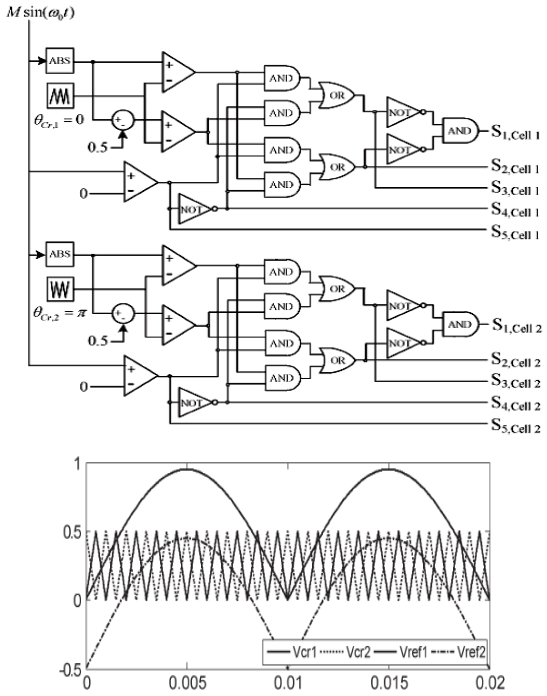

Figure 5: (a) PWM signal generation circuitry (b) Multicarrier phase-shifted PWM for two-cell configuration.

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 2, Issue 7, July 2014

The analysis of the output voltage harmonics and the total power losses covering the conduction and the switching power losses are carried out and compared with the cascaded neutral-point-clamped and the conventional cascaded H-bridge inverter.

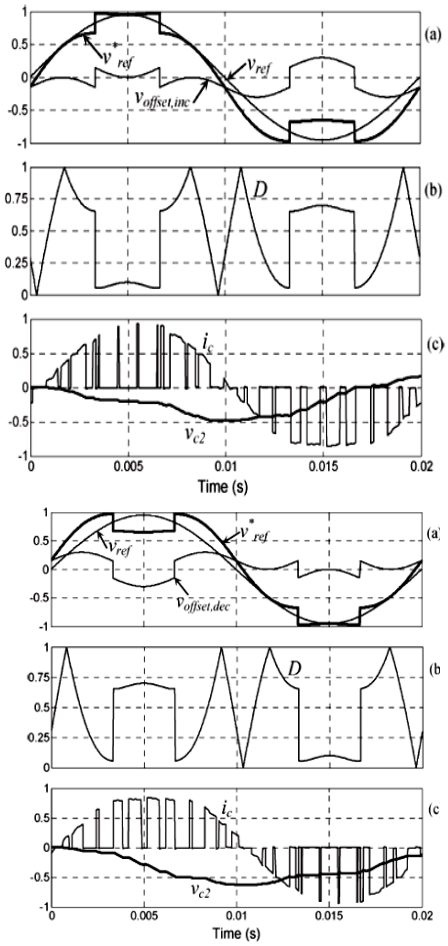

Figure 7: (a) Offset voltage to vary the midpoint capacitor voltage and the corresponding voltage reference, (b) duty cycle, (c) midpoint capacitor current and voltage.

Recently, the transistor clamped converter topology has received increased attention as it provides a simpler approach to increase output levels by taking different voltage levels from the series stacked capacitors [11], this configuration uses a five-level transistor-clamped H-bridge (TCHB) as a power cell that can produce a five-level output instead of three-level as with the conventional H-bridge [17].

A similar arrangement using a NPC in each power cell has been presented [3]. However, an excessive number of power switches and diodes are required. In [14], though the number of switches for each cell is lower, and to achieve the same output quality, more cells are required, which increases the number of isolated dc sources, as well as bulky transformers.

The midpoint capacitor in the concern inverter the midpoint capacitor voltage needs to be adjusted in order to obtain balanced output voltage and uniform losses in the switching devices.

TABLE IV
PHASE-TO-NEUTRAL VOLTAGE FOR TWO-CELL CONFIGURATION

	Va1	Va2	VaN
0<Vref<1/2	0	0	0
	1/2Vdc	0	1/2Vdc
	0	1/2Vdc	1/2Vdc
	1/2Vdc	1/2Vdc	Vdc
½<Vref≤1	1/2Vdc	1/2Vdc	Vdc
	Vdc	1/2Vdc	3/2Vdc
	1/2Vdc	Vdc	3/2Vdc
	Vdc	Vdc	2Vdc
-½<Vref≤ 0	0	0	0
	-1/2Vdc	0	-1/2Vdc
	0	-1/2Vdc	-1/2Vdc
	-1/2Vdc	-1/2Vdc	-Vdc
-1<Vref≤-½	-1/2Vdc	-1/2Vdc	-Vdc
	-Vdc	-1/2Vdc	-3/2Vdc
	-1/2Vdc	-Vdc	-3/2Vdc
	-Vdc	-Vdc	-2Vdc

The offset voltage command is shown in Figure 7 and the capacitor voltage and current. The phase to neutral voltage for two cell configuration is given in table 4, that provides preliminary idea of the inverters output voltages.

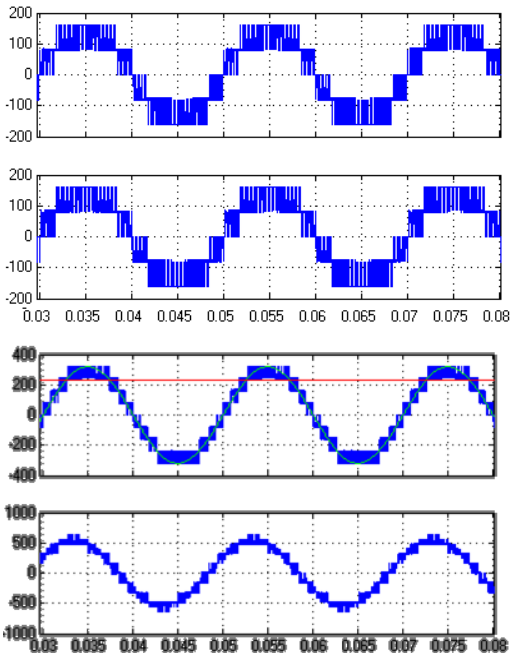

Fig. 8: Output voltage of TCHB inverter (a) Cell 1 output voltage & Cell 2 output voltage. (b) Phase & Line voltage.

VI. CONCLUSION

The Multilevel inverter configurations are analytically reviewed and a transistor clamped half bridge inverter power cell with multicarrier phase shifted PWM modulation method is reviewed comprehensively. It is hence summarised that the inverter configuration offers multiple merits but requires a mechanism to balance the midpoint capacitor voltage in each cell based on third harmonic offset injection. The output voltages of the TCHB inverter are shown in figure 8.

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 2, Issue 7, July 2014

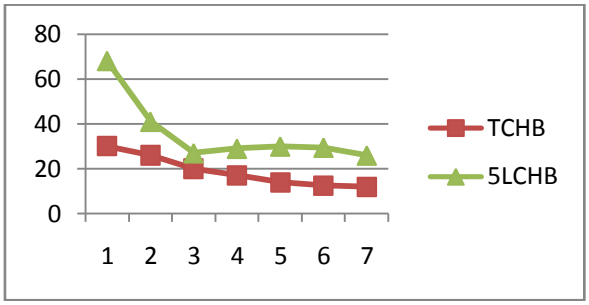

Fig. 9: Line voltage THD of the TCHB inverter and CHB multilevel inverters.

Table 5: Comparison between the TCML inverter and the other multilevel inverters

Parameter	TCMLI	NPC	CHB
Phase voltage	$2n_p$-1	$2n_p$-1	$2n_p$-1
Line voltage	$4n_p$-3	$4n_p$-3	$4n_p$-3
Power cells per phase	$(n_p-1)/2$	$(n_p-1)/2$	(n_p-1)
Power s witches	$5/2(n_p-1)$	$4(n_p-1)$	$4(n_p-1)$
Clamping diodes	0	$2(n_p-1)$	0
Capacitors per phase	n_p-1	n_p-1	n_p-1
Isolated DC sources per phase	$(n_p-1)/2$	$(n_p-1)/2$	(n_p-1)
Power per cell	$2P/(3(n_p-1))$	$2P/(3(n_p-1))$	$P/(3(n_p-1))$
Harmonic distortion	Low	Low	Low
Efficiency	Medium	Low	Low
Output Quality	High	High	High

Detailed comparisons between the TCHB inverter, cascaded NPC, 5L-CHB, and 9L-CHB in terms of power quality, power losses and inverter specifications were presented in Table 5 and the harmonic distortion index is presented in Figure 9. From the findings, the proposed inverter is found potential not only for medium-voltage drive application but also other applications demanding higher output quality.

ACKNOWLEDGMENT

The authors would like to acknowledge the Department of Electrical & Electronics Engineering, Oriental Institute of Science & Technology, Bhopal , India for providing the necessary setup and guidance towards the initiation of this research work.

REFERENCES

[1] P. W. Hammond, "A new approach to enhance power quality for medium voltage AC drives," IEEE Transactions on Industrial Application., vol. 33, no. 1, pp. 202–208, Jan./Feb. 1997.

[2] F. Khoucha, S. M. Lagoun, K. Marouani, A. Kheloui, and M. El Hachemi Benbouzid, "Hybrid cascaded H-bridge multilevel-inverter inductionmotor- drive direct torque control for automotive applications," IEEE Trans. Ind. Electron., vol. 57, no. 3, pp. 892–899, Mar. 2010.

[3] B. Ge, F. Z. Peng, A. T. de Almeida, and H. Abu-Rub, "An effective control technique for medium-voltage high-power induction motor fed by cascaded neutral-point-clamped inverter," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2659–2668, Aug. 2010.

[4] H. Akagi and R. Kondo, "A transformerless hybrid active filter using a three-level Pulsewidth Modulation (PWM) converter for a mediumvoltage motor drive," IEEE Trans. Power Electron., vol. 25, no. 6, pp. 1365–1374, Jun. 2010.

[5] A. Varschavsky, J. Dixon, M. Rotella, and L. Moran, "Cascaded ninelevel inverter for hybrid-series active power filter, using industrial controller," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2761–2767, Aug. 2010.

[6] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems," IEEE Trans. Ind. Electron., vol. 56, no. 11, pp. 4399–4406, Nov. 2009.

[7] N. A. Rahim and J. Selvaraj, "Multistring five-level inverter with novel PWM control scheme for PV application," IEEE Trans. Ind. Electron., vol. 57, no. 6, pp. 2111–2123, Jun. 2010.

[8] P. Lezana and R. Aceiton, "Hybrid multicell converter: Topology and modulation," IEEE Trans. Ind. Electron., vol. 58, no. 9, pp. 3938–3945, Sep. 2011.

[9] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

[10] F. Z. Peng, J. W. McKeever, and D. J. Adams, "Cascade multilevel inverters for utility applications," in Proc. Int. Conf. Ind. Electron. Control Instrum., 1997, vol. 2, pp. 437–442.

[11] M. F. Escalante, J. C. Vannier, and A. Arzande, "Flying capacitor multilevel inverters and DTC motor drive applications," IEEE Trans. Ind. Electron., vol.49, no.4, pp.809–815, Aug.2002.

[12] N. Yousefpoor, S. H. Fathi, N. Farokhnia, and H. A. Abyaneh, "THD minimization applied directly on the line-to-line voltage of multilevel inverters," IEEE Trans. Ind. Electron., vol. 59, no. 1, pp. 373–380, Jan. 2012.

[13] J. Selvaraj and N. A. Rahim, "Multilevel inverter for grid-connected PV system employing digital PI controller," IEEE Trans. Ind. Electron., vol. 56, no. 1, pp. 149–158, Jan. 2009.

[14] G. Waltrich and I. Barbi, "Three-phase cascaded multilevel inverter using power cells with two inverter legs in series," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2605–2612, Aug. 2010.

[15] B. Vafakhah, J. Salmon, and A. M. Knight, "A new space-vector PWM with optimal switching selection for multilevel coupled inductor inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2354–2364, Jul. 2010.

[16] L. Yu, H. Hoon, and A. Q. Huang, "Real-time algorithm for minimizing THD in multilevel inverters with unequal or varying voltage steps under staircase modulation," IEEE Trans. Ind. Electron., vol. 56, no. 6, pp. 2249–2258, Jun. 2009.

[17] N. A. Rahim, M. F. M. Elias, and H. W. Ping, "A three-phase five-level inverter for DTC drives application," IEICE Electron. Exp., vol. 8, no. 1, pp. 1–7, 2011.

[18] Arpita [1], P.G. Scholar, Power Systems, Department of electrical and electronics engineering, OIST, Bhopal, India,

[19] Tali Nagwan[2], Asst Prof, Department of electrical and electronics engineering, OIST, Bhopal, India,