

# Design Methodology of Neural Network for Signal Processing

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**Abstract :** There is various new & advance technologies in medical science we are trying to process the information artificially as our biological system performs inside our body. The main focus of the paper is on the implementation of Neural Network Architecture (NNA) with on chip learning in analog VLSI for generic signal processing applications. In the paper we used analog components like Gilbert Cell Multiplier (GCM), Neuron activation Function (NAF) are used to implement artificial NNA. Artificial intelligence through a biological word is realized based on mathematical equations and artificial neurons. The analog component is used for the compress of multipliers and adder in neural network, which is along with the tan-sigmoid function circuit using MOS transistor in sub threshold region. To trained the neural architecture we used the back propagation algorithm in analog domain with new techniques of weight storage. Layout design and verification of the proposed design is carried out using microwind3.1 software tool. The technology used in designing the layout is 45nm CMOS technology.

**Keyword:** Neural Network Architecture, Back Propagation Algorithm.

## INTRODUCTION

### Neural network :

The implementation of neural network architecture using back propagation algorithm for data compression. The neuron selected is comprises of multiplier and adder along with the tan-sigmoid function. The training algorithm used is performed in analog domain thus the whole neural architecture is a analog structure.

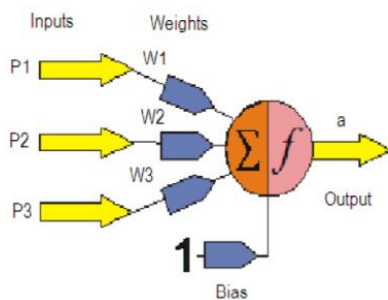


Figure 1: Neural Network

Figure 1 can be expressed mathematically as,  
 $a = f(P1W1+P2W2+P3W3+Bias)$

where „a\_ is the output of the neuron & „p\_ is input and „w\_ is neuron weight . In this neural network we used a neuron, this neuron itself a simple processing unit which has an associated weight for each input to strengthening it and produces an output. The working of neuron is to add together all the inputs and calculating an output to be passed on. The neural architecture is trained using back propagation algorithm and also it is a feed forward network. The designed neuron is suitable for both analog and digital applications. The proposed neural architecture is capable of performing operations like sine wave

learning, amplification and frequency multiplication and can also be used for analog signal processing activities. The purpose of this paper is to design the application for the compression and decompression of the signal. We used the multiple layers of neurons to fulfil this application. The set of single layer neurons are connected with each other it forms a multiple layer neurons, as shown in the figure 2.

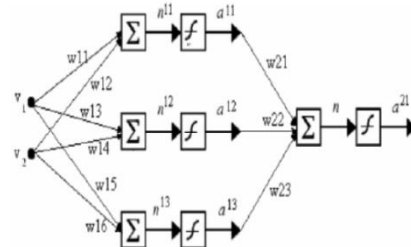


Figure 2: Layered structure of Neural Network

From the above figure that weights w11 to w16 are used to connect the inputs v1 and v2 to the neuron in the hidden layer. Then weights w21 to w23 transferred the output of hidden layer to the output layer. The final output is a21.

### Literature Review & Related work:

[1] Neeraj Chasta 1, Sarita Chouhan2 and Yogesh Kumar3 review of related work and published literature he design the implementation of Neural Network Architecture (NNA) with on a chip learning in analog VLSI for generic signal processing applications . He also say that Neural network with their remarkable ability to derive meaning from complicated or imprecise data can be

used to extract patterns and to detect trends that are too complex to be noticed by either humans or other computer techniques. Due to its adaptive learning, self-organization, real time operations and fault tolerance via redundant information coding properties it can be used in Modelling and Diagnosing the Cardiovascular System and in Electronic noses which has several potential applications in telemedicine. Another application developed was “Instant Physician” which represents the “best” diagnosis and treatment. This work can be further extended to implement neuro fuzzy system with high speed low power.

[2] Vincent F. Koosh, Rodney Goodman review of related work and published literature, it is observed that a VLSI implementation of a neural network has been demonstrated. Digital weights are used to provide stable weight storage. he also say that analog multipliers are used because full digital multipliers would occupy considerable space for large networks. Although the functions learned were digital, the network is able to accept analog inputs and provide analog outputs for learning other functions. A parallel perturbation technique was used to train the network successfully on the 2-input AND and XOR functions.

[3] From the continuous survey it is observed by B. M. Wilamowski, J. Binfet, and M. O. Kaynak Fuzzy controllers do have several advantages such as simple rule based design, but they usually produce relatively raw control surfaces, which are not acceptable for precision control. These fuzzy control surfaces also exhibit larger errors, 908.4 and 296.5. With the neural network approach presented in this paper, the resulting control surfaces are very smooth. Although the presented examples were for a two input case, the general nature of neural systems is such that they can easily handle multidimensional problems. This is not true for the fuzzy systems where the number of inputs is severely limited because with an increased number of inputs, the size of the rule table grows exponentially.

[4] Jabri, M. Sydney Univ., NSW, Australia Pickard, S. ; Leon g, P. ; Rigby, G. ; Jiang, J. Flower, B. ; Henderson, P. Mapping a functional neural network model to analog sub-threshold MOS technology is a challenging task, and requires careful architectural, system level and circuit level consideration, with respect to the constraints inherent in this technology. The authors present their experience in this mapping process. The artificial neural network systems addressed are programmable ones facilitating learning either on or off chip. The authors consider multi-layer feedforward networks, although the techniques can be easily adapted to recurrent networks. A multi-layer learning algorithm suitable for analog sub-threshold implementation is presented. The authors discuss system level issues, describe circuits of neurons and synapses that have been designed, and present fabrication results

[5] Wai-Chi Fang review of related work and published literature, a frequency-sensitive self-organization network has been described and shown to be effective for adaptive

vector quantization. The efficiency of this FSO network is measured by its compression ability, the resulting distortion, error tolerance, and the suitability for VLSI implementation. Based upon this frequency-sensitive self-organization method, a neural-based adaptive vector quantizer has been developed. By using a mixed analog-digital design approach in the massively paralleled computation blocks, the advantages of small silicon area, low power consumption, and reduced I/O requirement can be achieved. A VLSI chip for 25-dimensional vector quantizer of 64 code vectors has been fabricated and tested. Its throughput rate is 2 million vectors per second and its equivalent computation power is 3.2 billion connections per second. It achieved an intrinsic compression ratio of 33.

## CONCLUSION

Neural network can be used to extract patterns and to detect trends that are too complex which cannot be noticed by either humans or other computer techniques. It can be used in Modelling and Diagnosing the Cardiovascular System and in Electronic noses which has several potential applications in telemedicine, due to its adaptive learning, self-organization, real time operations and fault tolerance via redundant information coding properties . Another application developed was “Instant Physician” which represents the “best” diagnosis and treatment with high speed low power, CMOS circuit (Layout extraction) in current mode as well as for nano scale circuit simulation using Double Gate MOSFET (DG MOSFET) modeling.

## REFERENCES

- [1] Neeraj Chasta 1, Sarita Chouhan<sup>2</sup> and Yogesh Kumar<sup>3</sup> “ANALOG VLSI IMPLEMENTATION OF NEURAL NETWORK ARCHITECTURE FOR SIGNAL PROCESSING” International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.2, April 2012.
- [2] E. Vittoz, et al.,” The design of high performance analog circuits on digital CMOS chips,” IEEE J.Solid State Circuit 20, 1985, pp.657-665
- [3] Wilamowski B. M. "Neuro-Fuzzy Systems and its applications" tutorial at 24th IEEE International Industrial Electronics Conference - IECON'98 August 31 - September 4, 1998, Aachen, Germany, vol. 1, pp. t35-t49.
- [4] jabri m. Pickard s. Leong p. Rigby g. Jiang j. Flower b. Henderson p.” Vlsi implementation of neural networks with application to signal processing” proceedings of the ieee, 78(9):1415-1442, 1990.
- [5] Wai-Chi Fang et al, “A VLSI Neural Processor for Image Data Compression using Self-Organisation Networks” IEEE Transactions on Neural Networks, Vol. 3, No. 3, May 1992, pp. 506-517
- [6] Cyril Prasanna Raj P & S.L. Pinnae “DESIGN AND ANALOG VLSI IMPLEMENTATION OF NEURAL NETWORK ARCHITECTURE FOR SIGNAL PROCESSING” European Journal of Scientific Research ISSN 1450-216X Vol.27No.2 (2009), pp.199-216.
- [7] D. Nguyen a and B. Wid row, Improving the learning speed of 2-layer neural network by choosing initial values of the adaptive weights, IEEE First International Joint Conference on Neural Networks ,3, 21–26, (1990)
- [8] Cyril Prasanna Raj P & S.L. Pinnae “DESIGN AND ANALOG VLSI IMPLEMENTATION OF NEURAL NETWORK ARCHITECTURE FOR SIGNAL PROCESSING” European Journal of Scientific Research ISSN 1450-216X Vol.27No.2 (2009), pp.199-216

- [9] R.A. Jacobs, Increased rates of convergence through learning rate adaptation, *Neural Networks*, 1, 295–307, (1988).
- [10] T. P. Vogl, J. K. Man gis, J.K. Rigler, W. T. Z ink and D .L. Alkon, Accelerating the convergence of the back-propagation method , *Biological Cyberne tics*, 59 , 257–263,(1988).
- [11] Ranjeet Ranade & Sanjay Bhandari & A.N. Chandorkar “VLSI Implementation of Artificial Neural Digital Multiplier and Adder” pp.318-319
- [12] F. Djefal et al., “Design and Simulation of Nanoelectronic DG MOSFET Current Source using Artificial Neural Networks,” *Materials Science and Engineering C*, vol. 27, 2007, pp. 1111-1116
- [13] Isik Aybayetal , Classification of Neural Network Hardware, *Neural Network World* ,IDG Co., Vol6 No1, 1996, pp.11-29.

### BIOGRAPHIES



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