ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 2, Issue 2, February 2014

Design Approach towards High Performance Memory of 6 Transistors SRAM Cell Using 45nm CMOS Technology

Nupur G.Nanoti[1], Prafulla D.Gawande[2]

PG student, Department of Electronics & Telecommunication, Sipna's college of Engineering & Technology, Amravati, Maharashtra, India [1]

Associate Professor, Department of Electronics & Telecommunication, Sipna's college of Engineering & Technology, Amravati, Maharashtra, India [2]

Abstract: Semiconductor memory arrays capable of storing large quantities of digital information are essential to all digital systems. The amount of memory required in a particular system depends on the type of application, but, in general, the number of transistors utilized for the information (data) storage function is much larger than the number of transistors used in logic operations and for other purposes. The ever-increasing demand for larger data storage capacity has driven the fabrication technology and memory development towards more compact design rules and, consequently, toward higher data storage densities. The trend towards higher memory density and larger storage capacity will continue to push the leading edge of digital system design. The Microwind 3.1 software will allow designing and simulating an integrated circuit at physical description level. The main novelties related to the 45 nm technology are the high-k gate oxide, metal gate and very low-k interconnect dielectric. The effective gate length required for 45 nm technology is 25nm. Low Power (0.211mwatt), high speed static RAM area efficient chip is designed using 45 nm CMOS technology.

Keywords: 6T Static RAM cell, memory, 45nm VLSI technology, low power.

I. INTRODUCTION

Static Random Access Memory: This form of semiconductor memory gains its name from the fact that, unlike DRAM, the data does not need to be refreshed dynamically. It is able to support faster read and write times than DRAM (typically 10 ns against 60 ns for DRAM), and in addition its cycle time is much shorter because it does not need to pause between accesses. However it consumes more power, is less dense and more expensive than DRAM. Effort has been taken to design Low Power, High performance Static RAM, using VLSI technology. The design process, at various levels, is usually evolutionary in nature. It starts with a given set of requirement. When the requirements are not met, the design has to be improved. More simplified view of the VLSI technology consists of various representations, abstractions of design, logic circuits, CMOS circuits and physical layout. [11]

This paper introduces design aspects for layout design of static RAM memory using VLSI technology. This Static RAM is designed using latest 45nm process technology parameters, which in turn offers high speed performance at low power. There is a large variety of types of ROM and RAM that are available. These arise from the variety of applications and also the number of technologies available. This means that there are a large number of abbreviations or acronyms and categories for memories ranging from Flash to MRAM, PROM to EEPROM, and many more. [14]

II. LITERATURE REVIEW

From the rigorous review of related work and published literature, it is observed that many researchers have designed MOS memory by applying different techniques. Researchers have undertaken different systems, processes or phenomena with regard to design and analyse MOS memory. Since in the real world today VLSI/CMOS is in very much in demand, from the careful study of reported work it is observed that very few researchers have taken a work for designing MOS memory with CMOS/VLSI technology. In July 2008, B. Amelifard, F. Fallah and M.Pedram was worked on a method which based on dual-Vt and dual-Tox assignment to reduce the total leakage power dissipation of static random access memories(SRAM).[9] In September-Octomber 2010 Dr. Ujwala A.Belorkar has researched on application of 45nm VLSI technology to design layout of static RAM memory. [13]

From the careful study of reported work, it is observed that researchers have proposed various techniques to design the chip and to improve its characteristics and various parameters but up to the result of my survey regarding 6T static RAM cell design. It is also well known to that; VLSI technology is the fastest growing field today. And according to Moore's law which state that the numbers of transistors on an integrated circuit will double every 18 months. By scaling down the technology, we can optimize the parameters like power consumption.

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 2, Issue 2, February 2014

The current technology up to 2008 was lower range of nm technology. Hence considering the advancement of future technology and the advantage of 45 nm technology over 65 and 90 nm technologies, the proposed project has been decided to do with the selection of higher order of nm technology. Considering all this constraint regarding the demand of today's fast communication world, the research has been taken to design low power memory cell using 45nm VLSI technology.

III. SYSTEM ARCHITECTURE

A. Static RAM Cell Design

The static RAM is a very important class of memory. It consists of two cross-coupled inverters, which form a positive feedback with two possible states illustrated in figure1given below. [11]

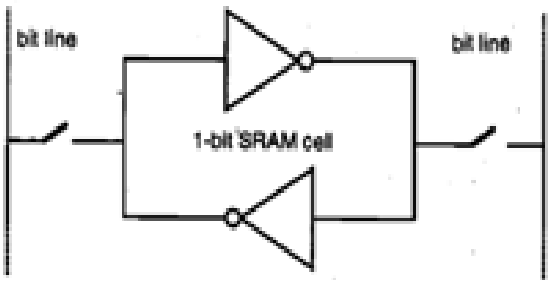
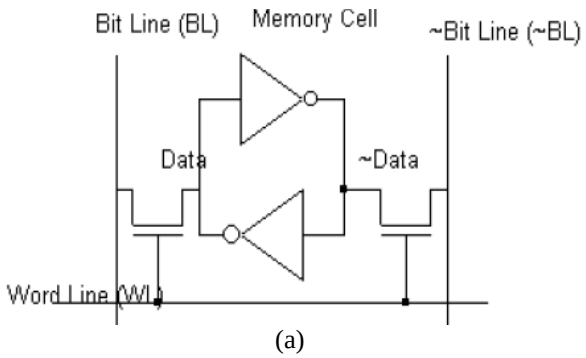


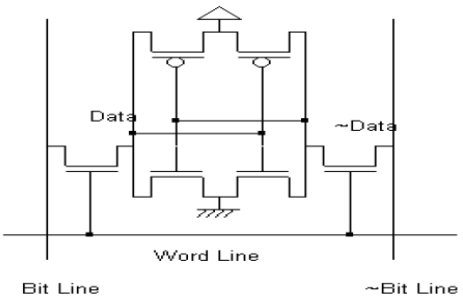
Fig. 1 Static RAM Cell

B. The 6 Transistor Memory Cell

The memory cell has shown in fig 2 (a) forms the basis for most static random-access memories in CMOS technology. It uses six transistors in fig.2 (b) to store and access one bit. The four transistors in the center form two cross-coupled inverters. In actual devices, these transistors are made as small as possible to save chip-area, and are very weak. Due to the feedback structure, a low input value on the first inverter will generate a high value on the second inverter, which amplifies (and stores) the low value on the second inverter. Similarly, a high input value on the first inverter will generate a low input value on the second inverter, which feeds back the low input value onto the first inverter. Therefore, the two inverters will store their current logical value, whatever value that is.



(a)



(b)

Fig. 2 The 6T transistor static memory cell

C. Design Steps

Every step of design follows the design flow of Microwind 3.1 software. The design methodology will be according to VLSI backend design flow. The main target is to design and analyse the hybrid architecture of memory for future high performance engines.

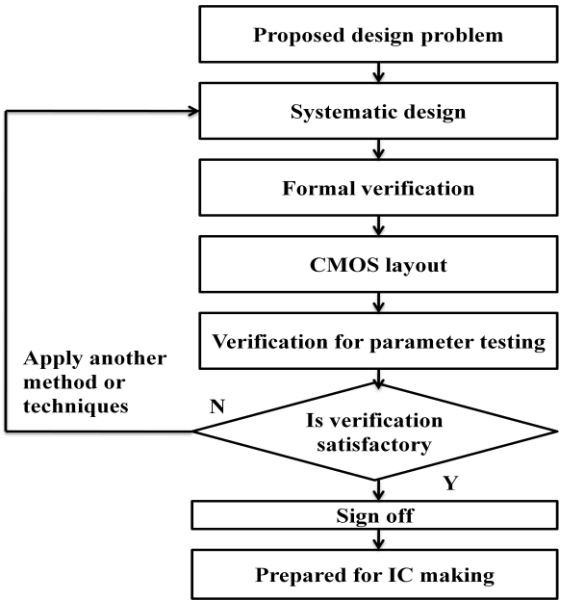


Fig. 3 Design Flow Chart

To achieve the proposed target following steps are included in the design and analysis of proposed memory.

1. Schematic design of proposed memory cell using CMOS transistors.
2. Performance verification of the above for different parameters.
3. CMOS layout for the proposed memory cell using VLSI backend.
4. Verification of CMOS layout and parameter testing.

If the goal is achieved for all proposed parameter including detail verification, sing off for the design analysis and design will be ready for IC making. If detail verification of parameters would not complete then again follow the first step with different methodology.

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 2, Issue 2, February 2014

Table-1: Design Rules for CMOS 45nm

Design rules and electrical parameters

Layer	Width	Spacing	Surface	Surf capa	Lin capa	Ctk capa	Res	Unsalicid	Thickn	Height	Permitt
	lambda	lambda	lambda2	af/µm2	af/µm	af/µm	ohm	ohm	µm	µm	
nitride	0	0	0								
siOxNy	800	800	0								
metal6	8	8	100	30.00	25.00	12.00	0.10/sq	1.00/sq	0.50	4.00	2.50
via5	5	5	0				1.00/via		0.50	3.65	4.00
metal5	8	15	16	30.00	20.00	12.00	0.20/sq	1.00/sq	0.35	3.30	2.50
via4	3	4	0				1.00/via		0.50	2.95	4.00
metal4	3	4	16	30.00	20.00	12.00	0.20/sq	1.00/sq	0.35	2.60	2.50
via3	3	4	0				2.00/via		0.50	2.25	4.00
metal3	3	4	16	30.00	20.00	12.00	0.20/sq	1.00/sq	0.35	1.90	2.50
via2	3	4	0				2.00/via		0.50	1.55	4.00
metal2	3	4	16	30.00	20.00	12.00	0.20/sq	1.00/sq	0.35	1.20	2.50
via	3	4	0				1.00/via		0.50	0.85	4.00
metal	3	4	16	28.00	42.00	10.00	0.20/sq	1.00/sq	0.35	0.50	2.50
poly	2	3	16	80.00			4.00/sq	40.00/sq	0.10	0.15	4.00
poly2	2	2	8				4.00/sq	1.00/sq	0.20	0.27	4.00
contact	2	3	0				2.00/via		0.50	0.00	4.00
diffn	4	4	16	350.00	100.00		25.00/sq	250.00/sq	0.10	0.00	4.00
diffp	4	4	16	300.00	100.00		30.00/sq	300.00/sq	0.10	0.00	4.00
nwell	10	11	144	250.00			120.00/sq		0.50	0.00	4.00
oxide				25000.00					1.80nm	(4.00nm)	4.00

D. Simulation Result

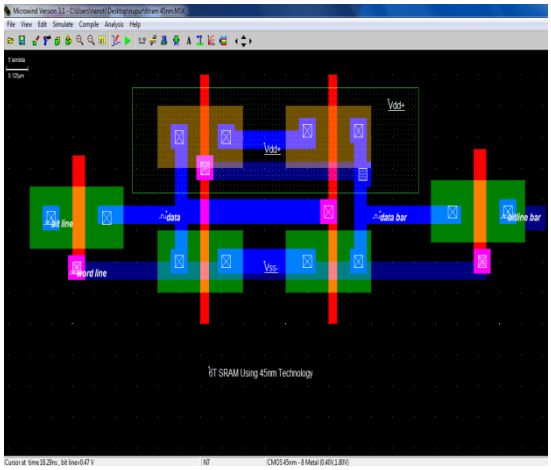


Fig. 4 Layout of the 6 transistor static memory cell

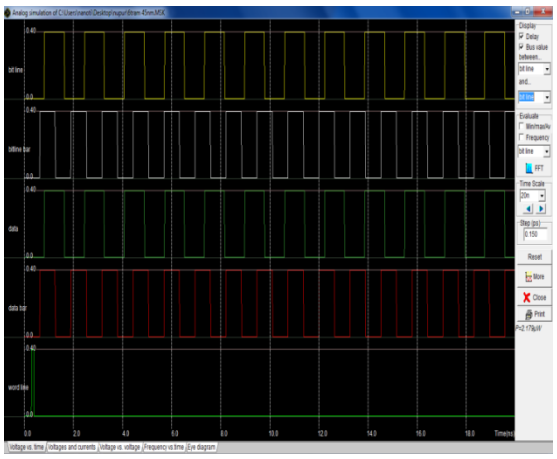


Fig. 5 Simulation for the 6T static RAM memory

The simulation of the RAM cell is proposed in figure 5. At time 0.0, Data reaches an unpredictable value of 1, after an unstable period. Meanwhile, ~Data reaches 0. At time 0.5ns, the memory cell is selected by a 1 on Word Line. As the Bit Line information is 0, the memory cell information Data goes down to 0. At time 1.5ns, the memory cell is selected again. As the Bit Line information is now 1, the memory cell information Data goes to 1. Corresponding to the stored values, cycle, where Bit Line and ~Bit Line signals are floating, the memory sets these wires respectively to 1 and 0.From figure, it is also observed that input at bit line are stored at data line without the delay. Similarly input at bit line bar appeared at data bar line without a delay. The total power consumed is 2.17microwatt.

Table- 2: Features of Dynamic and Static RAM

	DRAM	SRAM
KNOWLEDGE LEVEL	MATURE	MATURE
CELL ELEMENTS	1T1C	6T
HALF PITCH (F) (nm)	50	65
SMALLEST CELL AREA (F^2)	6	140
READ TIME (ns)	<1	<0.3
WRITE/ERASE TIME (ns)	<0.5	<0.3
RETENTION TIME (years)	SECONDS	N/A
WRITE OP. VOLTAGE (V)	2.5	1
READ OP. VOLTAGE (V)	1.8	1
WRITE ENDURANCE	10^{16}	10^{16}
WRITE ENERGY (fJ/bit)	5	0.7
DENSITY (Gbit/cm^2)	6.67	0.17

IV. CONCLUSION

The proposed Memory is designed using 45 nm CMOS/VLSI technology with Microwind 3.1. The main novelties related to the 45 nm technology are the high-k gate oxide, metal gate and very low-k interconnect .The Software used in program allows us to design and simulate an integrated circuit at physical description level. SRAM memory is used where speed or low power are in considerations. Its higher density and less complicated structure also lead it to use in semiconductor memory scenarios where high capacity memory is used, as in the case of the working memory within computers. Proposed layout of static RAM, consumes a very low power supply (0.2 microwatt). Also because of 45nm technology it consumes a very low area. As the number of transistors increases the storage capacity of memory also get increases. As the main aim of memory is to store the data/information. Whatever the input data is given to the memory device, it is expected that the output data should be equal to the input data. Hence 6T SRAM cell is a basic cell and 8T, 10T, 12T static RAM cell are the proposed work using 45 nm CMOS/VLSI technologies with Microwind 3.1.

REFERENCES

[1] M. M. Ziegler and M. R. Stan, "CMOS/nano co-design for crossbar-based molecular electronic systems," IEEE Trans. Nanotechnology, vol. 2, no. 4, pp. 217–230, Dec. 2003.

[2] K. Zhang et al., "SRAM design on 65-nm CMOS technology with dynamic sleep transistor for leakage reduction," IEEE J. Solid-State Circuits, vol. 40, no. 4, pp. 895-901,Apr. 2005.

[3] K. Pagiamtzis and A. Sheikholeslami, "Content-addressable memory (CAM) circuits and architectures:A tutorial and survey," IEEE J. Solid- State Circuits, vol. 41, no. 3, pp. 712–727, Mar. 2006.

[4] M. Yamaoka, N. Maeda, Y. Shinozaki, Y. Shimazaki, K. Nii, S. Shimada, K. Yanagisawa, and T. Kawahara, "90-nm process-variation adaptive embedded SRAM modules with power line-floating write technique," IEEE J. Solid-State Circuits, vol. 41, no. 3, pp. 705–711, Mar.2006.

[5] S. K. Lu and C. H. Hsu, "Fault tolerance techniques for high capacity RAM," IEEE Trans. Reliab., vol. 55, no. 6, pp. 293–306, Jun. 2006.

[6] G. I. Bourianoff, P. A. Gargini, and D. E. Nikonov, "Research directions in beyond CMOS computing," Solid-State Electron., vol. 51, no. 11–12, pp. 1426–1431, 2007.

[7] N. Engheta, "Circuits with light at nanoscales: Optical nanocircuits inspired by metamaterials," Science, vol. 317, no. 5845, pp. 1698–1702, Sept 2007.

[8] Michael Wieckowski, Student Member, IEEE, Sandeep Patil, Student Member, IEEE, and Martin Margala, "Portless SRAM—A High-Performance Alternative to the 6T Methodology,"IEEE J. Solid-State Circuits, vol. 42, no. 11, pp.2600-2610 Nov 2007.

[9] B. Amelifard, F. Fallah and M.Pedram, "Leakage Minimization of SRAM Cells in a Dual-Vt and Dual-Tox Technology" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 16, No. 7,pp.851-860, July 2008.

[10] D. Akinwande, S. Yasuda, B. Paul, S. Fujita, G. Close, and H. S. P.Wong, "Monolithic integration of CMOS VLSI and Carbon Nanotubes for Hybrid Nanotechnology Applications," IEEE Transactions On Nanotechnology, vol. 7, no. 5,pp.636-639 Sept 2008.

[11] S.M.Kang & Y.Leblebici "CMOS Digital Integrated Circuits Analysis and Design,"3rd edition TATA McGraw Hill Edition, pp.405-474.

[12] E. Sicard, Syed Mahfuzul Aziz, "Introducing 45 nm technology in Microwind3" Microwind application note.

[13] Ujwala A. Belorkar, "Application of 45 nm VLSI Technology to Design Layout of Static RAM Memory," International Journal, vol.1.no.3, pp.288-292, Sept-Oct 2010.

[14] K. Eshraghian, Kyoung-Rok Cho, Member, IEEE, O. Kavehei, Student Member, IEEE, Soon-Ku Kang, D. Abbott, Fellow, IEEE, and Sung-Mo S. Kang, Fellow, IEEE, "Memristor MOS Content Addressable Memory (MCAM): Hybrid Architecture for Future High Performance Search Engines," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, no. 8,pp.1407-1417, August 2011.

BIOGRAPHIES

G.Nanoti received the bachelor's degree in Electronics and Telecommunication Engineering from Sipna College of Engineering & Technology, Amravati, Maharashtra, India and currently pursuing M.E in Electronics &Telecommunication from Sipna College of Engineering & Technology, Amravati, Maharashtra, India.

Prafull D.Gawande is currently working as an Associate Professor in Electronics and Telecommunication Engineering Department, Sipna College of Engineering & Technology, Amravati, Maharashtra, India.